

RoHS Compliant

Embedded Multimedia Card 5.1

Industrial EH130 Product Specifications

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Version 1.1



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Product Features

- Packaged NAND flash memory with eMMC 5.1 interface
 - Compliant with eMMC Specification Ver. 4.3, 4.4, 4.41, 4.5, 4.51, 5.0, 5.1
 - Device can be converted to eMMC 4.3, 4.41 (Shows 4.4), 4.51 (Shows 4.5), 5.0 via initializing
- 153-ball FBGA (TFBGA) RoHS compliant package
- Package size: 11.5 x 13.0 x 1.0mm
- Capacity: 8, 16, 32GB
- NAND flash type: TLC
- Operating voltage range:
 - I/O voltage (VCCQ) = 1.7-1.95V/2.7-3.6V
 - Core voltage (VCC) = 2.7-3.6V
- Temperature range:
 - Operating temperature¹: -40°C to 85°C
 - Storage temperature: -40°C to 85°C

eMMC-Specific Features

- High-speed eMMC protocol
- Variable clock frequencies of 0-200MHz
- Ten-wire bus interface (clock, 1 bit command, 8 bit data bus) with a hardware reset
- Supports three different data bus widths: 1 bit (default), 4 bits, 8 bits
- Bus modes
 - Single data transfer rate: up to 52MB/s (using 8 parallel data lines at 52MHz)
 - High speed, single data rate mode (HS-200): up to 200MB/s @ 200MHz
 - High speed, dual data rate mode (HS-400): up to 400MB/s @ 200MHz
- Error free memory access
 - Internal error correction code (ECC) for improved data storage integrity
 - Internal enhanced data management algorithm
 - Data protection for sudden power failure during program operations
- Security
 - Secure erase/trim commands
 - Enhanced write protection with permanent and partial protection options
- Major features
 - HS400, Field Firmware Update (FFU), Power-off Notification, Pre EOL Information, Enhanced Device Life time, Optimal Size
- Major eMMC 5.1 features
 - Command Queuing, Enhanced Strobe, Cache Flushing Report, BKOPS Control, Cache Barrier, RPMB Throughput Improve, Secure Write Protection

Note 1: The temperature surface (Tc) cannot over 95°C.

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Preliminary

1. General Description

Apacer EH130 is an embedded, non-volatile memory system that combines triple-level cell (TLC) NAND flash memory with an onboard eMMC controller, supporting the JEDEC Standard eMMC 5.1 interface. The integrated eMMC controller directly manages NAND flash media, freeing the host processor from various tasks, including ECC, wear-leveling, IOPS optimization, and read sensing.

EH130 serves as the ideal storage solution for a wide range of industrial applications, including embedded systems, factory automation, networking, transportation, aerospace and defense, surveillance, medical equipment, and more. Its compact BGA package sizes and minimal power consumption render eMMC an affordable and efficient memory solution for mobile and embedded products.

Offering capacities ranging from 8GB to 32GB within a JEDEC-compatible form factor, EH130 provides an excellent solution for vendors looking for seamless integration, a quick market entry, and ample storage capacity.

2. Signal Assignments (153-Ball)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NC	NC	DAT0	DAT1	DAT2	VSS	RFU	NC	NC	NC	NC	NC	NC	NC	A
B	NC	DAT3	DAT4	DAT5	DAT6	DAT7	NC	NC	NC	NC	NC	NC	NC	NC	B
C	NC	VDDI	NC	VSSQ	NC	VCCQ	NC	NC	NC	NC	NC	NC	NC	NC	C
D	NC	NC	NC	NC							NC	NC	NC	D	
E	NC	NC	NC		RFU	VCC	VSS	VSF	VSF	VSF		NC	NC	NC	E
F	NC	NC	NC		VCC					VSF		NC	NC	NC	F
G	NC	NC	RFU		VSS					VSF		NC	NC	NC	G
H	NC	NC	NC		DS					VSS		NC	NC	NC	H
J	NC	NC	NC		VSS					VCC		NC	NC	NC	J
K	NC	NC	NC		RST_n	RFU	RFU	VSS	VCC	VSF		NC	NC	NC	K
L	NC	NC	NC								NC	NC	NC	L	
M	NC	NC	NC	VCCQ	CMD	CLK	NC	NC	NC	NC	NC	NC	NC	NC	M
N	NC	VSSQ	NC	VCCQ	VSSQ	NC	NC	NC	NC	NC	NC	NC	NC	NC	N
P	NC	NC	VCCQ	VSSQ	VCCQ	VSSQ	RFU	NC	NC	VSF	NC	NC	NC	NC	P

Figure 2-1 Ball Assignments

3. Product Specifications

3.1 Partition Capacity

Table 3-1 Partition Capacity

Capacity	Boot Partition 1	Boot Partition 2	RPMB
8GB	4096 KB	4096 KB	4096 KB
16GB	4096 KB	4096 KB	4096 KB
32GB	4096 KB	4096 KB	4096 KB

3.2 User Density

Table 3-2 User Density

Capacity	User Density
8GB	8,589,934,592 Bytes
16GB	17,179,869,184 Bytes
32GB	34,359,738,368 Bytes

3.3 Operating and Storage Temperatures

Table 3-3 Operating and Storage Temperatures

Condition	Temperature
Minimum and Maximum Ambient Temperature ¹	-40°C to 85°C
Maximum Case Operating Temperature	95°C
Minimum and Maximum Non-operating Temperature ²	-40°C to 85°C

Notes:

1. To achieve optimized power and performance, ensure that the case temperature does not exceed the maximum ambient operating temperature.
2. After being soldered onto PCBA

3.4 Performance

3.4.1 Typical Sequential Performance

Table 3-4 Sequential Burst Performance: PSA Pseudo-SLC Burst Status

Speed Mode and Operation			Sequential Burst Performance (MB/s)		
			8GB	16GB	32GB
HS400	Write Cache on	Read	260	280	280
		Write	110	220	230
	Write Cache off	Read	270	290	290
		Write	100	190	200
HS200	Write Cache on	Read	170	170	170
		Write	110	140	140
	Write Cache off	Read	170	170	170
		Write	100	130	130
DDR52	Write Cache on	Read	80	80	80
		Write	70	70	70
	Write Cache off	Read	80	80	80
		Write	60	70	70
SDR52	Write Cache on	Read	40	40	40
		Write	40	40	40
	Write Cache off	Read	40	40	40
		Write	40	40	40

Notes:

- Performance values may be subject to changes without notice
- Values are given at an 8-bit bus width, running on Apacer proprietary tool.
- Performance is measured at VCC = 3.3V, VCCQ = 1.8V in HS400 and HS200 mode and at VCC = 3.3V, VCCQ = 3.3V in DDR52MHz and SDR52MHz mode.
- The write cache size is 128KB.

Table 3-5 Sequential Sustained Performance: Normal Status

Speed Mode and Operation			Sequential Sustained Performance (MB/s)		
			8GB	16GB	32GB
HS400	Write Cache on	Read	260	280	280
		Write	110	220	230
	Write Cache off	Read	270	290	290
		Write	100	190	200
HS200	Write Cache on	Read	170	170	170
		Write	110	140	140
	Write Cache off	Read	170	170	170
		Write	100	130	130
DDR52	Write Cache on	Read	80	80	80
		Write	70	70	70
	Write Cache off	Read	80	80	80
		Write	60	70	70
SDR52	Write Cache on	Read	40	40	40
		Write	40	40	40
	Write Cache off	Read	40	40	40
		Write	40	40	40

Notes:

- Performance values may be subject to changes without notice
- Values are given at an 8-bit bus width, running on Apacer proprietary tool.
- Performance is measured at VCC = 3.3V, VCCQ = 1.8V in HS400 and HS200 mode and at VCC = 3.3V, VCCQ = 3.3V in DDR52MHz and SDR52MHz mode.
- The write cache size is 128KB.

3.4.2 Typical Random Performance

Table 3-6 Random Burst Performance: PSA Pseudo-SLC Burst Status

Speed Mode and Operation			Random Burst Performance (IOPS)		
			8GB	16GB	32GB
HS400	Write Cache on	Read	10000	18400	22600
		Write	25900	28700	25700
	Write Cache off	Read	10000	18500	22800
		Write	2700	2800	2800
HS200	Write Cache on	Read	5800	5600	5100
		Write	22400	24300	22300
	Write Cache off	Read	5800	5600	5700
		Write	2700	2700	3100
DDR52	Write Cache on	Read	5000	4800	4500
		Write	14200	14700	14200
	Write Cache off	Read	5000	4800	4500
		Write	2500	2500	2500
SDR52	Write Cache on	Read	4200	4100	3800
		Write	9100	9300	9100
	Write Cache off	Read	4200	4000	3800
		Write	2300	2300	2300

Notes:

- Performance values may be subject to changes without notice
- Values are given at an 8-bit bus width, running on Apacer proprietary tool.
- Performance is measured at VCC = 3.3V, VCCQ = 1.8V in HS400 and HS200 mode and at VCC = 3.3V, VCCQ = 3.3V in DDR52MHz and SDR52MHz mode.
- The write cache size is 128KB.

Table 3-7 Random Sustained Performance: Normal Status

Speed Mode and Operation			Sequential Sustained Performance (IOPS)		
			8GB	16GB	32GB
HS400	Write Cache on	Read	10000	18400	22600
		Write	4300	5400	5200
	Write Cache off	Read	10000	18600	22800
		Write	1800	1900	1900
HS200	Write Cache on	Read	5700	5500	5000
		Write	19200	22100	22800
	Write Cache off	Read	5700	5500	5700
		Write	2600	2700	3100
DDR52	Write Cache on	Read	4900	4800	4400
		Write	12800	14000	14300
	Write Cache off	Read	4900	4700	4400
		Write	2400	2500	2500
SDR52	Write Cache on	Read	4100	4000	3800
		Write	8500	9100	9200
	Write Cache off	Read	4100	4000	3800
		Write	2200	2300	2300

Notes:

- Performance values may be subject to changes without notice
- Values are given at an 8-bit bus width, running on Apacer proprietary tool.
- Performance is measured at VCC = 3.3V, VCCQ = 1.8V in HS400 and HS200 mode and at VCC = 3.3V, VCCQ = 3.3V in DDR52MHz and SDR52MHz mode.
- The write cache size is 128KB.

4. Electrical Specifications

4.1 Operating Voltage

Table 4-1 Operating Voltage

Symbol		Min	Max	Unit
VCCQ	1.8V	1.7	1.95	V
	3.3V	2.7	3.6	V
VCC	3.3V	2.7	3.6	V

4.2 Power Consumption

Table 4-2 RMS Current Consumption

Speed Mode and Operation			Unit	8GB	16GB	32GB
HS400	Read	ICC	mA	85	95	105
		ICCQ		145	150	155
	Write	ICC		65	105	175
		ICCQ		75	85	80
HS200	Read	ICC		70	70	80
		ICCQ		110	110	110
	Write	ICC		65	95	175
		ICCQ		75	75	80
DDR52	Read	ICC		50	50	60
		ICCQ		85	85	85
	Write	ICC		60	95	175
		ICCQ		65	70	75
SDR52	Read	ICC	40	40	45	
		ICCQ	75	75	75	
	Write	ICC	60	95	175	
		ICCQ	65	70	75	

Notes:

- Power consumption values may be subject to changes without notice
- The measurement for the maximum RMS current is calculated as the average RMS current consumption over a 100ms period.
- The RMS current is measured at TA = 25°C, VCC = 3.3V, VCCQ = 1.8V in HS400 and HS200 mode and at VCC = 3.3V, VCCQ=3.3V in DDR52MHz and SDR52MHz mode, 8-bit bus width without clock frequency.

Table 4-3 Standby Current Consumption

Speed Mode and Operation		Unit	8GB	16GB	32GB
HS400	Sleep	uA	75	75	75
	Standby ICCQ		105	105	105
	Standby ICC		30	40	50
HS200	Sleep		75	75	75
	Standby ICCQ		105	105	105
	Standby ICC		30	40	50
DDR52	Sleep		75	75	75
	Standby ICCQ		105	105	105
	Standby ICC		30	50	50
SDR52	Sleep		75	75	75
	Standby ICCQ		105	105	105
	Standby ICC		30	40	50

Notes:

- Power consumption values may be subject to changes without notice
- Standby current is measured at TA = 25°C, VCC = 3.3V, VCCQ = 1.8V in HS400 and HS200 mode and at VCC = 3.3V, CCQ = 3.3V in DDR52MHz and SDR52MHz mode, 8-bit bus width without clock frequency.

Preliminary

5. eMMC Device and System

5.1 eMMC System Overview

The eMMC specification addresses the behavior of the interface and the device controller. While this specification implies the presence of a host controller and a memory storage array, it does not fully define their operation.

Apacer EH130 comprises a single-chip MMC controller and a NAND flash memory module. The microcontroller interfaces with a host system, facilitating the reading and writing of data to and from the NAND flash memory module. This controller allows the host to operate independently from the intricacies of erasing and programming the flash memory.

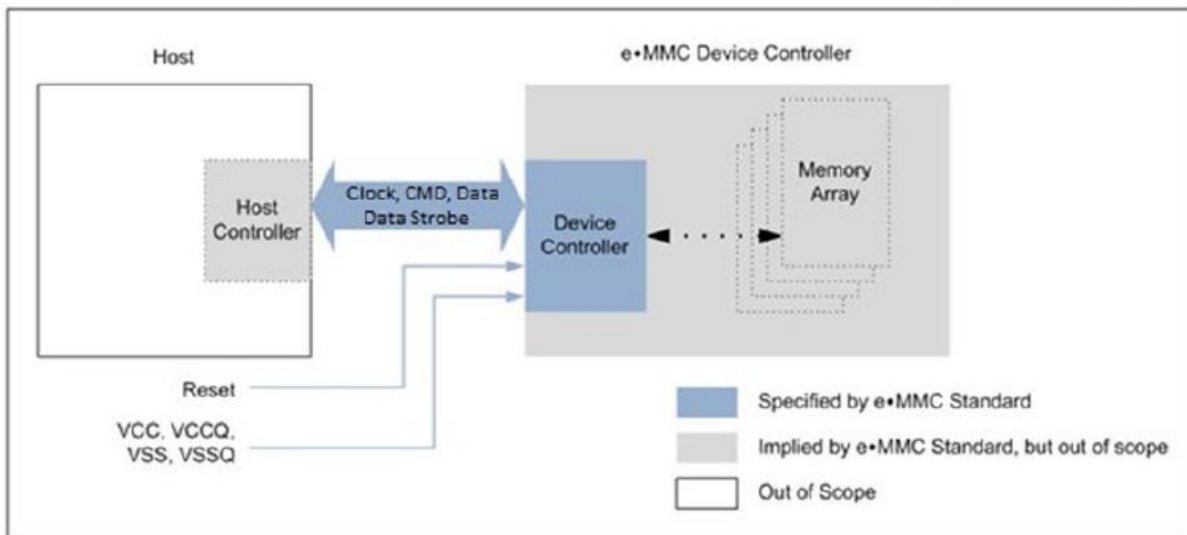


Figure 5-1 eMMC System Overview

5.2 Memory Addressing

Previous implementations of the eMMC specification followed byte addressing with a 32-bit field. This addressing mechanism allowed for eMMC densities up to and including 2GB.

To support larger densities, the addressing mechanism was updated to accommodate sector addresses (512B sectors). Sector addresses should be used for all devices with a capacity larger than 2GB.

To determine the addressing mode, the host should read bit [30:29] in the OCR register.

5.3 Signal Descriptions

Apacer EH130 transfers data via a number of data bus signals. The communication signals are summarized in the table below.

Table 5-1 Signal Descriptions

Name	Type	Description
CLK	I	Clock: Each cycle of this signal directs a one bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency.
DAT[7:0]	I/O/PP	Data: These are bidirectional data channels. The DAT signals operate in push-pull mode. Only the device or the host is driving these signals at a time. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0-DAT7, by the eMMC host controller. The eMMC device includes internal pull-ups for data lines DAT1-DAT7. Immediately after entering the 4-bit mode, the Device disconnects the internal pull ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering to the 8-bit mode the Device disconnects the internal pull-ups of lines DAT1-DAT7.
CMD	I/O/PP/OD	Command: This signal is a bidirectional command channel used for device initialization and transfer of commands. The CMD signal has two operation modes: open-drain for initialization mode, and push-pull for fast command transfer. Commands are sent from the eMMC host controller to the eMMC Device and responses are sent from the device to the host.
DS	O/PP	Data Strobe: This signal is generated by the device and used for output in HS400 mode. The frequency of this signal follows the frequency of CLK. For data output each cycle of this signal directs two bits transfer(2x) on the data - one bit for positive edge and the other bit for negative edge. For CRC status response output and CMD response output (enabled only HS400 enhanced strobe mode), the CRC status is latched on the positive edge only, and don't care on the negative edge.
RST_n	I	Hardware Reset: By default, hardware reset is disabled and must be enabled in the EXT_CSD register if used. Otherwise, it can be left un-connected.
VCC	S	Supply voltage for core
VCCQ	S	Supply voltage for I/O
VSS	S	Supply voltage ground for core
VSSQ	S	Supply voltage ground for I/O
VDDi	-	Connect a capacitor from VDDi to GND to stabilize internal power.
NC	-	Not Connected. Leave floating
RFU	-	Reserved for future use. Leave floating
VSF	-	Vendor Specific Function. Reserved for test points on the PCB, default status is NU (Not Used).

Note: I: input; O: output; PP: push-pull; OD: open-drain; NC: Not connected (or logical high); S: power supply.

6. eMMC 5.1 Selected Features

6.1 Pseudo Technology (pSLC)

Each cell in a TLC NAND can be programmed to store 3 bits of data, with 8 total voltage states. In Pseudo-SLC (pSLC) mode, the memory cell is used in 1-bit mode, resulting in higher endurance, lower error rates, and an extended temperature range. The firmware of the eMMC device is optimized with Pseudo technology to achieve industrial-level reliability. In the eMMC device, Pseudo SLC (pSLC) mode provides one-quarter of the capacity of TLC mode.

6.2 Field Firmware Update (FFU)

Field Firmware Updates (FFU) enable feature enhancements in the field. Through this mechanism, the host downloads a new version of the firmware to the eMMC device and, after a successful download, instructs the eMMC device to install the newly downloaded firmware.

To initiate the FFU process, the host first checks if the eMMC device supports FFU capabilities by examining the SUPPORTED_MODES and FW_CONFIG fields in the EXT_CSD. If the eMMC device supports the FFU feature, the host can begin the FFU process. The FFU process commences by transitioning to FFU Mode in the MODE_CONFIG field of the EXT_CSD. While in FFU Mode, the host should employ either closed-ended or open-ended commands for downloading the new firmware and reading vendor proprietary data. In this mode, the host should set the argument of these commands as defined in the FFU_ARG field. If these commands use a different argument, the device's behavior is undefined, and the FFU process may fail. The host should set the Block Length to be DATA_SECTOR_SIZE. The downloaded firmware bundle must align with DATA_SECTOR_SIZE (internal padding of the bundle might be required). Once in FFU Mode, the host may send the new firmware bundle to the device using one or more write commands.

To revert to regular write and read functionality, the host can restore the MODE_CONFIG field in the EXT_CSD to the Normal state. Exiting FFU Mode prematurely may result in the abortion of the firmware download operation. If the host switches back to FFU Mode, it should examine the FFU Status to determine the number of sectors downloaded successfully, which can be done by reading the NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED in the extended CSD. If the number of sectors downloaded successfully is zero, the host should restart the downloading process from the first sector. If the number of successfully downloaded sectors is positive, the host should resume the download from the next sector, thereby continuing the firmware download operation.

In cases where the MODE_OPERATION_CODES field is not supported by the device, the host should transition to the NORMAL state and initiate a CMD0/HW_Reset/Power cycle to install the new firmware. In such a scenario, the device doesn't need to use NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED. In both cases, if a CMD0/HW_Reset/Power occurs before the host has successfully downloaded the new firmware bundle to the device, it may cause the firmware download process to be aborted.

6.3 Power-off Notifications for Sleep

The host should notify the device before powering the device off. This notification allows the device to better prepare itself for the impending power-off operation. "Powering the device off" refers to turning off all its power supplies. Specifically, the host should issue a power-off notification (POWER_OFF_LONG or POWER_OFF_SHORT) if it intends to turn off both VCC and VCCQ power. Alternatively, it may use a power-off notification (SLEEP_NOTIFICATION) if its intention is to turn off VCC after transitioning the device to the Sleep state.

To signal to the device that it supports power-off notifications, a supporting host should initially set the POWER_OFF_NOTIFICATION byte in EXT_CSD [34] to POWERED_ON (0x01). To perform a power-off operation, before shutting down the device, the host changes the value to either POWER_OFF_SHORT (0x02) or POWER_OFF_LONG (0x03). The host should then wait for the busy line to be de-asserted. Once the setting has changed to either 0x02 or 0x03, the host can safely power off the device.

If the host wants to enter or exit the Sleep state and has set the POWER_OFF_NOTIFICATION byte to POWERED_ON, it may issue the SLEEP_AWAKE command (CMD5). Before transitioning to the Standby state and then to the Sleep state, the host sets POWER_OFF_NOTIFICATION to SLEEP_NOTIFICATION and waits for the DAT0 line to be de-asserted. While in the Sleep (slp) state, VCC (Memory supply) may be turned off as defined in Section 6.6.21 of the JEDEC Standard Specification No. JESD84-B51 other than VCC while the device is in the Sleep (slp) state may result in undefined device behavior. Before removing all power supplies, the host should transition the device out of the Sleep (slp) state back to the Transfer state using CMD5 and CMD7, and then execute a power-off notification by setting the POWER_OFF_NOTIFICATION byte to either POWER_OFF_SHORT or POWER_OFF_LONG.

If the host continues to send commands to the device after switching to the power-off settings (POWER_OFF_LONG, POWER_OFF_SHORT, or SLEEP_NOTIFICATION) or performs HPI during its busy condition, the device shall restore the POWER_OFF_NOTIFICATION byte to POWERED_ON. If the host attempts to change the POWER_OFF_NOTIFICATION to 0x00 after writing another value, a SWITCH_ERROR is generated.

The difference between the two power-off modes is how urgently the host wishes to turn the power off. The device should respond to POWER_OFF_SHORT quickly within the generic CMD6 timeout. If more time is acceptable, POWER_OFF_LONG may be used, and the device should respond to it within the POWER_OFF_LONG_TIME timeout.

While POWER_OFF_NOTIFICATION is set to POWERED_ON, the device expects the host to:

- Maintain the device power supplies in their active mode (both VCC and VCCQ).
- Avoid intentionally powering off the device before changing POWER_OFF_NOTIFICATION to either POWER_OFF_LONG or POWER_OFF_SHORT.
- Refrain from intentionally powering off VCC before changing POWER_OFF_NOTIFICATION to SLEEP_NOTIFICATION and before transitioning the device to the Sleep state.

Before transitioning to the Sleep state, hosts may set the POWER_OFF_NOTIFICATION byte to SLEEP_NOTIFICATION (0x04) if they are aware that the device is capable of autonomously initiating background operations for potential performance improvements. The host should wait for the busy line to be de-asserted. The busy line may be asserted for a period defined in the SLEEP_NOTIFICATION_TIME byte in EXT_CSD [216]. Once the setting has changed to 0x04, the host can set the device into Sleep mode (CMD7+CMD5). After exiting Sleep mode, the POWER_OFF_NOTIFICATION byte will restore its value to POWERED_ON. HPI may interrupt the SLEEP_NOTIFICATION operation. In that case, the POWER_OFF_NOTIFICATION byte will be restored to POWERED_ON.

6.4 Write Cache

Cache is a temporary storage space within an eMMC device. In typical cases, the cache is designed to reduce access time and increase speed when compared to accessing the main nonvolatile storage. It's important to note that the cache is not directly accessible by the host. This temporary storage space may also serve various implementation-specific functions, such as acting as execution memory for the memory controller or storing an address mapping table.

However, there is a risk of data inconsistency when using a nonvolatile cache. It's recommended to enable the cache only for applications that do not require extremely high reliability.

By default, the cache shall be OFF after power-up, RST_n assertion, or CMD0. All access operations should be directed to the nonvolatile storage, as defined elsewhere in this specification. The cache function can be turned ON and OFF by writing to the CACHE_CTRL byte (EXT_CSD byte [33]). Enabling the cache shall follow the behavior model defined in this section, while disabling the cache shall trigger the flushing of data to the nonvolatile storage.

6.5 Cache Enhancement Barrier

The barrier function provides a way to perform delayed, in-order flushing of cached data. The primary motivation for using barrier commands is to avoid the extended delay introduced by flush commands. There are situations where the host doesn't need to flush data immediately but wants to maintain the order between different batches of cached data. The barrier command allows the host to achieve in-order processing without incurring the flush delay since the actual flushing can be deferred by the device to a later idle time. The formal definition of the barrier rule is as follows:

Let's denote a sequence of requests as R_i , where i ranges from 0 to N . Assuming a barrier is set between requests R_x and R_{x+1} ($0 < x < N$), all the requests from R_0 to R_x must be flushed to the non-volatile memory before any of the requests from R_{x+1} to R_N . Between two barriers, the device has the flexibility to write data into non-volatile memory in any order. If the host wishes to preserve a specific order, it should flush the cache or set another barrier at a point where order is crucial.

To set a barrier, the host writes to the BARRIER bit of the FLUSH_CACHE byte (EXT_CSD byte [32]). Any errors resulting from this operation can be read from the status register using CMD13 after the programming process is completed, as defined for a regular write request. These errors could potentially affect any data written to the cache since the previous flush operation.

The device should support any number of barrier commands between two flush commands. In cases where there are multiple barrier commands between two flush commands, a subset of the cached data may be written to nonvolatile memory in accordance with the barrier rule. Internally, the device may have an upper limit on the number of barriers it can accommodate without performing a cache flush. If the host exceeds this barrier limit, the device may internally issue a normal flush.

The device's support for barrier function should be indicated via the BARRIER_SUPPORT byte (EXT_CSD byte [486]). If a device does not support the barrier function, this register shall be zero. If a device supports the barrier function, this register shall be set to one.

Assuming the device supports the barrier function, when the BARRIER bit of the FLUSH_CACHE byte is set, a barrier operation should be executed.

If the cache becomes entirely full or cannot accommodate the data for the next access (as per the block count indicated in CMD23 or for any initiated single/open-ended multiple block write in general), it remains the responsibility of the eMMC device to store the data for the next access within the specified timeouts, as described elsewhere in this specification. The specific algorithm for managing the new data and any potential flushing of older cached data is left to the implementation.

Note: When issuing a force-programming write request (CMD23 with bit 24 on) or a reliable write request (CMD23 with bit 31 on), the host should be aware that the data may be written to non-volatile

memory before any cached data, even if a barrier command was issued. Therefore, if the writing order to non-volatile memory is crucial, it is the host's responsibility to issue a flush command before the force-programming or reliable-write request.

To use the barrier function, the host should set bit 0 of BARRIER_EN (EXT_CSD byte [31]). It's important to note that the barrier feature is optional for an eMMC device.

6.6 Cache Flushing Policy

The host may occasionally require the eMMC device to flush cache data in a specific, in-order manner. To ensure this order, the host can use cache barrier commands or instruct the device to perform a cache flush.

However, if the eMMC device's default flushing policy is to naturally flush cache data in a First-In-First-Out (FIFO) order, the use of cache barrier or flush commands to guarantee flushing order becomes redundant. This redundancy imposes unnecessary overhead on both the device and the host.

The FIFO bit in the CACHE_FLUSH_POLICY field (EXT_CSD byte [240]) is utilized by the device to inform the host that its cache flushing policy follows a First-In-First-Out sequence. In this case, the device ensures that the order of data flushing matches the order in which the data was written to the cache. When the FIFO bit is set, it is advisable for the host to refrain from sending cache barrier commands or flush operations aimed at guaranteeing a specific flushing order. These commands become redundant and can unnecessarily burden the system.

However, if the FIFO bit is set to 1b (binary 1) and the device still supports the cache barrier mechanism, the host can send barrier commands without encountering errors. Despite this, the device's behavior remains consistent as it naturally flushes cache data in the correct order.

It's important to note that the CACHE_FLUSH_POLICY field is read-only, and its value remains unchanged by both the host and the device.

6.7 Command Queuing (Disabled by default)

To facilitate command queuing in eMMC, the device manages an internal task queue to which the host can queue data transfer tasks. Initially, the task queue is empty. Every task is issued by the host and initially queued as pending. The device controller works to prepare pending tasks for execution. When a task is ready for execution, its state changes to "ready for execution." The exact meaning of "ready for execution" is left for device implementation. The host tracks the state of all queued tasks and may order the execution of any task marked as "ready for execution" by sending a command indicating its task ID. When the execute command is received (CMD46/CMD47), the device executes the data transfer transaction.

For example, to queue a write transaction, the host sends a CMD44 indicating the task's parameters. The device responds, and the host sends a CMD45, indicating the start block address. The device regards the two commands as a single task in the queue and sends a response indicating success if no error is detected. This exchange may be executed on the CMD line while a data transfer or busy state is ongoing on the DAT lines. The host tracks the state of the queue using CMD13.

At a later time, when data transfer is not in progress, the host issues a CMD47, ordering the device to execute a task from the queue, providing the Task ID in its argument. The device responds with an R1 response, and the data transfer starts.

Note that if hosts need to access the RPMB partition, the host should disable the Command Queue mechanism and access the RPMB partition not through the command queue. General Purpose partitions may be accessed when command queuing is enabled. The queue must be empty when CMD6 is sent (to switch partitions or to disable command queuing). Sending CMD6 while the queue is

not empty shall be regarded as an illegal command (refer to Section 6.6.39.9 of the JEDEC Standard Specification No. JESD84-B51 for details). Prior to enabling command queuing, the block size shall be set to 512B. The device may respond with an error to CMD46/CMD47 if the block size is not 512B.

Preliminary

7. Register Settings

Within the device interface, six registers are defined: OCR, CID, CSD, EXT_CSD, RCA, and DSR. These can only be accessed by the corresponding commands (refer to Section 6.10 of JEDEC Standard Specification No. JESD84-B51 for details).

7.1 OCR Register

The 32-bit operation conditions register (OCR) stores the VDD voltage profile of the device and the access mode indication. In addition, this register includes a status information bit. This status bit is set if the device-power-up procedure has been completed. The OCR register shall be implemented by all devices.

Table 7-1 OCR Register

OCR bit	VDD Voltage Window	High Voltage Value	Dual Voltage Value
[6:0]	Reserved	00 00000b	00 00000b
[7]	1.70-1.95V	0b	1b
[14:8]	2.0-2.7V	000 0000b	000 0000b
[23:15]	2.7-3.6V	1 1111 1111b	1 1111 1111b
[28:24]	Reserved	0 0000b	0 0000b
[30:29]	Access mode	00b (byte mode) 10b (sector mode)	00b (byte mode) 10b (sector mode)
[31]	Device power up status bit (busy) ¹		

Note:

1. This bit is set to LOW during the device's power-up routine.

7.2 CID Register

The Card Identification (CID) register is 128 bits wide. It contains the device identification information used during the device identification phase as required by eMMC protocol. Refer to JEDEC Standard Specification No. JESD84-B51 for details.

Table 7-2 CID Register

CID Filed Name	Field	Width	CID Slice	Value
Manufacturer ID	MID	8	[127:120]	32h
Reserved	-	6	[119:114]	0h
Device/BGA	CBX	2	[113:112]	1h
OEM/Application ID	OID	8	[111:104]	1h
Product name	PNM	48	[103:56]	8GB: 4D4D43303847h (MMC8GB) 16GB: 4D4D43313647h (MMC16G) 32GB: 4D4D43333247h (MMC32G)
Product revision	PRV	8	[55:48]	51h
Product serial number	PSN	32	[47:16]	Random by production
Manufacturing date	MDT	8	[15:8]	Month, Year
CRC7 checksum	CRC	7	[7:1]	See Note 1

CID Filed Name	Field	Width	CID Slice	Value
Reserved	-	1	[0:0]	1h

Note:

- The descriptions are same as eMMC JEDEC standard.

7.3 CSD Register

The Card-Specific Data (CSD) register provides information on how to access the contents stored in eMMC. The CSD registers are used to define the error correction type, maximum data access time, data transfer speed, data format...etc. For details, refer to Section 7.3 of the JEDEC Standard Specification No.JESD84-B51.

Table 7-3 CSD Register

Name	Field	Width	Cell Type	CSD Slice	Value
CSD structure	CSD_STRUCTURE	2	R	[127:126]	3h
System specification version	SPEC_VERS	4	R	[125:122]	4h
Reserved	-	2	R	[121:120]	0h
Data read access-time 1	TAAC	8	R	[119:112]	4Fh
Data read access-time 2 in CLK cycles (NSAC100) ¹	NSAC	8	R	[111:104]	1h
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	32h
Device command classes	CCC	12	R	[95:84]	8F5h
Max. read data block length	READ_BL_LEN	4	R	[83:80]	9h
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0h
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0h
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0h
DSR implemented	DSR_IMP	1	R	[76:76]	0h
Reserved	-	2	R	[75:74]	0h
Device size	C_SIZE	12	R	[73:62]	FFFh
Max. read current @ VDD min	VDD_R_CURR_MIN	3	R	[61:59]	7h
Max. read current @ VDD max	VDD_R_CURR_MAX	3	R	[58:56]	7h
Max. write current @ VDD min	VDD_W_CURR_MIN	3	R	[55:53]	7h
Max. write current @ VDD max	VDD_W_CURR_MAX	3	R	[52:50]	7h
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	7h
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	1Fh
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	1Fh
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0Fh
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	1h
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0h
Write speed factor	R2W_FACTOR	3	R	[28:26]	2h
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	9h
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0h

Name	Field	Width	Cell Type	CSD Slice	Value
Reserved	-	4	R	[20:17]	0h
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0h
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0h
Copy flag (OTP)	COPY	1	R/W	[14:14]	0h
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0h
Temporary write protection	TMP_WRITE_PROTECT	1	R/W	[12:12]	0h
File format	FILE_FORMAT	2	R/W	[11:10]	0h
ECC code	ECC	2	R/W	[9:8]	0h
CRC	CRC	7	R/W	[7:1]	2Eh
Reserved	-	1		[0:0]	1h

Note:

1. Subject to change according to the firmware release note.

7.4 Extended CSD Register

The Extended CSD register defines the device properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the device capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the device is working in. These modes can be changed by the host by means of the SWITCH command.

Table 7-4 Extended CSD Register

Name	Field	Size (Bytes)	CSD Slice	Value
Reserved	-	6	[511:506]	0h
Extended Security Commands Error	EXT_SECURITY_ERR	1	[505]	0h
Supported Command Sets	S_CMD_SET	1	[504]	1h
HPI features	HPI_FEATURES	1	[503]	1h
Background operations support	BKOPS_SUPPORT	1	[502]	1h
Max packed read commands	MAX_PACKED_READS	1	[501]	3Ch
Max packed write commands	MAX_PACKED_WRITES	1	[500]	20h
Data Tag Support	DATA_TAG_SUPPORT	1	[499]	1h
Tag Unit Size	TAG_UNIT_SIZE	1	[498]	3h
Tag Resources Size	TAG_RES_SIZE	1	[497]	0h
Context management capabilities	CONTEXT_CAPABILITIES	1	[496]	5h
Large Unit size	LARGE_UNIT_SIZE_M1	1	[495]	8GB: 17h 16GB: 2Fh 32GB: 5Fh
Extended partitions attribute support	EXT_SUPPORT	1	[494]	3h
Supported modes	SUPPORTED_MODES	1	[493]	2h
FFU features	FFU_FEATURES	1	[492]	0h

Name	Field	Size (Bytes)	CSD Slice	Value
Operation codes timeout	OPERATION_CODE_TIMEOUT	1	[491]	0h
FFU Argument	FFU_ARG	4	[490:487]	FFFFFFFFh
Barrier support	BARRIER_SUPPORT	1	[486]	1h
Reserved	Reserved	177	[485:309]	-
CMDQ support	CMDQ_SUPPORT	1	[308]	1h
CMDQ depth	CMDQ_DEPTH	1	[307]	1Fh
Reserved	Reserved	1	[306]	-
Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	4	[305:302]	0h
Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT	32	[301:270]	0h
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	[269]	1h
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	[268]	1h
Pre EOL information	PRE_EOL_INFO	1	[267]	1h
Optimal read size	OPTIMAL_READ_SIZE	1	[266]	1h
Optimal write size	OPTIMAL_WRITE_SIZE	1	[265]	8h
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	[264]	1h
Device version	DEVICE_VERSION	2	[263:262]	0h
Firmware version	FIRMWARE_VERSION	8	[261:254]	0h ¹
Power class for 200MHz, DDR at VCC=3.6V	PWR_CL_DDR_200_360	1	[253]	0h
Cache size	CACHE_SIZE	4	[252:249]	1024
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	[248]	32h
Power off notification (long) timeout	POWER_OFF_LONG_TIME	1	[247]	28h
Background operations status	BKOPS_STATUS	1	[246]	0h
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	[245:242]	0h
1 st initialization time after partitioning	NI_TIMEOUT_AP	1	[241]	Ch
Cache Flushing Policy	CACHE_FLUSH_POLICY	1	[240]	1h
Power class for 52MHz, DDR at 3.6V	PWR_CL_DDR_52_360	1	[239]	0h
Power class for 52MHz, DDR at 1.95V	PWR_CL_DDR_52_195	1	[238]	0h
Power class for 200MHz at 3.6V	PWR_CL_200_195	1	[237]	0h
Power class for 200MHz, at 1.95V	PWR_CL_200_130	1	[236]	0h
Minimum Write Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	[235]	0h
Minimum Read Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	[234]	0h
Reserved	-	1	[233]	-

Name	Field	Size (Bytes)	CSD Slice	Value
TRIM Multiplier	TRIM_MULT	1	[232]	8/16GB: 11h 32GB: 22h
Secure Feature support	SEC_FEATURE_SUPPORT	1	[231]	55h
Secure Erase Multiplier	SEC_ERASE_MULT	1	[230]	F7h
Secure TRIM Multiplier	SEC_TRIM_MULT	1	[229]	F7h
Boot information	BOOT_INFO	1	[228]	7h
Reserved	-	1	[227]	-
Boot partition size	BOOT_SIZE_MULT	1	[226]	20h
Access size	ACC_SIZE	1	[225]	8GB: 7h 16GB: 8h 32GB: 9h
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	[224]	1h
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	[223]	8/16GB: 11h 32GB: 22h
Reliable write sector count	REL_WR_SEC_C	1	[222]	1h
High-capacity write protect group size	HC_WP_GRP_SIZE	1	[221]	10h
Sleep current (VCC)	S_C_VCC	1	[220]	8h
Sleep current (VCCQ)	S_C_VCCQ	1	[219]	8h
Production state awareness Timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT	1	[218]	17h
Sleep/awake timeout	S_A_TIMEOUT	1	[217]	15h
Sleep Notification timeout	SLEEP_NOTIFICATION_TIME	1	[216]	10h
Sector Count	SEC_COUNT	4	[215:212]	8GB: 16777216 16GB: 33554432 32GB: 67108864
Security write protect information	SECURE_WP_INFO	1	[211]	1h
Minimum Write Performance for 8bit at 52MHz	MIN_PERF_W_8_52	1	[210]	8h
Minimum Read Performance for 8bit at 52MHz	MIN_PERF_R_8_52	1	[209]	8h
Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	[208]	8h
Minimum Read Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	[207]	8h
Minimum Write Performance for 4bit at 26MHz	MIN_PERF_W_4_26	1	[206]	8h
Minimum Read Performance for 4bit at 26MHz	MIN_PERF_R_4_26	1	[205]	8h
Reserved	-	1	[204]	-
Power class for 26MHz at 3.6V 1R	PWR_CL_26_360	1	[203]	0h
Power class for 52MHz at 3.6V 1R	PWR_CL_52_360	1	[202]	0h
Power class for 26MHz at 1.95V 1R	PWR_CL_26_195	1	[201]	0h
Power class for 52MHz at 1.95V 1R	PWR_CL_52_195	1	[200]	0h
Partition switching timing	PARTITION_SWITCH_TIME	1	[199]	FFh
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	[198]	FFh

Name	Field	Size (Bytes)	CSD Slice	Value
I/O Driver Strength	DRIVER_STRENGTH	1	[197]	1Fh
Device type	DEVICE_TYPE	1	[196]	57h
Reserved	-	1	[195]	-
CSD structure version	CSD_STRUCTURE	1	[194]	2h
Reserved	-	1	[193]	-
Extended CSD revision	EXT_CSD_REV	1	[192]	8h
Command set	CMD_SET	1	[191]	0h
Reserved	-	1	[190]	-
Command set revision	CMD_SET_REV	1	[189]	0h
Reserved	-	1	[188]	-
Power class	POWER_CLASS	1	[187]	0h
Reserved	-	1	[186]	-
High-speed interface timing	HS_TIMING	1	[185]	1h ²
Strobe support	STROBE_SUPPORT	1	[184]	1h
Bus width mode	BUS_WIDTH	1	[183]	2h ³
Reserved	-	1	[182]	-
Erased memory content	ERASED_MEM_CONT	1	[181]	0h
Reserved	-	1	[180]	-
Partition configuration	PARTITION_CONFIG	1	[179]	0h
Boot config protection	BOOT_CONFIG_PROT	1	[178]	0h
Boot bus Conditions	BOOT_BUS_CONDITIONS	1	[177]	0h
Reserved	-	1	[176]	-
High-density erase group definition	ERASE_GROUP_DEF	1	[175]	0h
Boot write protection status registers	BOOT_WP_STATUS	1	[174]	0h
Boot area write protection register	BOOT_WP	1	[173]	0h
Reserved	-	1	[172]	-
User area write protection register	USER_WP	1	[171]	0h
Reserved	-	1	[170]	-
FW configuration	FW_CONFIG	1	[169]	0h
RPMB Size	RPMB_SIZE_MULT	1	[168]	20h
Write reliability setting register	WR_REL_SET	1	[167]	0h
Write reliability parameter register	WR_REL_PARAM	1	[166]	15h
Start Sanitize operation	SANITIZE_START	1	[165]	0h
Manually start background operations	BKOPS_START	1	[164]	0h
Enable background operations handshake	BKOPS_EN	1	[163]	0h

Name	Field	Size (Bytes)	CSD Slice	Value
H/W reset function	RST_n_FUNCTION	1	[162]	0h
HPI management	HPI_MGMT	1	[161]	0h
Partitioning Support	PARTITIONING_SUPPORT	1	[160]	7h
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	[159:157]	8GB: 1024 16GB: 2048 32GB: 4096
Partitions attribute	PARTITIONS_ATTRIBUTE	1	[156]	1h
Partitioning Setting	PARTITION_SETTING_COMPLETED	1	[155]	1h
General Purpose Partition Size	GP_SIZE_MULT4	3	[154:152]	0h
General Purpose Partition Size	GP_SIZE_MULT3	3	[151:149]	0h
General Purpose Partition Size	GP_SIZE_MULT2	3	[148:146]	0h
General Purpose Partition Size	GP_SIZE_MULT1	3	[145:143]	0h
Enhanced User Data Area Size	ENH_SIZE_MULT	3	[142:140]	8GB: 1024 16GB: 2048 32GB: 4096
Enhanced User Data Start Address	ENH_START_ADDR	4	[139:136]	0h
Reserved	-	1	[135]	-
Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	[134]	0h
Production state awareness	PRODUCTION_STATE_AWARENESS	1	[133]	-
Package Case Temperature is controlled	TCASE_SUPPORT	1	[132]	0h
Periodic Wake-up	PERIODIC_WAKEUP	1	[131]	0h
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	1	[130]	1h
Reserved	-	2	[129:128]	-
Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	61	[127:67]	-
Error code	ERROR_CODE	2	[66:65]	0h
Error type	ERROR_TYPE	1	[64]	0h
Native sector size	NATIVE_SECTOR_SIZE	1	[63]	0h
Sector size emulation	USE_NATIVE_SECTOR	1	[62]	0h
Sector size	DATA_SECTOR_SIZE	1	[61]	0h
1 st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	[60]	0h
Class 6 commands control	CLASS_6_CTRL	1	[59]	0h
Number of addressed group to be Released	DYNCAP_NEEDED	1	[58]	0h
Exception events control	EXCEPTION_EVENTS_CTRL	2	[57:56]	0h
Exception events status	EXCEPTION_EVENTS_STATUS	2	[55:54]	0h
Extended Partitions Attribute	EXT_PARTITIONS_ATTRIBUTE	2	[53:52]	0h
Context configuration	CONTEXT_CONF	15	[51:37]	0h

Name	Field	Size (Bytes)	CSD Slice	Value
Packed command status	PACKED_COMMAND_STATUS	1	[36]	0h
Packed command failure index	PACKED_FAILURE_INDEX	1	[35]	0h
Power Off Notification	POWER_OFF_NOTIFICATION	1	[34]	0h
Control to turn the Cache ON/OFF	CACHE_CTRL	1	[33]	0h
Flushing of the cache	FLUSH_CACHE	1	[32]	0h
Barrier control	BARRIER_CTRL	1	[31]	0h
Mode config	MODE_CONFIG	1	[30:30]	0h
Mode operation codes	MODE_OPERATION_CODES	1	[29:29]	0h
Reserved	Reserved	2	[28:27]	-
FFU status	FFU_STATUS	1	[26:26]	0h
Pre loading data size	PRE_LOADING_DATA_SIZE	4	[25:22]	0h
Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	4	[21:18]	8GB: 16777216 16GB: 33554432 32GB: 67108864
Product state awareness enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT	1	[17:17]	1h
Secure removal type	SECURE_REMOVAL_TYPE	1	[16:16]	39h
Command Queue Mode enable	CMQ_MODE_EN	1	[15:15]	0h
Reserved	Reserved	15	[14:0]	-

Notes:

1. Subject to change according to the firmware release note.
2. This field is set to 0 after power-on, hardware reset, or software reset, selecting the backward compatibility interface timing for the device. If the host sets this field to 1, the device switches to high-speed interface timing (refer to Section 10.6.1 of JESD84-B50). If the host sets it to 2, the device switches to HS200 interface timing (refer to Section 10.8.1 of JESD84-B50). If the host sets HS_TIMING [3:0] to 0x3, the device switches to HS400 interface timing (refer to Section 10.10 of JESD84-B50).
3. It is initially set to "0" for a 1-bit data bus configuration and can be modified using a SWITCH command.
4. Reserved bits should read as "0."
5. Obsolete values should be considered "don't care."

8. Package Dimensions

Table 8-1 Package Dimensions

Parameter	Unit	8GB	16GB	32GB
Length	mm	11.5		
Width		13.0		
Height		1.0		
Weight	g ± 5%	0.3		

Top View

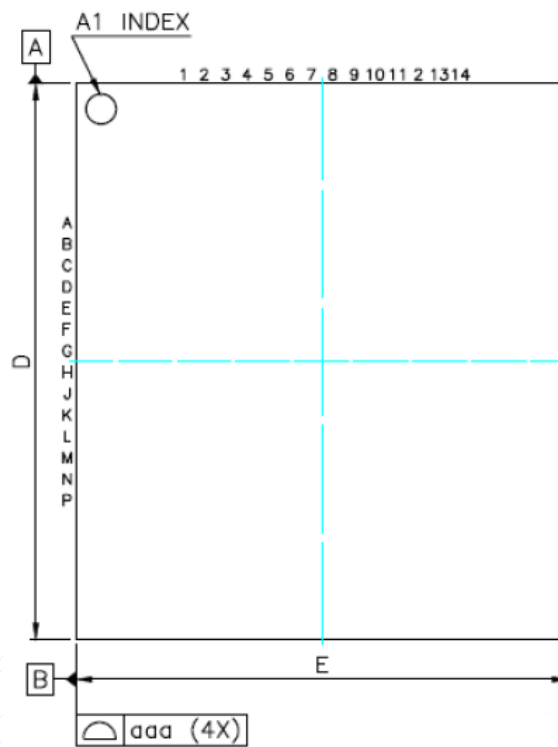


Figure 8-1 Top View

Side View

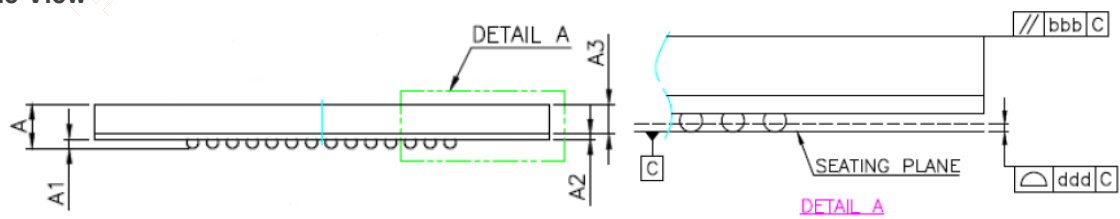


Figure 8-2 Side View

Bottom View

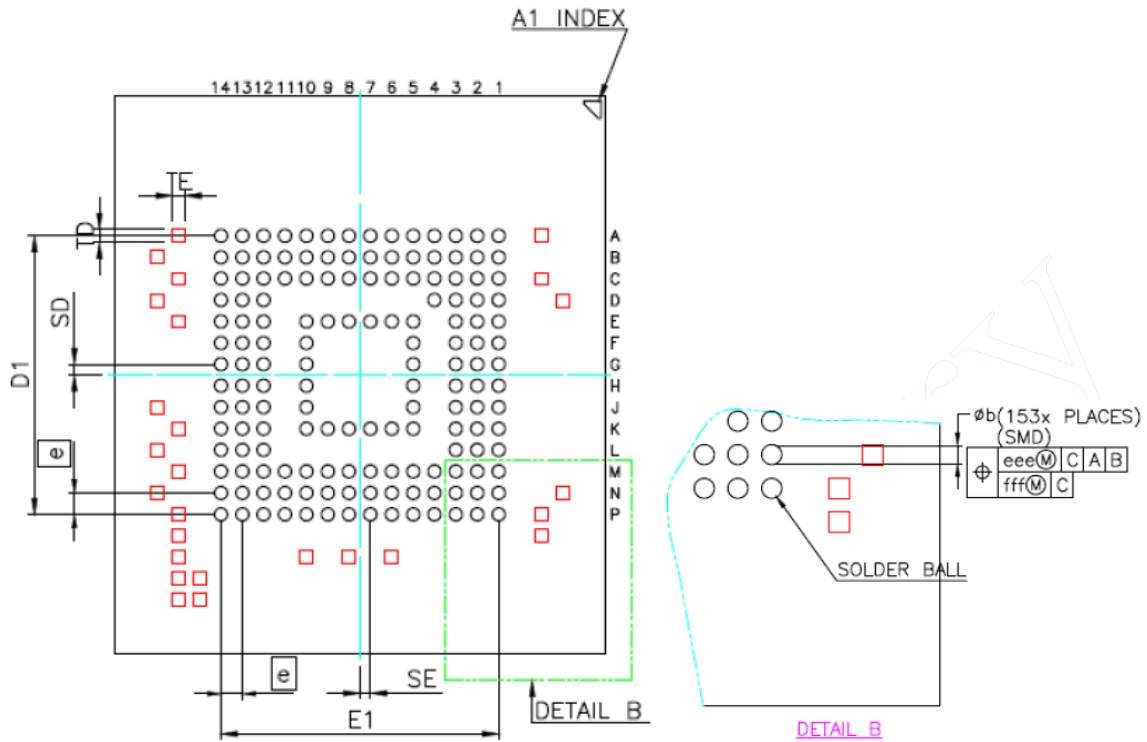


Figure 8-3 Bottom View

	SYM.	DIMENSION (mm)		
		MIN.	NOM.	MAX.
TOTAL THICKNESS	A	0.80	0.95	1.00
STAND OFF	A1	0.17	0.22	0.27
SUBSTRATE THICKNESS	A2	—	0.13	—
MOLD THICKNESS	A3	—	0.60	—
BALL WIDTH	b	0.25	0.30	0.35
BODY SIZE	D	12.90	13.00	13.10
BALL DIAMETER (PRE-REFLOW)		0.30		
BALL OPENING		0.275		
EDGE BALL CENTER TO CENTER	D1	6.50 BSC		
BODY SIZE	E	11.40	11.50	11.60
EDGE BALL CENTER TO CENTER	E1	6.50 BSC		
BODY CENTER TO CONTACT BALL	SD	0.25 BSC		
	SE	0.25 BSC		
MO-276(REF.)		MO-276(REF.)		
BALL PITCH	\square	0.50 BSC		
BALL COUNT	N	153		
TEST PAD	TE	0.25	0.30	0.35
TEST PAD	TD	0.25	0.30	0.35
PACKAGE EDGE TOLERANCE	aaa	0.15		
MOLD FLATNESS	bbb	0.20		
COPLANARITY	ddd	0.08		
BALL OFFSET(PACKAGE)	eee	0.15		
BALL OFFSET(BALL)	fff	0.05		

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER.

9. Product Ordering Information

9.1 Product Code Designations

Apacer EH130 is available in different configurations and densities. See the chart below for a comprehensive list of options for the EH130 series devices.

Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	A	M	6	.	1	3	8	X	M	A	.	0	0	1	0	3

Code 1-3 (Model Name)	EH130															
Code 5-6 (Model/Solution)	Embedded MultiMedia Card															
Code 7-8 (Product Capacity)	8F: 8GB 8G: 16GB 8H: 32GB															
Code 9 (Flash Type & Product Temp)	3D TLC SLC-lite Wide Temperature															
Code 10 (Product Spec)	eMMC															
Code 12-14 (Version Number)	Random numbers generated by system															
Code 15-16 (Firmware Version)	pSLC Wide Temperature															

PRELIMINARY

9.2 Valid Combinations

The following table lists the available models of the Apacer EH130 series which are in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Capacity	Valid Combination
8GB	AM6.138FMA.00103
16GB	AM6.138GMA.00103
32GB	AM6.138HMA.00103

Preliminary

Revision History

Revision	Description	Date
1.0	Initial release	11/20/2023
1.1	Added 3.4.2 Typical Random Performance	2/15/2024

Preliminary

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