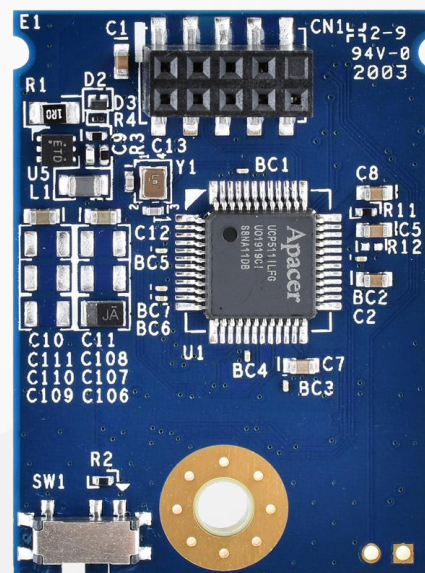


RoHS Recast Compliant

## USB Flash Drive

UV110-UFM2 Product Specifications



November 6, 2020

Version 1.1



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## Specifications Overview:

- **USB2.0 High-Speed and USB1.1 Full-Speed Compatible Interface**
- **Capacity**
  - 16, 32, 64, 128 GB
- **Performance\***
  - Sequential read: Up to 40 MB/sec
  - Sequential write: Up to 33 MB/sec
  - Random read (4K): Up to 1,100 IOPS
  - Random write (4K): Up to 300 IOPS
- **Flash Management**
  - Low-Density Parity-Check (LDPC) Code
  - Flash bad-block management
  - Flash Translation Layer: Page Mapping
  - Global Wear Leveling
  - Power Failure Management
  - S.M.A.R.T.
  - Hyper Cache Technology
  - SMART Read Refresh™
- **Support Non-Removable Setting**
- **NAND Flash Type: 3D TLC (BiCS3)**
- **MTBF: >3,000,000 hours**
- **Endurance (in Terabytes Written: TBW)**
  - 16 GB: 46 TBW
  - 32 GB: 93 TBW
  - 64 GB: 187 TBW
  - 128 GB: 375 TBW
- **Temperature Range**
  - Operating:
    - Standard: 0°C to 70°C
    - Wide: -40°C to 85°C
  - Storage: -55°C to 100°C
- **OS Support**
  - Windows: Win7/Win10 or later
  - Linux: 2.4.10 or later
- **Power Consumption\***
  - Operating voltage: 5V (with a certain percentage of tolerance)
  - Active mode: 110 mA
  - Idle mode: 70 mA
- **Connector**
  - 10-pin (2x5) female header in 2.00 mm
- **Dimensions**
  - 36.8(L) x 26.5(W) x 7.5(H), unit: mm
- **Write Protect Switch (optional)**
- **RoHS Recast Compliant (2011/65/EU)**

\*Varies from capacities. The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings.

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## 1. General Descriptions

Apacer's UV110-UFM2 is a high performance, embedded solid state drive (SSD) designed to replace a conventional IDE hard disk drive. As an embedded flash storage, UV110-UFM2 is compliant with USB2.0 and backward compliant with USB1.1. Utilizing 3D NAND, UV110-UFM2 offers capacity up to 128GB and provides more power efficiency than 2D NAND, and can be plugged into a standard Embedded USB connector commonly found in desktops, portable PC systems and industrial PC systems. Regarding reliability, UV110-UFM2 is implemented with LDPC (Low Density Parity Check) ECC engine to extend SSD endurance and increase data reliability. This product is well suited for embedded flash storage applications offering new and expanded functionality as well as more cost-effective designs, better performance and increased reliability.

## 2. Functional Block

UV110-UFM2 contains a controller, embedded firmware, and Flash Media with a female connector. It interfaces with the host system allowing data to be written to and read from the Flash Media.

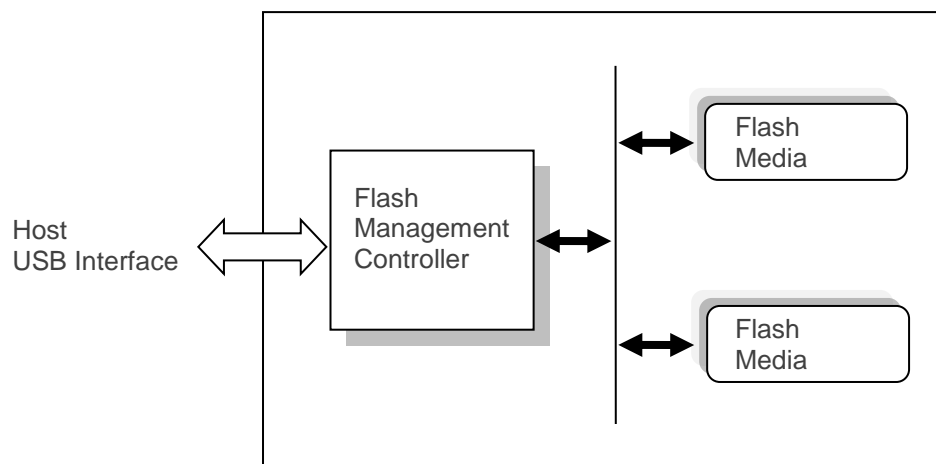
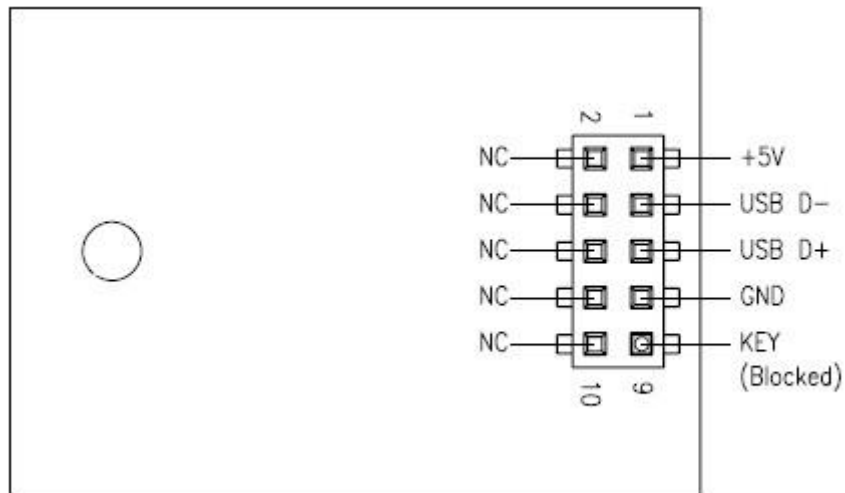


Figure 2-1 Functional Block Diagram

### 3. Pin Assignments

This chapter provides information on the pin assignments and signal descriptions.



**Table 3-1** Pin Assignment of the 10-Pin Configuration

Pin	Signal	Pin	Signal
1	+5V	2	N.C
3	USB D-	4	N.C
5	USB D+	6	N.C
7	GND	8	N.C
9	Key (Blocked)	10	N.C

## 4. Product & Reliability Specifications

### 4.1 Capacity Specifications

UV110-UFM2 is available as shown in Table 4-1.

**Table 4-1** Capacity Specifications

Capacity	Total Bytes	Total LBA
16 GB	15,557,361,664	30,385,472
32 GB	31,039,324,160	60,623,680
64 GB	62,018,519,040	121,129,920
128 GB	123,936,440,320	242,063,360

Note: The number of total bytes may vary depending on the file system in use.

### 4.2 Performance Specifications

Performance of UV110-UFM2 is listed below in Table 4-2.

**Table 4-2** Performance Specifications

Capacity	16 GB	32 GB	64 GB	128 GB
<b>Performance</b>				
<b>Sequential Read* (MB/s)</b>	40	40	40	40
<b>Sequential Write* (MB/s)</b>	17	19	28	33
<b>Random Read IOPS** (4K)</b>	1,100	1,100	1,100	1,100
<b>Random Write IOPS** (4K)</b>	200	200	300	300

Note:

Results may differ from various flash configurations or host system setting, and the above test results are based on the default file structure with FAT 32 file system.

\*Sequential performance is based on CrystalDiskMark 5.2.1 with file size 1,000MB.

\*\*Random performance measured using IOMeter with Queue Depth 32.

### 4.3 Environmental Specifications

Environmental specification of UV110-UFM2 is available as shown in Table 4-3.

**Table 4-3** Environmental Specifications

Item	Specifications	
Temperature	Operation	0°C to 70°C (Standard); -40°C to 85°C (Wide)
	Storage	-55°C to 100°C
Shock	Operating	50(G)/11(ms)/half sine (compliant with MIL-STD-202G)
	Non-operating	1,500(G)/0.5(ms)/half sine (compliant with MIL-STD-202G)
Vibration	Operating	7.69(Grms), 20~2000(Hz)/random (compliant with MIL-STD-810G)
	Non-operating	4.02(Grms), 15~2000(Hz)/random (compliant with MIL-STD-810G)

## 4.4 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in Apacer’s USB flash drive. Serving as statistical reference, the prediction result for Apacer’s UV110-UFM2 is more than 3,000,000 hours.

Note: The MTBF is predicated and calculated based on “Telcordia Technologies Special Report, SR-332, Issue 3” method.

## 4.5 Certification and Compliance

UV110-UFM2 complies with the following standards:

- CE
- FCC
- RoHS Recast
- MIL-STD-810G

## 4.6 Endurance

The endurance of a storage device is predicted by TeraBytes Written based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

**Table 4-4** Endurance Specifications

Capacity	TeraBytes Written
16 GB	46
32 GB	93
64 GB	187
128 GB	375

Note:

- This estimation values are based on sequential write behavior. (Apacer EDTestTool, test mode – sequential data pattern – 100.00% of disk space with 128K)
- Flash vendor guaranteed 3D NAND TLC P/E cycle: 3K
- WAF may vary from capacity, flash configurations and writing behavior on each platform.
- 1 Terabyte = 1,024GB

## 5. Flash Management

### 5.1 Performance-optimized Controller

The heart of UV110-UFM2 is the USB controller, which translates standard USB signals into the data and controls of the flash media. This proprietary USB controller is specifically designed to attain high data throughput from host to flash.

### 5.2 Error Correction/Detection

UV110-UFM2 implements a hardware ECC scheme, based on the Low Density Parity Check (LDPC). LDPC is a class of linear block error correcting code which has apparent coding gain over BCH code because LDPC code includes both hard decoding and soft decoding algorithms. With the error rate decreasing, LDPC can extend SSD endurance and increase data reliability while reading raw data inside a flash chip.

### 5.3 Global Wear Leveling

Flash memory can be erased a limited number of times, This number is called the erase cycle limit, or write endurance limit, The erase cycle limit applies to each individual erase block in the flash device.

In a typical application, and especially if a file system is used, specific pages are constantly updated (e.g., the page that contains the FAT, registry, etc.). Without any special handling, these pages would wear out more rapidly than other pages, reducing the lifetime of the entire flash.

To overcome this inherent deficiency, Apacer's UV110-UFM2 uses Global Wear Leveling algorithm. This algorithm ensures that consecutive writes of a specific sector are not written physically to the same page in the flash. This spreads flash media usage evenly across all pages, thereby maximizing flash lifetime.

The Global Wear Leveling mechanism provides write/erase cycles for reliable data storage over an extended period.

### 5.4 Flash Translation Layer – Page Mapping

Page mapping is an advanced flash management technology whose essence lies in the ability to gather data, distribute the data into flash pages automatically, and then schedule the data to be evenly written. Page-level mapping uses one page as the unit of mapping. The most important characteristic is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different sizes of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. Thus, page mapping is adopted to increase random access speed and improve SSD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

### 5.5 Power Failure Management

Power Failure Management plays a crucial role when power supply becomes unstable. Power disruption may occur when users are storing data into the SSD, leading to instability in the drive. However, with Power Failure Management, a firmware protection mechanism will be activated to scan pages and blocks once power is resumed. Valid data will be transferred to new blocks for merging and the mapping table will be rebuilt. Therefore, data reliability can be reinforced, preventing damage to data stored in the NAND Flash.

## 5.6 S.M.A.R.T.

S.M.A.R.T. is an abbreviation for Self-Monitoring, Analysis and Reporting Technology, a self-monitoring system that provides indicators of drive health as well as potential disk problems. It serves as a warning for users from unscheduled downtime by monitoring and displaying critical drive information. Ideally, this should allow taking proactive actions to prevent drive failure and make use of S.M.A.R.T. information for future product development reference.

## 5.7 Hyper Cache Technology

Apacer proprietary Hyper Cache technology uses a portion of the available capacity as SLC (1bit-per-cell) NAND flash memory, called Hyper cache mode. When data is written to SSD, the firmware will direct the data to Hyper Cache mode, providing excellent performance to handle various scenarios in industrial use.

## 5.8 SMART Read Refresh™

Apacer's SMART Read Refresh plays a proactive role in avoiding read disturb errors from occurring to ensure health status of all blocks of NAND flash. Developed for read-intensive applications in particular, SMART Read Refresh is employed to make sure that during read operations, when the read operation threshold is reached, the data is refreshed by re-writing it to a different block for subsequent use.

## 6. Electrical Specifications

### 6.1 Operating Conditions

Table 6-1 lists the absolute stress rating for UV110-UFM2.

**Caution: Absolute Maximum Stress Ratings** – Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.

**Table 6-1** Operating Range

Range	Ambient Temperature	Voltage
Standard Temperature	0°C to 70°C	4.5-5.5V
Wide Temperature	-40°C to 85°C	

### 6.2 Absolute Maximum Rating

Table 6-2 lists the absolute maximum power ratings for UV110-UFM2.

**Table 6-2** Absolute maximum power pin stress ratings

Parameter	Symbol	Min	Max	Unit
Power Supply Input	VDD- VSS	-0.3	5.5	V
Voltage on any pin except VDD with respect to GND	VIN	-ss - 0.3	VDD +0.3	V

### 6.3 Power Consumption

Table 6-3 lists the power consumption for UV110-UFM2.

**Table 6-3** Power Consumption

Mode	Capacity			
	16 GB	32 GB	64 GB	128 GB
Active (mA)	90	95	110	110
Standby (mA)	70	70	70	70

Note:

\*All values are typical and may vary depending on flash configurations or host system settings.

\*\*Active power is an average power measurement performed using CrystalDiskMark with 128KB sequential read/write transfers.

## 6.4 AC Characteristics

**Table 6-4 AC Characteristics Full Speed**

Parameter	Symbol	Min	Typ	Max	Unit
Rise Time	$T_{FR}$	4	—	20	ns
Fall Time	$T_{FF}$	4	—	20	ns
Differential Rise and Fall Time Matching	$T_{FRFM}$	90		111.11	%
Driver Output Resistance	$Z_{DRV}$	28	—	44	$\Omega$

**Table 6-5 AC Characteristics High Speed**

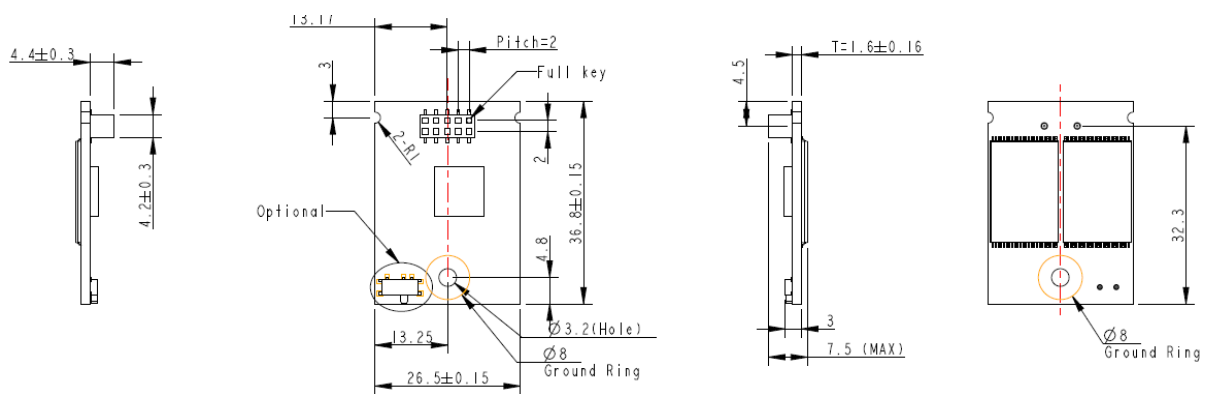
Parameter	Symbol	Min	Typ	Max	Unit
Rise Time (10%~90%)	$T_{HSR}$	500	—	—	ps
Fall Time (10%~90%)	$T_{HSF}$	500	—	—	ps
Driver Output Resistance	$Z_{HSDRV}$	40.5	—	49.5	$\Omega$

## 7. Physical Dimensions

### 7.1 Dimensions

Horizontal Design – Type E (STD 90D-MS)

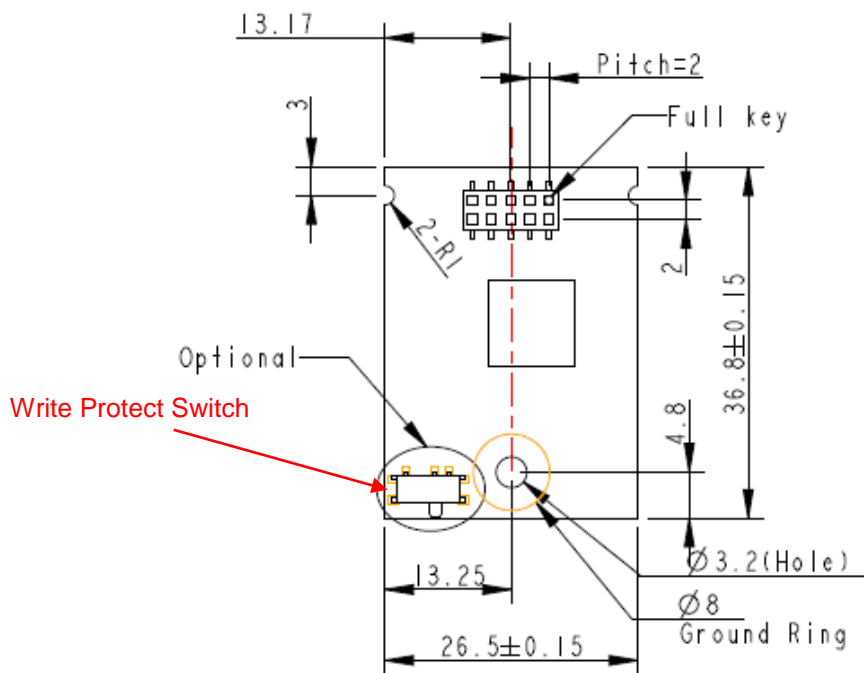
Length	Width	Height (Max)
36.8 mm	26.5 mm	7.5 mm



Unit: mm  
Tolerance:  $\pm 0.2$

## 7.2 Write Protect Switch (optional)

Apacer implements the Virtual Write scheme that allows write commands to go through the flash controller and data temporarily stored, but no data has been actually written into the flash. Once the system is reset and rebooted, the temporarily stored data will be lost and nowhere to be found in the system. Since the Virtual Write scheme runs at device level, it requires no software or driver installation and is independent from the host OS.



## 8. Product Ordering Information

### 8.1 Product Code Designations

Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	A	P	2	.	1	1	2	X	X	X	.	X	X	X	1	5

<b>Code 1-3 (Product Line &amp; form factor)</b>	USB+UFM2
<b>Code 5-6 (Model/Solution)</b>	PS2251-11
<b>Code 7-8 (Product Capacity)</b>	2E: 16GB 2F: 32GB 2G: 64GB 2H: 128GB
<b>Code 9 (Flash Type &amp; Product Temp)</b>	G: TLC standard temperature H: TLC wide temperature
<b>Code 10 (Product Spec)</b>	Q: UV110-UFM2 (LP 90D Type E) without write protect switch R: UV110-UFM2 (LP 90D Type E) with write protect switch
<b>Code 12-14 (Version Number)</b>	Random numbers generated by system
<b>Code 15-16 (Firmware Version)</b>	15: UFPA312A

## 8.2 Valid Combinations

### 8.2.1 Without Write Protect

Capacity	Standard Temperature	Wide Temperature
16GB	AP2.112EGQ.00115	N/A
32GB	AP2.112FGQ.00115	AP2.112FHQ.00115
64GB	AP2.112GGQ.00115	AP2.112GHQ.00115
128GB	AP2.112HGQ.00115	AP2.112HHQ.00115

### 8.2.2 With Write Protect

Capacity	Standard Temperature	Wide Temperature
16GB	AP2.112EGR.00115	NA
32GB	AP2.112FGR.00115	AP2.112FHR.00115
64GB	AP2.112GGR.00115	AP2.112GHR.00115
128GB	AP2.112HGR.00115	AP2.112HHR.00115

**Note:** Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

## Revision History

Revision	Description	Date
1.0	Initial release	8/11/2020
1.1	- Added Power Failure Management to Flash Management on Specifications Overview page - Added 5.5 Power Failure Management	11/6/2020

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