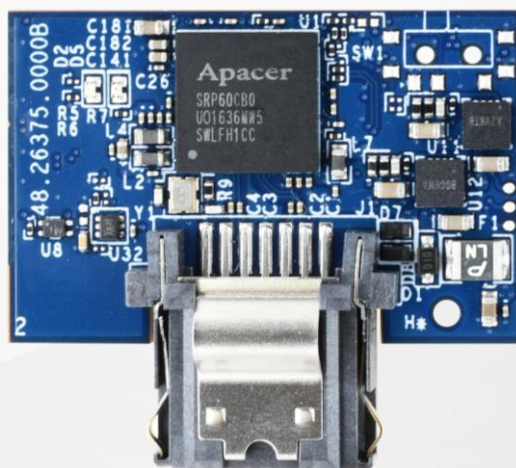


## RoHS Recast Compliant **SATA-Disk Module**

### ST170-7LP2 Product Specifications



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Version 1.3



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## Specifications Overview:

- **Compliance with SATA Interface**
  - Serial ATA Revision 3.1
  - SATA 6.0 Gbps
  - ATA-8 command set
  - Backward compatible with SATA 1.5/3.0 Gbps
- **Capacity**
  - 30, 60, 120 GB
- **Performance\***
  - Burst read/write: 600 MB/sec
  - Sequential read: Up to 335 MB/sec
  - Sequential write: Up to 235 MB/sec
  - Random read (4K): Up to 38,000 IOPS
  - Random write (4K): Up to 55,000 IOPS
- **Flash Management**
  - Low-Density Parity-Check (LDPC) Code
  - Global Wear Leveling
  - Flash bad-block management
  - Flash Translation Layer: Page Mapping
  - S.M.A.R.T.
  - DataDefender™
  - ATA Secure Erase
  - TRIM
  - Hyper Cache Technology
- **DRAM Cache for Enhanced Random Performance**
- **Reliability**
  - Thermal Sensor
  - Thermal Management Technique (optional)
- **Security**
  - End-to-End Data Protection
- **Endurance (in drive writes per day: DWPD)**
  - 30 GB: 1.58 DWPD
  - 60 GB: 1.58 DWPD
  - 120 GB: 1.88 DWPD
- **Temperature Range**
  - Operating: 0°C to 70°C
  - Storage: -40°C to 100°C
- **Supply Voltage**
  - 5.0 V ± 5%
- **Power Consumption\***
  - Active mode: 240 mA
  - Idle mode: 85 mA
- **Connector Type**
  - 7-pin SATA signal connector
  - Power segment options: 2 metal pins on each side of SATA connector or power cable connector
- **Form Factor**
  - SATA Disk Module: 7-pin/180 degree
  - Dimensions: 33.00 x 29.30 x 8.85, unit: mm
- **NAND Flash Type: 3D TLC (BiCS3)**
- **MTBF: >1,000,000 hours**
- **Power Supply Option: Multi-PowerPath Technology**
  - Cable type: +5V VCC from power cable
  - Cable-less type:
    - Pin 7: +5V VCC from the 7th pin
    - 7+2 Pin: +5V VCC from the 2 metal pins on both sides of the SATA connector
- **Shock & Vibration\*\***
  - Shock: 1,500 G
  - Vibration: 15 G
- **LED Indicators for Drive Behavior**
- **RoHS Recast Compliant (Complies with 2011/65/EU Standard)**

\*Varies from capacities. The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings. The term idle refers to the standby state of the device.

\*\*Non-operating

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## 1. General Descriptions

Apacer ST170-7LP2 (SATA Disk Module 7Pin/180 Degree Low Profile 2) is a super-mini industrial SSD module, utilizing 3D NAND for higher capacity up to 120 GB and provides more power efficiency than 2D NAND. Designed in SATA 6.0 Gb/s interface, ST170-7LP2 can deliver outstanding performance up to 335 MB/s in reading and 235 MB/s in writing, highly suitable to serve as operating system boot drive or storage media of important data.

For data efficiency, the internal controlling unit of the product is engineered with a DRAM as a write cache for enhanced random performance and endurance. Besides, ST170-7LP2 features Apacer Multi-PowerPath technology that provides three methods to supply power to the host either via a conventional cable or cable-less design via pin7 or state-of-art 7+2 pin connector, which in turn offers developers maximum flexibility when it comes to board design.

Moreover, the device adopts the latest page mapping file translation layer and thermal throttling function, making it a powerful yet compact solution for space-limited design. Regarding reliability, ST170-7LP2 is implemented with LDPC (Low Density Parity Check) ECC engine to extend SSD endurance and increase data reliability while reading raw data inside a flash chip.

## 2. Functional Block

Apacer ST170-7LP2 includes a single-chip SATA 6.0 Gbps and the flash media. The controller integrates the flash management unit to support multi-channel, multi-bank flash arrays. Figure 2-1 shows the functional block diagram.

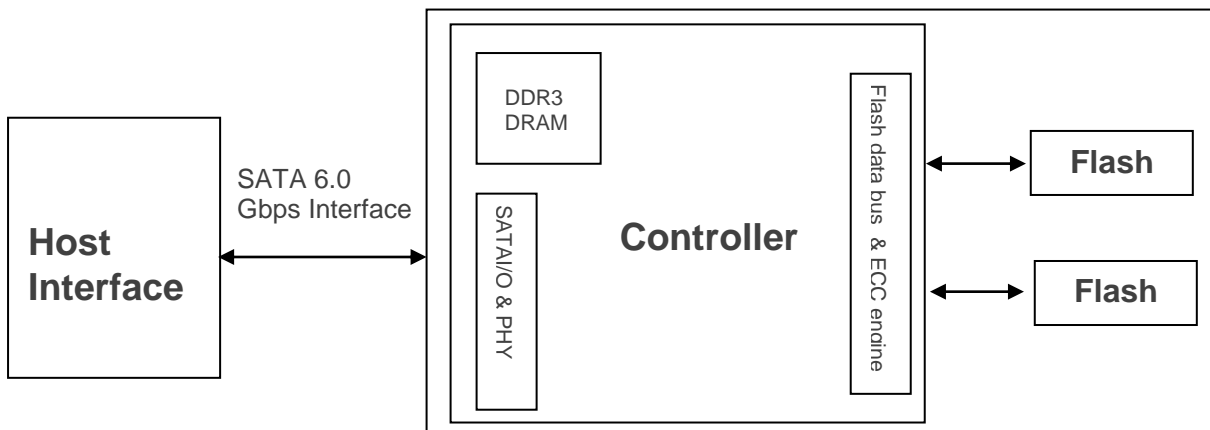


Figure 2-1 Block Diagram

### 3. Pin Assignments

#### 3.1 Multi-PowerPath Technology

Apacer’s patented Multi-PowerPath technology provides a three-option plug-and-play solution for power supply. In addition to using a conventional power cable, power can also be supplied through state-of-art 7+2 pin connector on the side with cable-less design, allowing an SSD to operate without external power supply, giving it the dual advantages of signal integrity and flexible configuration on the motherboard. With the exclusive, innovative power circuit mechanism, Multi-PowerPath protects miniature SSD from being damaged by overheating even when power is concurrently supplied via the three methods.

#### 3.2 Cable Type

+5V VCC from Power Cable

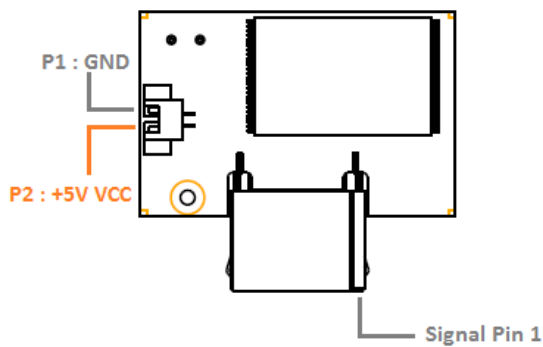


Table 3-1 Signal Segment

| Pin | Type | Description                |
|-----|------|----------------------------|
| 1   | GND  | Ground                     |
| 2   | A+   | Differential Signal Pair A |
| 3   | A-   |                            |
| 4   | GND  | Ground                     |
| 5   | B-   | Differential Signal Pair B |
| 6   | B+   |                            |
| 7   | GND  | Ground                     |

Table 3-2 Power Segment

| Pin | Type | Description |
|-----|------|-------------|
| P1  | GND  | Ground      |
| P2  | VCC  | +5V VCC     |

### 3.3 Cable-Less Type

Pin 7: +5V VCC from the 7th pin

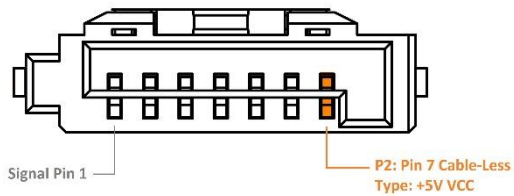


Table 3-3 Signal/Power Segment (Pin 7 Cable-less)

| Pin | Type | Description                |
|-----|------|----------------------------|
| 1   | GND  | Ground                     |
| 2   | A+   | Differential Signal Pair A |
| 3   | A-   |                            |
| 4   | GND  | Ground                     |
| S5  | B-   | Differential Signal Pair B |
| S6  | B+   |                            |
| P2  | VCC  | +5V VCC                    |

7+2 Pin: +5V VCC from the 2 metal pins on both sides of the SATA connector

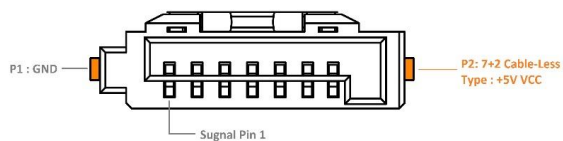


Table 3-4 Signal Segment

| Pin | Type | Description                |
|-----|------|----------------------------|
| 1   | GND  | Ground                     |
| 2   | A+   | Differential Signal Pair A |
| 3   | A-   |                            |
| 4   | GND  | Ground                     |
| 5   | B-   | Differential Signal Pair B |
| 6   | B+   |                            |
| 7   | GND  | Ground                     |

Table 3-5 Power Segment (7+2 Cable-less)

| Pin | Type | Description |
|-----|------|-------------|
| P1  | GND  | Ground      |
| P2  | VCC  | +5V VCC     |

## 4. Product Specifications

### 4.1 Capacity

Capacity specifications of ST170-7LP2 are available as shown in Table 4-1. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

**Table 4-1** Capacity Specifications

| Capacity | Total bytes*    | Cylinders | Heads | Sectors | Max LBA     |
|----------|-----------------|-----------|-------|---------|-------------|
| 30 GB    | 30,016,536,576  | 16,383    | 16    | 63      | 58,626,288  |
| 60 GB    | 60,021,538,816  | 16,383    | 16    | 63      | 117,231,408 |
| 120 GB   | 120,033,640,448 | 16,383    | 16    | 63      | 234,441,648 |

\*Display of total bytes varies from file systems, which means not all of the bytes can be used for storage.

\*\*Notes: 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.

LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

### 4.2 Performance

Performance of ST170-7LP2 is listed below in Table 4-2.

**Table 4-2** Performance Specifications

| Capacity                        | 30 GB  | 60 GB  | 120 GB |
|---------------------------------|--------|--------|--------|
| Performance                     |        |        |        |
| <b>Sequential Read* (MB/s)</b>  | 295    | 335    | 335    |
| <b>Sequential Write* (MB/s)</b> | 130    | 235    | 235    |
| <b>Random Read IOPS** (4K)</b>  | 20,000 | 34,000 | 38,000 |
| <b>Random Write IOPS** (4K)</b> | 30,000 | 55,000 | 55,000 |

Note:

Results may differ from various flash configurations or host system setting.

\*Sequential performance is based on CrystalDiskMark 5.2.1 with file size 1,000MB.

\*\*Random performance measured using IOMeter with Queue Depth 32.

### 4.3 Environmental Specifications

Environmental specifications of ST170-7LP2 product are shown in Table 4-3.

**Table 4-3** Environmental Specifications

| Item                    | Specifications   |
|-------------------------|--|
| Operating temp.         | 0°C to 70°C  |
| Non-operating temp.     | -40°C to 100°C   |
| Operating vibration     | 7.69 GRMS, 20~2000 Hz/random (compliant with MIL-STD-810G) |
| Non-operating vibration | 4.02 GRMS, 15~2000 Hz/random (compliant with MIL-STD-810G) |
| Operating shock         | 50G, 11ms  |
| Non-operating shock     | 1500G, 0.5ms (compliant with MIL-STD-883K)                 |

Note: This Environmental Specification table indicates the conditions for testing the device. Real world usages may affect the results.

## 4.4 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in ST170-7LP2. The prediction result for ST170-7LP2 is more than 1,000,000 hours. Note: The MTBF is predicated and calculated based on “Telcordia Technologies Special Report, SR-332, Issue 2” method.

## 4.5 Certification and Compliance

ST170-7LP2 complies with the following standards:

- CE
- FCC
- RoHS Recast
- MIL-STD-810

## 4.6 Endurance

The endurance of a storage device is predicted by Drive Writes Per Day based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

**Table 4-4** Drive Writes Per Day

| Capacity | Drive Writes Per Day |
|----------|----------------------|
| 30 GB    | 1.58                 |
| 60 GB    | 1.58                 |
| 120 GB   | 1.88                 |

Note:

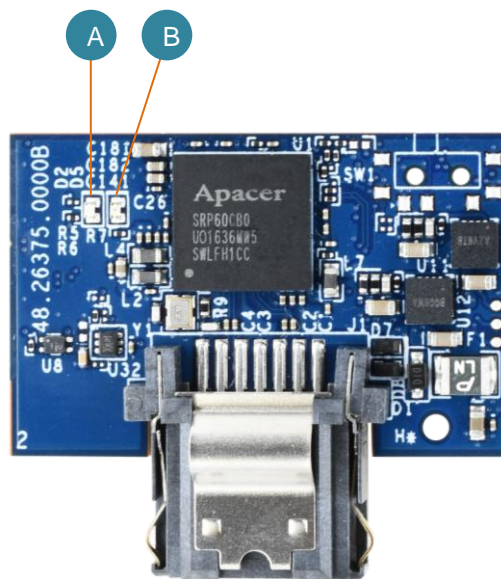
- This estimation complies with JEDEC random client workload.
- Flash vendor guaranteed 3D NAND TLC P/E cycle: 3K
- WAF may vary from capacity, flash configurations and writing behavior on each platform.
- 1 Terabyte = 1,024GB
- DWPD (Drive Writes Per Day) is calculated the number of times that user can overwrite the entire capacity of an SSD per day of its lifetime during the warranty period. (3D NAND TLC warranty: 2 years)

## 4.7 LED Indicator Behavior

The behavior of the ST170-7LP2 LED indicators is described in Table 4-5.

**Table 4-5** LED Behavior

| Location | LED   | Description                                 |
|----------|-------|---|
| LED A    | DAS   | LED blinks when the drive is being accessed |
| LED B    | Power | LED glows solidly when power is on          |



## 5. Flash Management

### 5.1 Error Correction/Detection

ST170-7LP2 implements a hardware ECC scheme, based on the Low Density Parity Check (LDPC). LDPC is a class of linear block error correcting code which has apparent coding gain over BCH code because LDPC code includes both hard decoding and soft decoding algorithms. With the error rate decreasing, LDPC can extend SSD endurance and increase data reliability while reading raw data inside a flash chip.

### 5.2 Bad Block Management

Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. When host performs program/erase command on a block, bad block may appear in Status Register. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, page mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

### 5.3 Global Wear Leveling

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Global wear leveling is an important mechanism that levels out the wearing of all blocks so that the wearing-down of all blocks can be almost evenly distributed. This will increase the lifespan of SSDs.

### 5.4 DataDefender™

Apacer DataDefender™ combines both firmware and hardware mechanisms to ensure data integrity. When power disruption occurs, the hardware mechanism will notice and trigger the controller to run multiple write-to-flash cycles to store data. Then the firmware will check that the data was correctly written to the NAND flash after the power disruption, preventing data loss.

Note: The controller unit of this product model is designed with a DRAM as a write cache for improved performance and data efficiency. Though unlikely to happen in most cases, the data cached in the volatile DRAM might be potentially affected if a sudden power loss takes place before the cached data is flushed into non-volatile NAND flash memory.

### 5.5 ATA Secure Erase

ATA Secure Erase is an ATA disk purging command currently embedded in most of the storage drives. Defined in ATA specifications, (ATA) Secure Erase is part of Security Feature Set that allows storage drives to erase all user data areas. The erase process usually runs on the firmware level as most of the ATA-based storage media currently in the market are built-in with this command. ATA Secure Erase can securely wipe out the user data in the drive and protects it from malicious attack.

## 5.6 TRIM

TRIM is a SATA command that helps improve the read/write performance and efficiency of solid-state drives (SSD). The command enables the host operating system to inform SSD controller which blocks contain invalid data, mostly because of the erase commands from host. The invalid will be discarded permanently and the SSD will retain more space for itself.

## 5.7 Flash Translation Layer – Page Mapping

Page mapping is an advanced flash management technology whose essence lies in the ability to gather data, distribute the data into flash pages automatically, and then schedule the data to be evenly written. Page-level mapping uses one page as the unit of mapping. The most important characteristic is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different sizes of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. Thus, page mapping is adopted to increase random access speed and improve SSD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

## 5.8 Hyper Cache Technology

Apacer proprietary Hyper Cache technology uses a portion of the available capacity as SLC (1bit-per-cell) NAND flash memory, called Hyper cache mode. When data is written to SSD, the firmware will direct the data to Hyper Cache mode, providing excellent performance to handle various scenarios in industrial use.

## 5.9 SATA Power Management

By complying with SATA 6.0 Gb/s specifications, the SSD supports the following SATA power saving modes:

- ACTIVE: PHY ready, full power, Tx & Rx operational
- PARTIAL: Reduces power, resumes in under 10  $\mu$ s (microseconds)
- SLUMBER: Reduces power, resumes in under 10 ms (milliseconds)
- HIPM: Host-Initiated Power Management
- DIPM: Device-Initiated Power Management
- AUTO-SLUMBER: Automatic transition from partial to slumber.

Note: The behaviors of power management features would depend on host/device settings.

## 6. Security & Reliability Features

### 6.1 Thermal Sensor

Apacer Thermal Sensor is a digital temperature sensor with serial interface. By using designated pins for transmission, storage device owners are able to read temperature data.

### 6.2 Thermal Management Technique (optional)

Thermal management technique can monitor the temperature of the SSD equipped with a built-in thermal sensor via S.M.A.R.T. commands. This method can ensure the temperature of the device stays within temperature limits by drive throttling, i.e. reducing the speed of the drive when the device temperature reaches the threshold level, so as to prevent overheating, guarantee data reliability, and prolong product lifespan. When the temperature exceeds the maximum threshold level, thermal throttling will be triggered to reduce performance step by step to prevent hardware components from being damaged. Performance is only permitted to drop to the extent necessary for recovering a stable temperature to cool down the device's temperature. Once the temperature decreases to the minimum threshold value, transfer speeds will rise back to its optimum performance level.

### 6.3 End-to-End Data Protection

End-to-End Data Protection is a feature implemented in Apacer SSD products that extends error control to cover the entire path from the host computer to the drive and back, and ensure data integrity at multiple points in the path to enable reliable delivery of data transfers. Unlike ECC which does not exhibit the ability to determine the occurrence of errors throughout the process of data transmission, End-to-End Data Protection allows SSD controller to identify an error created anywhere in the path and report the error to the host computer before it is written to the drive. This error-checking and error-reporting mechanism therefore guarantees the trustworthiness and reliability of the SSD.

## 7. Software Interface

### 7.1 Command Set

This section defines the software requirements and the format of the commands the host sends to ST170-7LP2. Commands are issued to ST170-7LP2 by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command register.

Table 7-1 Command Set

| Code    | Command                           | Code | Command                 |                                |  |
|---------|-----------------------------------|------|-------------------------|--------------------------------|--|
| 00h     | NOP                               | C9h  | Read DMA without Retrv  |                                |  |
| 06h     | Data Set Management               | CAh  | Write DMA               |                                |  |
| 10h-1Fh | Recalibrate                       | CBh  | Write DMA without Retry |                                |  |
| 20h     | Read Sectors                      | CEh  | Write Multiple FUA EXT  |                                |  |
| 21      | Read Sectors without Retrv        | E0h  | Standby Immediate       |                                |  |
| 24h     | Read Sectors EXT                  | E1h  | Idle Immediate          |                                |  |
| 25h     | Read DMA EXT                      | E2h  | Standby                 |                                |  |
| 27h     | Read Native Max Address EXT       | E3h  | Idle                    |                                |  |
| 29h     | Read Multiple EXT                 | E4h  | Read Buffer             |                                |  |
| 2Fh     | Read Log EXT                      | E5h  | Check Power Mode        |                                |  |
| 30h     | Write Sectors                     | E6h  | Sleep                   |                                |  |
| 31h     | Write Sectors without Retrv       | E7h  | Flush Cache             |                                |  |
| 34h     | Write Sectors EXT                 | E8h  | Write Buffer            |                                |  |
| 35h     | Write DMA EXT                     | E9h  | READ BUFFER DMA         |                                |  |
| 37h     | Set Native Max Address EXT        | EAh  | Flush Cache EXT         |                                |  |
| 38h     | CFA Write Sectors without Erase   | EBh  | Write Buffer DMA        |                                |  |
| 39h     | Write Multiple EXT                | EC   | Identify Device         |                                |  |
| 3Dh     | Write DMA FUA EXT                 | EFh  | Set Features            |                                |  |
| 3Fh     | Write Long EXT                    | EFh  | 02h                     | Enable volatile write cache    |  |
| 40h     | Read Verify Sectors               | EFh  | 03h                     | Set transfer mode              |  |
| 41h     | Read Verify Sectors without Retrv | EFh  | 05h                     | Enable the APM feature set     |  |
| 42h     | Read Verify Sectors EXT           | EFh  | 10h                     | Enable use of SATA feature set |  |
| 44h     | Zero EXT                          | EFh  | 10h                     | 02h                            | Enable DMA Setup FIS Auto-Activate optimization                  |
| 45h     | Write Uncorrectable EXT           | EFh  | 10h                     | 03h                            | Enable Device-initiated interface power state (DIPM) transitions |
| 47h     | Read Log DMA EXT                  | EFh  | 10h                     | 06h                            | Enable Software Settings Preservation (SSP)                      |
| 57h     | Write Log DMA EXT                 | EFh  | 10h                     | 07h                            | Enable Device Automatic Partial to Slumber transitions           |
| 60h     | Read FPDMA Queued                 | EFh  | 10h                     | 09h                            | Enable Device Sleep  |

| Code    |     | Command                                 | Code |     | Command                                |   |
|---------|-----|---|------|-----|--|---|
| 61h     |     | Write FPDMA Queued                      | EFh  | 55h | Disable read look-ahead                |   |
| 70h-7Fh |     | Seek                                    | EFh  | 66h | Disable reverting to power-on defaults |   |
| 90h     |     | Execute Device Diagnostic               | EFh  | 82h | Disable volatile write cache           |   |
| 91h     |     | Initialize Device Parameters            | EFh  | 85h | Disable the APM feature set            |   |
| 92h     |     | Download Microcode                      | EFh  | 90h | Disable use of SATA feature set        |   |
| 93h     |     | Download Microcode DMA                  | EFh  | 90h | 02h                                    | Disable DMA Setup FIS Auto-Activate optimization                  |
| B0h     |     | SMART                                   | EFh  | 90h | 03h                                    | Disable Device-initiated interface power state (DIPM) transitions |
| B0h     | D0h | SMART READ DATA                         | EFh  | 90h | 06h                                    | Disable Software Settings Preservation (SSP)                      |
| B0h     | D1h | SMART READ ATTRIBUTE THRESHOLDS         | EFh  | 90h | 07h                                    | Disable Device Automatic Partial to Slumber transitions           |
| B0h     | D2h | SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE | EFh  | 90h | 09h                                    | Disable Device Sleep  |
| B0h     | D3h | SMART SAVE ATTRIBUTE VALUES             | EFh  | AAh |  | Enable read look-ahead  |
| B0h     | D4h | SMART EXECUTE OFF-LINE IMMEDIATE        | EFh  | CCh |  | Enable reverting to power-on defaults                             |
| B0h     | D5h | SMART READ LOG                          | F1h  |     |  | Security Set Password   |
| B0h     | D6h | SMART WRITE LOG                         | F2h  |     |  | Security Unlock   |
| B0h     | D8h | SMART ENABLE OPERATIONS                 | F3h  |     |  | Security Erase Prepare  |
| B0h     | D9h | SMART DISABLE OPERATIONS                | F4h  |     |  | Security Erase Unit   |
| B0h     | DAh | SMART RETURN STATUS                     | F5h  |     |  | Security Freeze Lock  |
| B0h     | DBh | SMART ENABLE/DISABLE AUTOMATIC OFF-LINE | F6h  |     |  | Security Disable Password   |
| B1h     |     | Device Configuration                    | F8h  |     |  | Read Native Max Address   |
| B4h     |     | Sanitize                                | F9h  |     |  | Set Max Address   |
| C4h     |     | Read Multiple                           | F9h  | 01h |  | SET MAX SET PASSWORD  |
| C5h     |     | Write Multiple                          | F9h  | 02h |  | SET MAXLOCK   |
| C6h     |     | Set Multiple Mode                       | F9h  | 03h |  | SET MAX UNLOCK  |
| C8h     |     | Read DMA                                | F9h  | 04h |  | SET MAX FREEZE LOCK   |

## 7.2 S.M.A.R.T.

S.M.A.R.T. is an abbreviation for Self-Monitoring, Analysis and Reporting Technology, a self-monitoring system that provides indicators of drive health as well as potential disk problems. It serves as a warning for users from unscheduled downtime by monitoring and displaying critical drive information. Ideally, this should allow taking proactive actions to prevent drive failure and make use of S.M.A.R.T. information for future product development reference.

Apacer devices use the standard SMART command B0h to read data out from the drive to activate our S.M.A.R.T. feature that complies with the ATA/ATAPI specifications. S.M.A.R.T. Attribute IDs shall include initial bad block count, total later bad block count, maximum erase count, average erase count, power on hours and power cycle. When the S.M.A.R.T. Utility running on the host, it analyzes and reports the disk status to the host before the device reaches in critical condition.

Note: Attribute IDs may vary from product models due to various solution design and supporting capabilities.

Apacer memory products come with S.M.A.R.T. commands and subcommands for users to obtain information of drive status and to predict potential drive failures. Users can take advantage of the following commands/subcommands to monitor the health of the drive.

| Code | SMART Subcommand                  |
|------|-----------------------------------|
| D0h  | READ DATA                         |
| D1h  | READ ATTRIBUTE THRESHOLDS         |
| D2h  | Enable/Disable Attribute Autosave |
| D4h  | Execute Off-line Immediate        |
| D5h  | Read Log (optional)               |
| D6h  | Write Log (optional)              |
| D8h  | Enable Operations                 |
| D9h  | Disable operations                |
| DAh  | Return Status                     |

**General SMART attribute structure**

| Byte  | Description |
|-------|-------------|
| 0     | ID (Hex)    |
| 1 – 2 | Status flag |
| 3     | Value       |
| 4     | Worst       |
| 5*-11 | Raw Data    |

\*Byte 5: LSB

SMART attribute ID list

| ID (Hex)   | Attribute Name                     |
|------------|------------------------------------|
| 9 (0x09)   | Power-on hours                     |
| 12 (0x0C)  | Power cycle count                  |
| 163 (0xA3) | Max. erase count                   |
| 164 (0xA4) | Avg. erase count                   |
| 166 (0xA6) | Total later bad block count        |
| 167 (0xA7) | SSD Protect Mode (vendor specific) |
| 168 (0xA8) | SATA PHY Error Count               |
| 171 (0xAB) | Program fail count                 |
| 172 (0xAC) | Erase fail count                   |
| 175 (0xAF) | Bad Cluster Table Count            |
| 192 (0xC0) | Unexpected Power Loss Count        |
| 194 (0xC2) | Temperature                        |
| 231 (0xE7) | Lifetime left                      |
| 241 (0xF1) | Total sectors of write             |

## 8. Electrical Specifications

### 8.1 Operating Voltage

Table 8-1 lists the supply voltage for ST170-7LP2.

**Caution: Absolute Maximum Stress Ratings** – Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.

**Table 8-1** Operating Range

| Item           | Range                |
|----------------|----------------------|
| Supply Voltage | 5V ± 5% (4.75-5.25V) |

### 8.2 Power Consumption

Table 8-2 lists the power consumption for ST170-7LP2.

**Table 8-2** Power Consumption

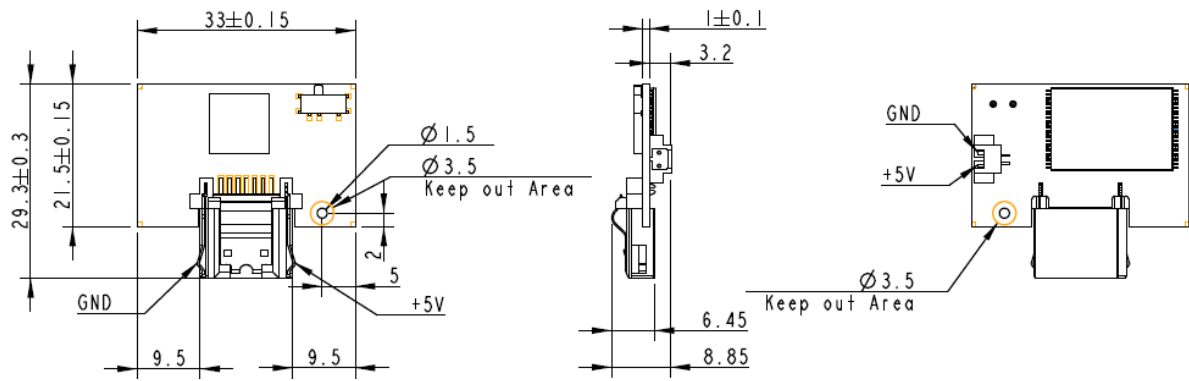
| Mode \ Capacity | Capacity |       |        |
|-----------------|----------|-------|--------|
|                 | 30 GB    | 60 GB | 120 GB |
| Active (mA)     | 230      | 240   | 240    |
| Idle (mA)       | 85       | 80    | 80     |

Note:

\*All values are typical and may vary depending on flash configurations or host system settings.

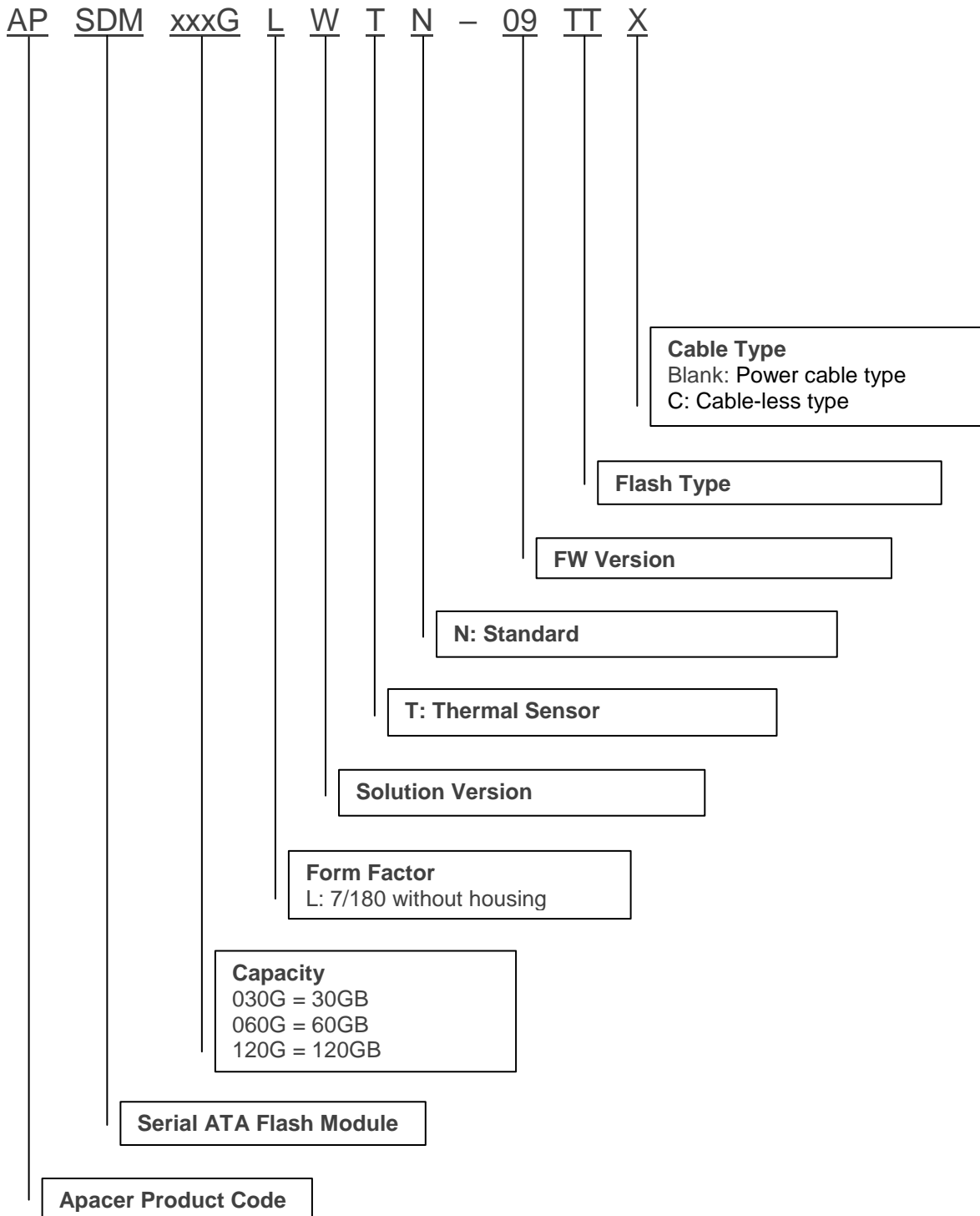
\*\*Active power is an average power measurement performed using CrystalDiskMark with 128KB sequential read/write transfers.

## 9. Physical Characteristics



## 10. Product Ordering Information

### 10.1 Product Code Designations



## 10.2 Valid Combinations

### 10.2.1 Multi-Power Path: Power Cable Type

| Capacity | Part Number        |
|----------|--------------------|
| 30GB     | APSDM030GLWTN-09TT |
| 60GB     | APSDM060GLWTN-09TT |
| 120GB    | APSDM120GLWTN-09TT |

### 10.2.2 Multi-Power Path: Cable-less Type

| Capacity | Part Number         |
|----------|---------------------|
| 30GB     | APSDM030GLWTN-09TTC |
| 60GB     | APSDM060GLWTN-09TTC |
| 120GB    | APSDM120GLWTN-09TTC |

**Note:** Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

## Revision History

| Revision | Date       | Description   | Remark |
|----------|------------|---|--------|
| 0.1      | 8/8/2018   | Preliminary release   |        |
| 1.0      | 8/20/2018  | <ul style="list-style-type: none"> <li>- Updated Endurance on Specifications Overview page and 4.6 Endurance</li> <li>- Removed Write Protect support</li> <li>- Removed cable-less type (pin 7) support</li> <li>- Updated 10. Product Ordering Information</li> </ul>                     |        |
| 1.1      | 8/22/2018  | <ul style="list-style-type: none"> <li>- Updated cable-less type at Power Supply Option on Specifications Overview page</li> <li>- Updated the illustration at 3.2 Power Cable Type and 3.3 Cable-Less Type and revised Table 3-5 Signal/Power Segment</li> </ul>                           |        |
| 1.2      | 11/6/2018  | <ul style="list-style-type: none"> <li>- Revised supply voltage from 3.3V to 5V</li> <li>- Removed the last sentence about the support of CoreAnalyzer from 1. General Descriptions</li> </ul>  |        |
| 1.3      | 11/21/2018 | <ul style="list-style-type: none"> <li>- Remove the redundant asterisk mark from note 2 at 4.6 Endurance</li> <li>- Renamed Power Failure Management to DataDefender™ at Flash Management on Specifications Overview page and 5.4 section and updated the technology description</li> </ul> |        |

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