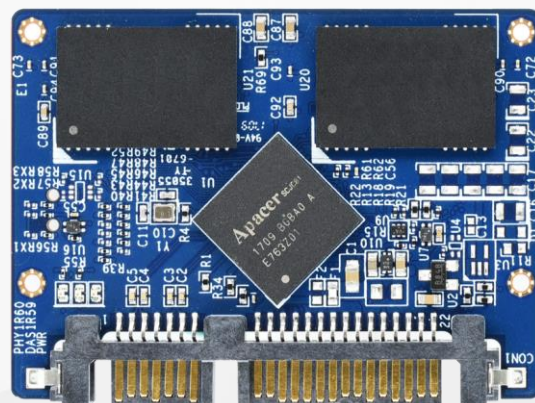


RoHS Compliant

## Serial ATA Flash Drive

SM230-297 Product Specifications

(Toshiba 15nm)



July 22, 2020

Version 1.9



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## Specifications Overview:

- **Compliance with SATA Revision 3.2**
  - SATA 6 Gb/s interface
  - Backward compatible with SATA 1.5 and 3 Gb/s interfaces
  - ATA-8 command set
- **Capacity**
  - 32, 64, 128, 256, 512 GB
- **Performance\***
  - Burst read/write: 600 MB/sec

**Standard:**

  - Sequential read: up to 560 MB/sec
  - Sequential write: up to 495 MB/sec
  - Random read 4K: up to 41,000 IOPS
  - Random write 4K: up to 60,000 IOPS

**AES & Opal Implemented:**

  - Sequential read: up to 560 MB/sec
  - Sequential write: up to 500 MB/sec
  - Random read 4K: up to 39,000 IOPS
  - Random write 4K: up to 60,000 IOPS
- **Flash Management**
  - Built-in hardware ECC
  - Global Wear Leveling
  - Flash bad-block management
  - Flash Translation Layer: Page Mapping
  - S.M.A.R.T.
  - Power Failure Management
  - Device Sleep
  - ATA Secure Erase
  - TRIM
  - Hyper Cache Technology
  - SMART Read Refresh™
- **NAND Flash Type:** MLC
- **MTBF:** >1,000,000 hours
- **Temperature Range**
  - Operating:
    - Standard: 0°C to 70°C
    - Wide: -40°C to 85°C
  - Storage: -40°C to 100°C
- **Supply Voltage**
  - 5.0 V ± 5%
- **Power Consumption\***
  - Active mode: 645 mA
  - Idle mode: 110 mA
- **Form Factor**
  - JEDEC MO-297
  - Dimensions: 54.00 x 39.80 x 4.00, unit: mm
- **Shock & Vibration\*\***
  - Shock: 1,500 G
  - Vibration: 15 G
- **SATA Power Management Modes**
- **Security (optional)**
  - Trusted Computing Group (TCG) Opal 2.0
  - AES 256-bit hardware encryption
- **Reliability**
  - Thermal Sensor\*\*\*
- **Endurance (in Terabytes Written: TBW)**
  - 32 GB: 42 TBW
  - 64 GB: 77 TBW
  - 128 GB: 136 TBW
  - 256 GB: 197 TBW
  - 512 GB: 208 TBW
- **Write Protect Switch (optional)**
- **RoHS Compliant**

\*Varies from capacities. The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings.

\*\*Non-operating

\*\*\*Built-in feature for wide temperature products; optional feature for standard temperature products.

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# 1. Product Descriptions

## 1.1 Introduction

Apacer SM230-297 is a well-balanced solid-state disk (SSD) drive with compact form factor (JEDEC MO-297) and great performance. Designed in SATA 6 Gb/s interface, the mSATA SSD is able to deliver exceptional read/write speed, making it the ideal companion for heavy-loading embedded or server operations with space constraints for host computing systems. In regard of reliability, the drive comes with various implementations including powerful hardware ECC engine, power saving modes, wear leveling, flash block management, S.M.A.R.T., TRIM, and power failure management.

## 1.2 Capacity

Capacity specifications of SM230-297 are available as shown in Table 1-1. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

**Table 1-1** Capacity Specifications

Capacity	Total bytes*	Cylinders	Heads	Sectors	Total LBA
32 GB	32,017,047,552	16,383	16	63	62,533,296
64 GB	64,023,257,088	16,383	16	63	125,045,424
128 GB	128,035,676,160	16,383	16	63	250,069,680
256 GB	256,060,514,304	16,383	16	63	500,118,192
512 GB	512,110,190,592	16,383	16	63	1,000,215,216

\*Display of total bytes varies from file systems, which means not all of the bytes can be used for storage.

\*\*Notes: 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.

LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

## 1.3 Performance

Performance of SM230-297 is listed below in Table 1-2 and 1-3.

**Table 1-2** Performance Specifications (Standard)

Capacity	32 GB	64 GB	128 GB	256 GB	512 GB
<b>Performance</b>					
<b>Sequential Read* (MB/s)</b>	490	475	470	465	560
<b>Sequential Write* (MB/s)</b>	155	455	445	485	495
<b>Random Read IOPS** (4K)</b>	24,000	37,000	38,000	41,000	39,000
<b>Random Write IOPS** (4K)</b>	16,000	30,000	38,000	57,000	60,000

**Table 1-3 Performance Specifications (AES and Opal implemented)**

Capacity	32 GB	64 GB	128 GB	256 GB	512 GB
<b>Performance</b>					
<b>Sequential Read* (MB/s)</b>	560	560	560	560	560
<b>Sequential Write* (MB/s)</b>	265	480	445	500	495
<b>Random Read IOPS** (4K)</b>	23,000	36,000	37,000	39,000	39,000
<b>Random Write IOPS** (4K)</b>	16,000	30,000	38,000	58,000	60,000

Note:

Results may differ from various flash configurations or host system setting.

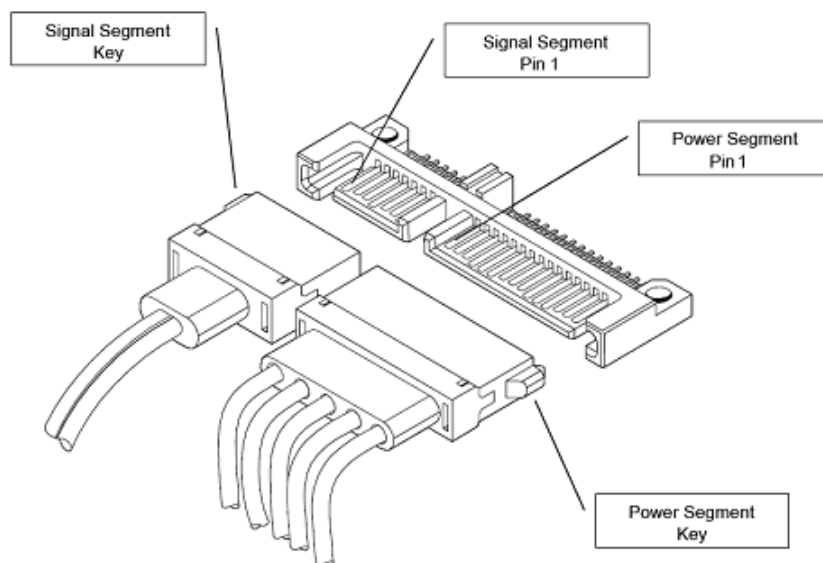
\*Sequential performance is based on CrystalDiskMark 5.2.1 with file size 1,000MB.

\*\*Random performance measured using IOMeter with Queue Depth 32.

## 1.4 Pin Assignments

Table 1-4 describes the SFD signal segment and Table1-5 for power segment.

**Figure 1-1 SATA Connectors**

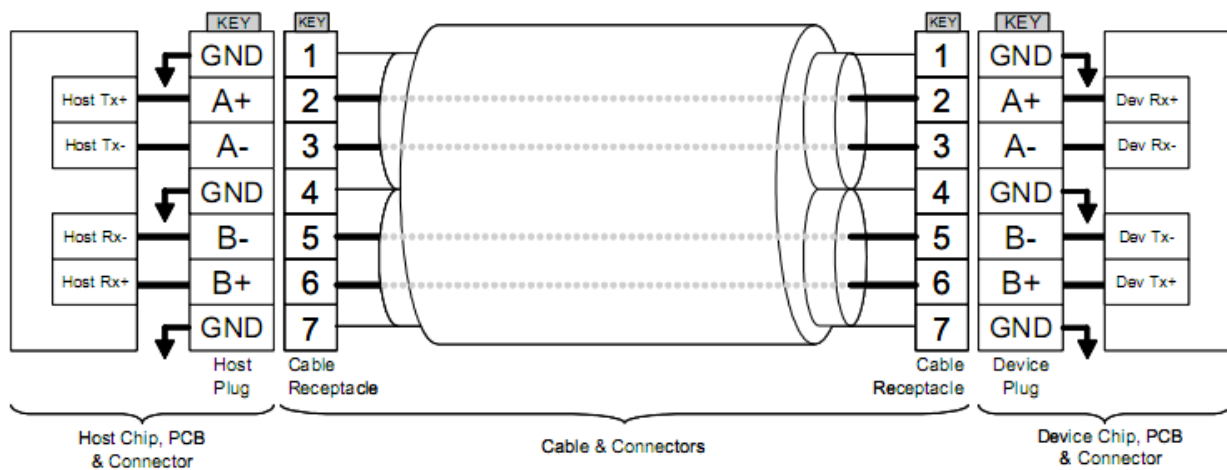


**Table 1-4 Signal Segment**

Pin	Type	Description
S1	GND	
S2	RxP	+ Differential Receive
S3	RxN	- Differential Receive
S4	GND	
S5	TxN	- Differential Transmit
S6	TxP	+ Differential Transmit
S7	GND	

**Table 1-5 Power Segment**

Pin	Signal/Description
Pin1	Unused (3.3V)
Pin2	Unused (3.3V)
Pin3	Device Sleep
Pin4	Ground
Pin5	Ground
Pin6	Ground
Pin7	5V
Pin8	5V
Pin9	5V
Pin10	Ground
Pin11	DAS
Pin12	Ground
Pin13	Unused (12V)
Pin14	Unused (12V)
Pin15	Unused (12V)



**Figure 1-2 SATA Cable/Connector Connection Diagram**

The connector on the left represents the Host with TX/RX differential pairs connected to a cable. The connector on the right shows the Device with TX/RX differential pairs also connected to the cable. Notice also the ground path connecting the shielding of the cable to the Cable Receptacle.

## 2. Software Interface

### 2.1 Command Set

This section defines the software requirements and the format of the commands the host sends to SM230-297. Commands are issued to SM230-297 by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command register.

**Table 2-1** Command Set

Code	Command	Code	Command
E5h	CHECK POWER MODE	F4h	SECURITY ERASE UNIT
06h	DATA SET MANAGEMENT	F5h	SECURITY FREEZE LOCK
92h	DOWNLOAD MICROCODE	F1h	SECURITY SET PASSWORD
90h	EXECUTE DEVICE DIAGNOSTIC	F2h	SECURITY UNLOCK
E7h	FLUSH CACHE	70h	SEEK
EAh	FLUSH CACHE EXT	EFh	SET FEATURES
ECh	IDENTIFY DEVICE	C6h	SET MULTIPLE MODE
E3h	IDLE	E6h	SLEEP
E1h	IDLE IMMEDIATE	B0h	SMART
91h	INITIALIZE DEVICE PARAMETERS	E2h	STANDBY
E4h	READ BUFFER	E0h	STANDBY IMMEDIATE
C8h	READ DMA	E8h	WRITE BUFFER
25h	READ DMA EXT	CAh	WRITE DMA
60h	READ FPDMA QUEUED	35h	WRITE DMA EXT
C4h	READ MULTIPLE	3Dh	WRITE DMA FUA EXT
29h	READ MULTIPLE EXT	61h	WRITE FPDMA QUEUED
2Fh	READ LOG EXT	3Fh	WRITE LOG EXT
47h	READ LOG DMA EXT	57h	WRITE LOG DMA EXT
20h	READ SECTOR	C5h	WRITE MULTIPLE
24h	READ SECTOR EXT	39h	WRITE MULTIPLE EXT
40h	READ VERIFY SECTORS	CEh	WRITE MULTIPLE FUA EXT
42h	READ VERIFY SECTORS EXT	30h	WRITE SECTOR
10h	RECALIBRATE	34h	WRITE SECTOR EXT
F6h	SECURITY DISABLE PASSWORD	45h	WRITE UNCORRECTABLE EXT
F3h	SECURITY ERASE PREPARE		

**Table 2-2** Trusted Computing Feature Set

Code	Command	Code	Command
5Ch	TRUSTED RECEIVE	5Eh	TRUSTED SEND
5Dh	TRUSTED RECEIVE DMA	5Fh	TRUSTED SEND DMA

Note: This feature set is only applicable to products implemented with AES and Opal functions.

## 2.2 S.M.A.R.T.

S.M.A.R.T. is an abbreviation for Self-Monitoring, Analysis and Reporting Technology, a self-monitoring system that provides indicators of drive health as well as potential disk problems. It serves as a warning for users from unscheduled downtime by monitoring and displaying critical drive information. Ideally, this should allow taking proactive actions to prevent drive failure and make use of S.M.A.R.T. information for future product development reference.

Apacer devices use the standard SMART command B0h to read data out from the drive to activate our S.M.A.R.T. feature that complies with the ATA/ATAPI specifications. S.M.A.R.T. Attribute IDs shall include initial bad block count, total later bad block count, maximum erase count, average erase count, power on hours and power cycle. When the S.M.A.R.T. Utility running on the host, it analyzes and reports the disk status to the host before the device reaches in critical condition.

Note: Attribute IDs may vary from product models due to various solution design and supporting capabilities.

Apacer memory products come with S.M.A.R.T. commands and subcommands for users to obtain information of drive status and to predict potential drive failures. Users can take advantage of the following commands/subcommands to monitor the health of the drive.

Code	SMART Subcommand
D0h	READ DATA
D1h	READ ATTRIBUTE THRESHOLDS
D2h	ENABLE/DISABLE ATTRIBUTE AUTOSAVE
D4h	EXECUTE OFF-LINE IMMEDIATE
D5h	SMART READ LOG
D6h	SMART WRITE LOG
D8h	ENABLE OPERATIONS
D9h	DISABLE OPERATIONS
DAh	RETURN STATUS

### General SMART attribute structure

Byte	Description
0	ID (Hex)
1 – 2	Status Flag
3	Value
4	Worst
5*-11	Raw Data

\*Byte 5: LSB

SMART attribute ID list

ID (Hex)	Attribute Name
9 (0x09)	Power-on Hours
12 (0x0C)	Power Cycle Count
163 (0xA3)	Max. Erase Count
164 (0xA4)	Avg. Erase Count
166 (0xA6)	Total Later Bad Block Count
167 (0xA7)	SSD Protect Mode (Vendor Specific)
168 (0xA8)	SATA PHY Error Count
171 (0xAB)	Program Fail Count
172 (0xAC)	Erase Fail Count
175 (0xAF)	Bad Cluster Table Count
192 (0xC0)	Unexpected Power Loss Count
194 (0xC2)	Temperature
231 (0xE7)	Lifetime Left
241 (0xF1)	Total Sectors of Write

## 3. Flash Management

### 3.1 Error Correction/Detection

SM230-297 implements a hardware ECC scheme, based on the BCH algorithm. It can detect and correct up to 76 bits error in 1K bytes.

### 3.2 Bad Block Management

Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, page mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

### 3.3 Global Wear Leveling

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Global wear leveling is an important mechanism that levels out the wearing of all blocks so that the wearing-down of all blocks can be almost evenly distributed. This will increase the lifespan of SSDs.

### 3.4 Flash Translation Layer – Page Mapping

Page mapping is an advanced flash management technology whose essence lies in the ability to gather data, distribute the data into flash pages automatically, and then schedule the data to be evenly written. Page-level mapping uses one page as the unit of mapping. The most important characteristic is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different sizes of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. Thus, page mapping is adopted to increase random access speed and improve SSD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

### 3.5 ATA Secure Erase

ATA Secure Erase is an ATA disk purging command currently embedded in most of the storage drives. Defined in ATA specifications, (ATA) Secure Erase is part of Security Feature Set that allows storage drives to erase all user data areas. The erase process usually runs on the firmware level as most of the ATA-based storage media currently in the market are built-in with this command. ATA Secure Erase can securely wipe out the user data in the drive and protects it from malicious attack.

### 3.6 Power Failure Management

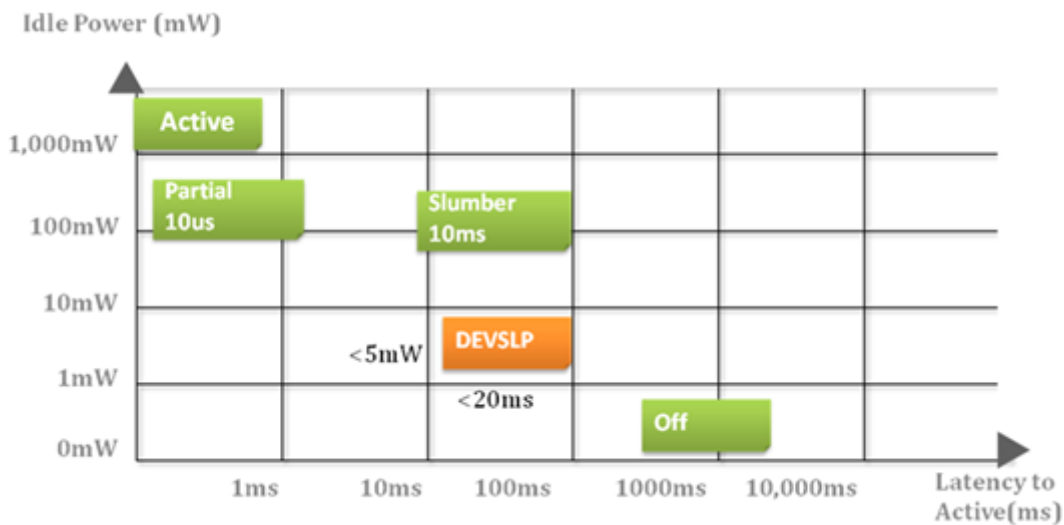
Power Failure Management plays a crucial role when power supply becomes unstable. Power disruption may occur when users are storing data into the SSD, leading to instability in the drive. However, with Power Failure Management, a firmware protection mechanism will be activated to scan pages and blocks once power is resumed. Valid data will be transferred to new blocks for merging and the mapping table will be rebuilt. Therefore, data reliability can be reinforced, preventing damage to data stored in the NAND Flash.

### 3.7 TRIM

TRIM is a SATA command that helps improve the read/write performance and efficiency of solid-state drives (SSD). The command enables the host operating system to inform SSD controller which blocks contain invalid data, mostly because of the erase commands from host. The invalid will be discarded permanently and the SSD will retain more space for itself.

### 3.8 Device Sleep (DevSleep or DEVSLP) Mode

Device Sleep is a feature that allows SATA devices to enter a low power mode by designating a particular pin as DEVSLP signal with an aim to reducing power consumption.



Parameter	Description & Conditions	Min	Max
V <sub>DIn</sub>	Tolerated input voltage.	-0.5 V	3.6 V
V <sub>HAssert</sub>	Voltage presented to host if signal not driven low. Value specified for all allowable I <sub>HAssert</sub> .	-	2.4 V
I <sub>HNegate</sub>	Device current delivered to host if host driving signal low. Value specified at V <sub>HNegate</sub> voltage of 0 V.	-	100 µA

### 3.9 SATA Power Management

By complying with SATA 6 Gb/s specifications, the SSD supports the following SATA power saving modes:

- ACTIVE: PHY ready, full power, Tx & Rx operational
- PARTIAL: Reduces power, resumes in under 10  $\mu$ s (microseconds)
- SLUMBER: Reduces power, resumes in under 10 ms (milliseconds)
- HIPM: Host-Initiated Power Management
- DIPM: Device-Initiated Power Management
- AUTO-SLUMBER: Automatic transition from partial to slumber.
- Device Sleep (DevSleep or DEVSLP): PHY powered down; power consumption  $\leq$  5 mW; host assertion time  $\leq$  10 ms; exit timeout from this state  $\leq$  20 ms (unless specified otherwise in SATA Identify Device Log).

Note: The behaviors of power management features would depend on host/device settings.

### 3.10 Hyper Cache Technology

Apacer proprietary Hyper Cache technology, a non-volatile SLC write cache, provides excellent performance to handle various scenarios in industrial use.

Using this method, a portion of the available capacity is being treated as SLC (1bit-per-cell) NAND flash memory in the Multi-Level Cell (MLC) models, two bits per cell technology, consists of a number of low and high pages. Apacer Hyper Cache Technology collects low pages for extraordinary performance, called Hyper Cache mode. And, the rest of high pages are combined together and performs normal MLC performance, called MLC mode. When data is written to SSD, the firmware will direct the data to Hyper Cache mode, thus improving the write speeds drastically.

### 3.11 SMART Read Refresh™

Apacer's SMART Read Refresh plays a proactive role in avoiding read disturb errors from occurring to ensure health status of all blocks of NAND flash. Developed for read-intensive applications in particular, SMART Read Refresh is employed to make sure that during read operations, when the read operation threshold is reached, the data is refreshed by re-writing it to a different block for subsequent use.

## 4. Security & Reliability Features

### 4.1 Advanced Encryption Standard (optional)

Advanced Encryption Standard (AES) is a specification for the encryption of electronic data. AES has been adopted by the U.S. government since 2001 to protect classified information and is now widely implemented in embedded computing applications. The AES algorithm used in software and hardware is symmetric so that encrypting/decrypting requires the same encryption key. Without the key, the encrypted data is inaccessible to ensure information security.

Notably in flash memory applications, AES 256-bit hardware encryption is the mainstream to protect sensitive or confidential data. The hardware encryption provides better performance, reliability, and security than software encryption. It uses a dedicated processor, which is built inside the controller, to process the encryption and decryption. This enormously shortens the processing time and makes it efficient.

### 4.2 TCG Opal (optional)

Developed by the Trusted Computing Group (TCG), an organization whose members work together to formulate industry standards, Opal is a set of security specifications used for applying hardware-based encryption to storage devices.

Hardware encryption has many advantages. First of all, it transfers the computational load of the encryption process to dedicated processors, reducing the stress on the host system's CPU. In addition, storage devices complying with Opal specifications are self-encryption devices. Opal specifications also feature boot authentication. When the drive is being accessed, the shadow MBR will request the drive password at boot. The drive will only unlock and decrypt if the correct password is supplied. The other feature is LBA-specific permissions. Users are assigned different permissions for LBA ranges created by the device administrator. Each LBA range is password-protected and can only be accessed by users with the correct key to perform permitted actions (read/write/erase).

### 4.3 Thermal Sensor

Apacer Thermal Sensor is a digital temperature sensor with serial interface. By using a designated pin for transmission, storage device owners are able to read temperature data.

## 5. Reliability Specifications

### 5.1 Environmental Specifications

Environmental specifications of SM230-297 product are shown in Table 5-1.

**Table 5-1** Environmental Specifications

Environment	Specifications
Temperature	0°C to 70°C (Standard); -40°C to 85°C (Wide)
	-40°C to 100°C (Non-operating)
Vibration	Non-operating: Sine wave, 15(G), 10~2000(Hz), Operating: Random, 7.69(GRMS), 20~2000(Hz)
Shock	Non-operating: Acceleration, 1,500 G, 0.5 ms Operating: Peak acceleration, 50 G, 11 ms

### 5.2 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in SM230-297. The prediction result for SM230-297 is more than 1,000,000 hours.

Note: The MTBF is predicated and calculated based on “Telcordia Technologies Special Report, SR-332, Issue 3” method.

### 5.3 Certification and Compliance

SM230-297 complies with the following standards:

- CE
- FCC
- RoHS
- MIL-STD-810F

## 5.4 Endurance

The endurance of a storage device is predicted by TeraBytes Written based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

**Table 5-2** Endurance Specifications

Capacity	TeraBytes Written
32 GB	42
64 GB	77
128 GB	136
256 GB	197
512 GB	208

Note:

- This estimation complies with JEDEC JESD-219, enterprise endurance workload of random data with payload size distribution.
- Flash vendor guaranteed MLC P/E cycle: 3K
- WAF may vary from capacity, flash configurations and writing behavior on each platform.
- 1 Terabyte = 1,024GB

## 6. Electrical Specifications

### 6.1 Operating Voltage

Table 6-1 lists the supply voltage for SM230-297.

**Table 6-1** Operating Range

Item	Range
Supply Voltage	5V $\pm$ 5%

### 6.2 Power Consumption

Table 6-2 lists the power consumption for SM230-297.

**Table 6-2** Power Consumption

Mode \ Capacity	32 GB	64 GB	128 GB	256 GB	512 GB
<b>Active (mA)</b>	420	445	480	645	500
<b>Idle (mA)</b>	105	105	110	110	105

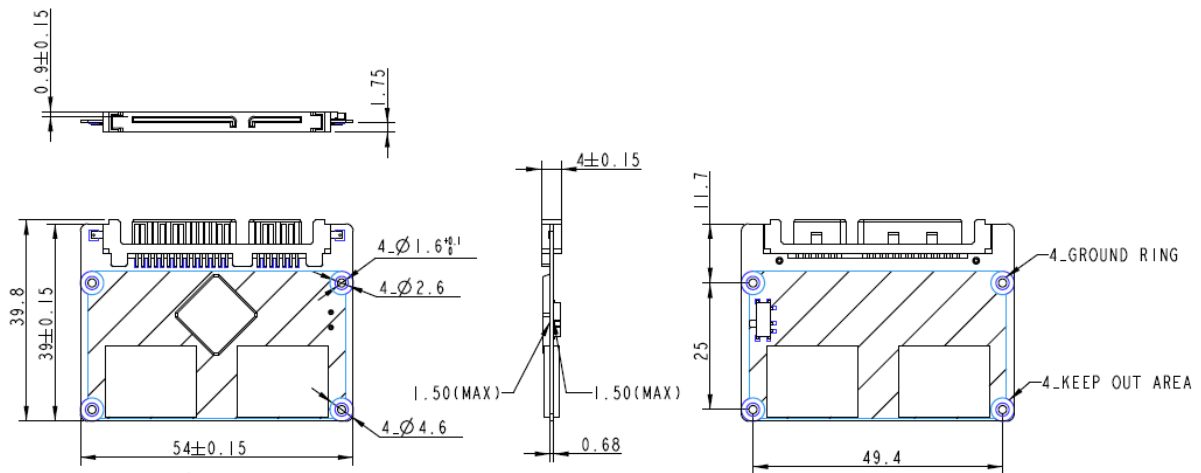
Note:

\*All values are typical and may vary depending on flash configurations or host system settings.

\*\*Active power is an average power measurement performed using CrystalDiskMark with 128KB sequential read/write transfers.

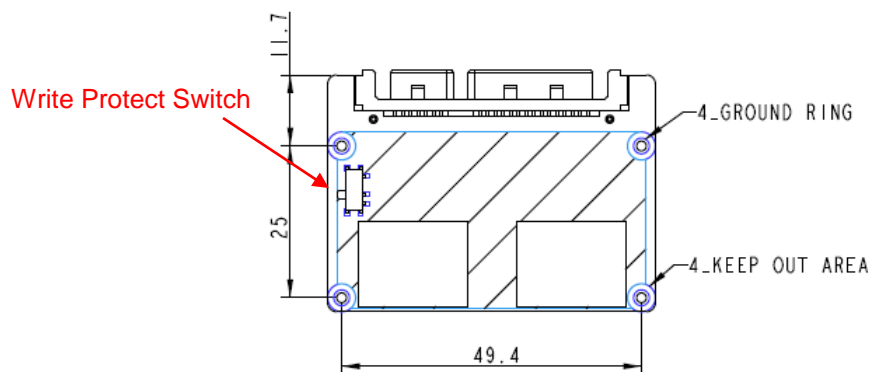
## 7. Physical Characteristics

### 7.1 Dimensions



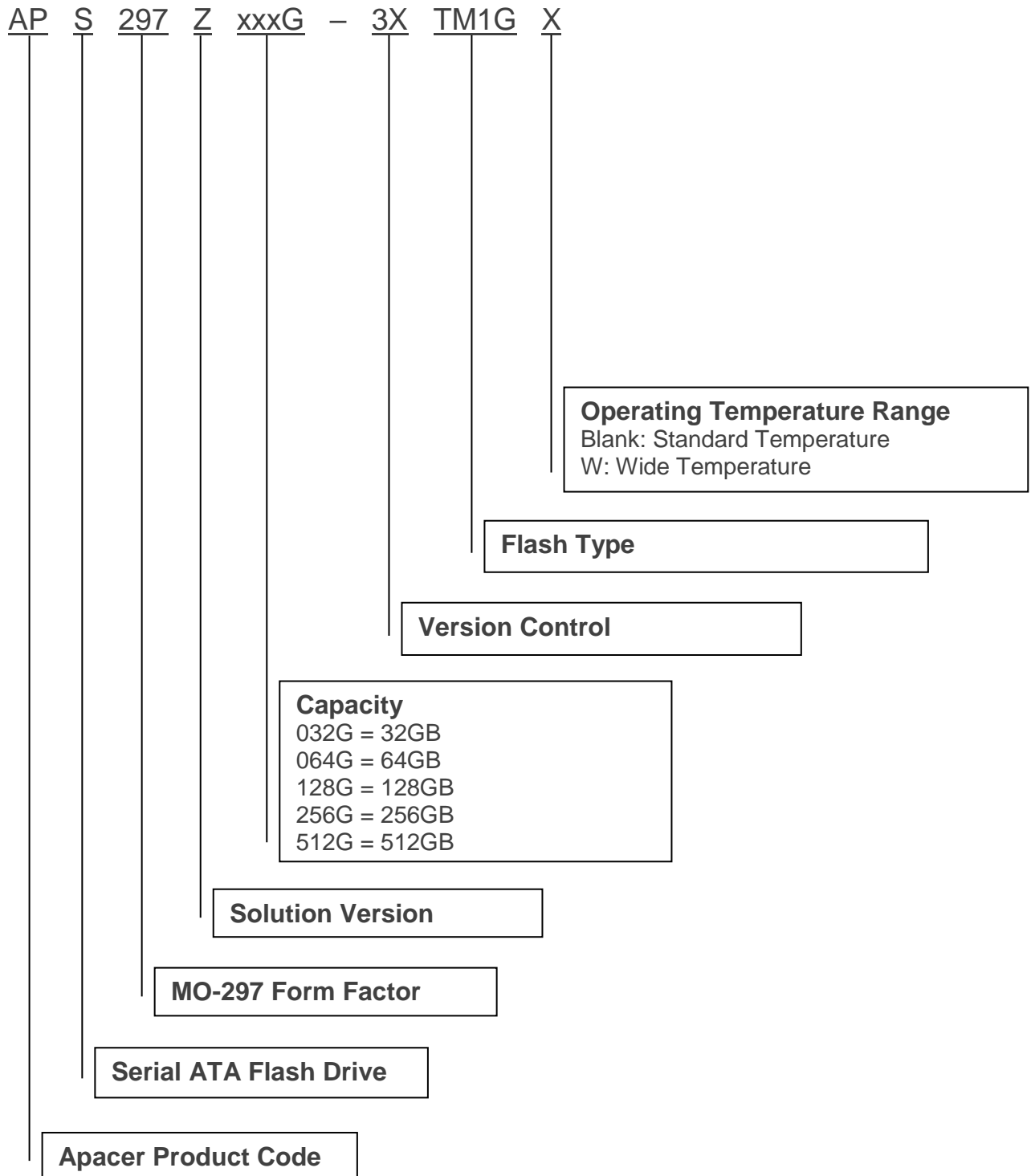
## 7.2 Write Protect Switch (optional)

Apacer implements the Virtual Write scheme that allows write commands to go through the flash controller and data temporarily stored, but no data has been actually written into the flash. Once the system is reset and rebooted, the temporarily stored data will be lost and nowhere to be found in the system. Since the Virtual Write scheme runs at device level, it requires no software or driver installation and is independent from the host OS.



## 8. Product Ordering Information

### 8.1 Product Code Designations



## 8.2 Valid Combinations

### 8.2.1 Standard

Capacity	Standard Temperature	Wide Temperature
32GB	APS297Z032G-3BTM1G	APS297Z032G-3BTM1GW
64GB	APS297Z064G-3BTM1G	APS297Z064G-3BTM1GW
128GB	APS297Z128G-3BTM1G	APS297Z128G-3BTM1GW
256GB	APS297Z256G-3BTM1G	APS297Z256G-3BTM1GW
512GB	APS297Z512G-3BTM1G	APS297Z512G-3BTM1GW

### 8.2.2 With AES/Opal Function (optional)

Capacity	Standard Temperature	Wide Temperature
32GB	APS297Z032G-3HTM1G	APS297Z032G-3HTM1GW
64GB	APS297Z064G-3HTM1G	APS297Z064G-3HTM1GW
128GB	APS297Z128G-3HTM1G	APS297Z128G-3HTM1GW
256GB	APS297Z256G-3HTM1G	APS297Z256G-3HTM1GW
512GB	APS297Z512G-3HTM1G	APS297Z512G-3HTM1GW

**Note:** Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

## Revision History

Revision	Description	Date
1.0	Official release	7/3/2018
1.1	Added a product photo to the cover page	7/5/2018
1.2	Revised ECC from 40 bits to 76 bits error in 1K bytes at 3.1 Error Correction/Detection	7/20/2018
1.3	<ul style="list-style-type: none"> <li>- Added Endurance to Specifications Overview</li> <li>- Added 5.4 Endurance</li> <li>- Mark Security features as optional on Specifications Overview page and 4. Security &amp; Reliability Features</li> </ul>	8/20/2018
1.4	Added a table to 3.8 DEVSLP (DevSleep or DEVSLP) Mode	8/23/2018
1.5	<ul style="list-style-type: none"> <li>- Renamed extended temperature to wide temperature</li> <li>- Updated technology description for 3.6 Power Failure Management</li> <li>- Updated 8. Product Ordering Information due to FW change</li> </ul>	7/12/2019
1.6	Updated 2.1 Command Set	11/15/2019
1.7	<ul style="list-style-type: none"> <li>- Changed SATA 6.0 Gbps to SATA 6 Gb/s in accordance with SATA naming guidelines</li> <li>- Added Hyper Cache Technology and SMART Read Refresh to Flash Management on Specifications Overview page</li> <li>- Updated Table 1-1 by changing max LBA to total LBA</li> <li>- Capitalized every letter for commands at 2.1 Command Set and SMART subcommand at 2.2 S.M.A.R.T.</li> <li>- Added 3.10 Hyper Cache Technology and 3.11 SMART Read Refresh</li> <li>- Modified the issue version for the note at 5.2 Mean Time Between Failures (MTBF)</li> <li>- Updated the notes for 5.4 Endurance</li> </ul>	6/16/2020
1.8	Updated the description of 3.2 Bad Block Management	6/19/2020
1.9	Updated Endurance section on Specifications Overview page and Table 5-2	7/22/2020

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