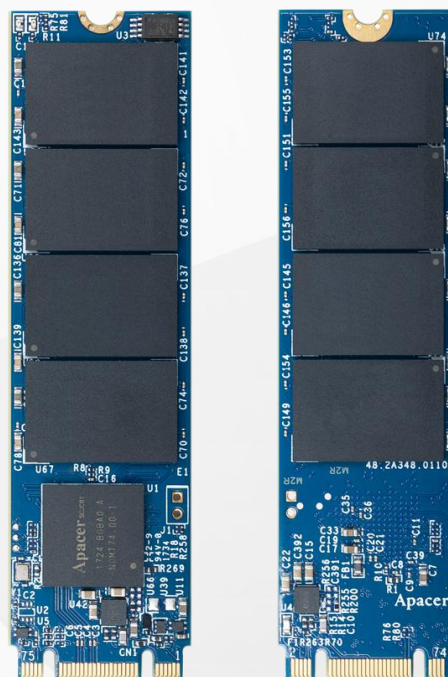


## RoHS Recast Compliant M.2 2280 Flash Drive

### SM230-M280 Product Specifications



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Version 1.4



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## Specifications Overview:

- **Compliance with SATA Interface**
  - Serial ATA Revision 3.1
  - SATA 6.0 Gbps
  - ATA-8 command set
  - Backward compatible with SATA 1.5/3.0 Gbps
- **Capacity**
  - Single side**
    - 32, 64, 128, 256 GB
  - Double side**
    - 512 GB
    - 1 TB (without TCG Opal support)
- **Performance\***
  - Burst read/write: 600 MB/sec
  - Sequential read: Up to 480 MB/sec
  - Sequential write: Up to 490 MB/sec
  - Seq. read QD32: Up to 560 MB/sec
  - Seq. write QD32: Up to 520 MB/sec
  - Random read (4K): Up to 41,000 IOPS
  - Random write (4K): Up to 63,000 IOPS
- **Flash Management**
  - Built-in hardware ECC
  - Global Wear Leveling
  - Flash bad-block management
  - Flash Translation Layer: Page Mapping
  - S.M.A.R.T.
  - Power Failure Management
  - Device Sleep (optional)
  - ATA Secure Erase
  - TRIM
  - Hyper Cache Technology
- **NAND Flash Type: MLC**
- **MTBF: >1,000,000 hours**
- **Temperature Range**
  - Operating:
    - Standard: 0°C to 70°C
    - Extended: -40°C to 85°C
  - Storage: -40°C to 100°C
- **Supply Voltage**
  - 3.3 V ± 5%
- **Power Consumption\***
  - Active mode: 710 mA
  - Idle mode: 125 mA
- **Connector Type**
  - 75-pin SATA-based M.2 module pinout
- **Form Factor**
  - M.2 2280 form factor
  - Dimensions:
    - Single side: 80.00 x 22.00 x 2.23, unit: mm
    - Double side: 80.00 x 22.00 x 3.58, unit: mm
- **Shock & Vibration\*\***
  - Shock: 1,500 G
  - Vibration: 4.02 GRMS
- **Security\*\*\***
  - Trusted Computing Group (TCG) Opal 2.0
  - AES 256-bit hardware encryption
- **Reliability**
  - Thermal Sensor
  - Thermal Management Technique
- **RoHS Recast Compliant (Complies with 2011/65/EU Standard)**

\*Varies from capacities. The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings. The term idle refers to the standby state of the device.

\*\*Non-operating

\*\*\*TCG Opal is not supported on 1TB model.

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## 1. General Descriptions

Apacer's SM230-M280 (M.2 2280) is the next generation modularized Solid State Drive (SSD) with the shape of all new M.2 form factor, with the aim to be the more suitable for mobile and compact computers with standard width at only 22.00 mm. SM230-M280 appears in M.2 2280 mechanical dimensions and is believed to be the leading add-in storage solution for future host computing systems.

The M.2 SSD is designed with SATA-based connector pinouts, providing full compliance with the latest SATA Revision 3.1 interface specifications. Aside from SATA compliance, SM230-M280 delivers exceptional performance and power efficiency. On the other hand, the extreme thin and light form factor makes SM230-M280 the ideal choice for mobile computing systems, which appears to be the trend in near future.

Regarding reliability, SM230-M280 is built with a powerful SATA controller that supports on-the-module ECC as well as efficient wear leveling scheme. Operating under SATA 6.0 Gbps interface, SM230-M280 is provided with Apacer latest S.M.A.R.T. that is primarily oriented for the latest SATA interface SSD, for drive lifetime monitoring and analyzing. Furthermore, with Advanced Encryption Standard (AES) and Trusted Computing Group (TCG) Opal support, SM230-M280 ensures data security and provides users with a peace of mind knowing their data is safeguarded against unauthorized use at all times.

## 2. Functional Block

Apacer SM230-M280 includes a single-chip SATA 6.0 Gbps and the flash media. The controller integrates the flash management unit to support multi-channel, multi-bank flash arrays. Figure 2-1 shows the functional block diagram.

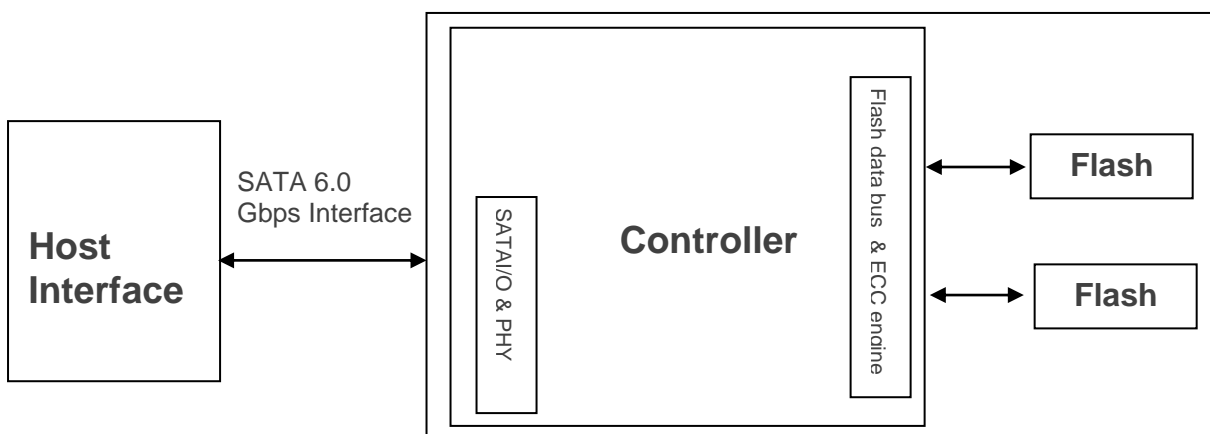
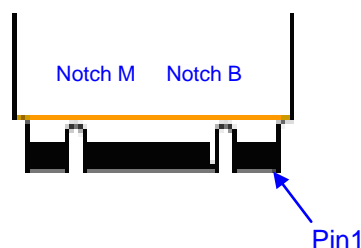


Figure 2-1 Block Diagram

### 3. Pin Assignments

This connector does not support hot plug capability. There are a total of 75 pins. 12 pin locations are used for mechanical key locations; this allows such a module to plug into both Key B and Key M connectors.



**Table 3-1** Pin Assignments

Pin	Type	Description
1	GND	Ground (according to M.2 configurations for SSD-SATA definition)
2	3.3V	Supply Pin, 3.3V
3	GND	Ground
4	3.3V	Supply pin, 3.3V
5	NC	No connect
6	NC	No connect
7	NC	No connect
8	NC	No connect
9	No connect	No connect
10	DAS/DSS	Device Activity Signal/Disable Staggered Spin-up
11	No connect	No connect (used for other purposes)
12	(removed for key)	Mechanical notch B
13	(removed for key)	Mechanical notch B
14	(removed for key)	Mechanical notch B
15	(removed for key)	Mechanical notch B
16	(removed for key)	Mechanical notch B
17	(removed for key)	Mechanical notch B
18	(removed for key)	Mechanical notch B
19	(removed for key)	Mechanical notch B
20	NC	No connect
21	GND	Ground (according to M.2 configurations for SSD-SATA definition)
22	NC	No connect
23	NC	No connect
24	NC	No connect
25	NC	No connect

Pin	Type	Description
26	NC	No connect
27	GND	Ground
28	NC	No connect
29	NC	Not used
30	NC	No connect
31	NC	Not used
32	NC	No connect
33	GND	Ground
34	NC	No connect
35	NC	Not used
36	NC	No connect
37	NC	Not used
38	DEVSLP	Device Sleep, input. If driven high the host is informing the SSD to enter a low power state
39	GND	Ground
40	NC	No connect
41	SATA-Rx+	Host receiver differential signal pair
42	NC	No connect
43	SATA-Rx-	Host receiver differential signal pair
44	NC	No connect
45	GND	Ground
46	NC	No connect
47	SATA-Tx-	Host transmitter differential pair
48	NC	No connect
49	SATA-Tx+	Host transmitter differential pair
50	NC	No connect
51	GND	Ground
52	NC	No connect
53	NC	No connect
54	NC	No connect
55	NC	No connect
56	Reserved/MFG Clock	Manufacturing pin. Use determined by vendor (no connect on a host)
57	GND	Ground
58	Reserved/MFG Clock	Manufacturing pin. Use determined by vendor (no connect on a host)
59	(removed for key)	Mechanical notch B
60	(removed for key)	Mechanical notch B
61	(removed for key)	Mechanical notch B

Pin	Type	Description
62	(removed for key)	Mechanical notch B
63	(removed for key)	Mechanical notch B
64	(removed for key)	Mechanical notch B
65	(removed for key)	Mechanical notch B
66	(removed for key)	Mechanical notch B
67	NC	No connect
68	SUSCLK	No connect
69	GND	Ground
70	3.3V	Supply pin, 3.3V
71	GND	Ground
72	3.3V	Supply pin, 3.3V
73	GND	Ground
74	3.3V	Supply pin, 3.3V
75	GND	Ground

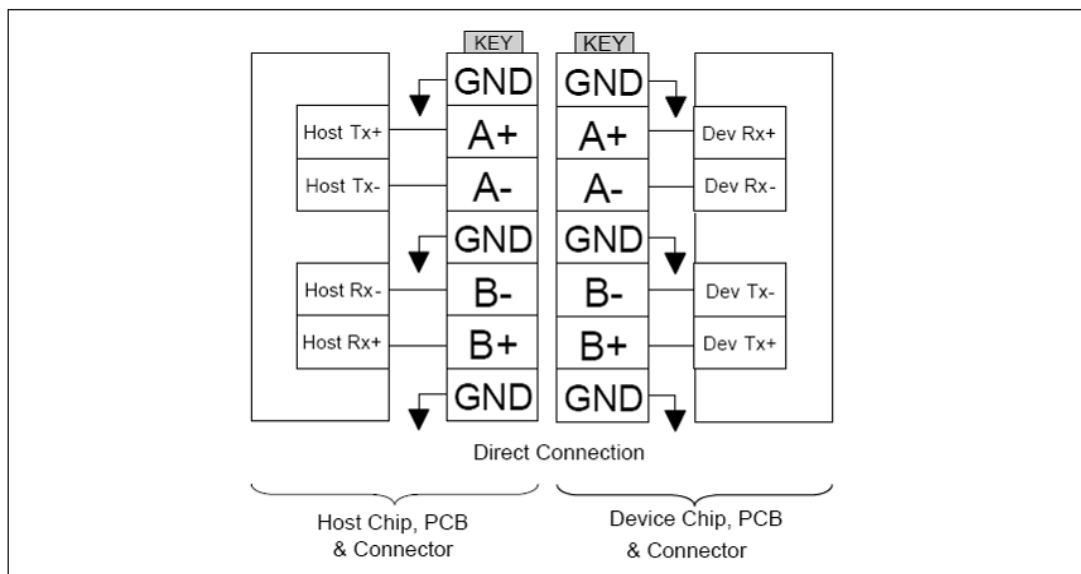


Figure 3-1 Direct Connection between the Host and Device

## 4. Product Specifications

### 4.1 Capacity

Capacity specifications of SM230-M280 are available as shown in Table 4-1. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

**Table 4-1** Capacity Specifications

Capacity	Total bytes*	Cylinders	Heads	Sectors	Max LBA
32 GB	32,017,047,552	16,383	16	63	62,533,296
64 GB	64,023,257,088	16,383	16	63	125,045,424
128 GB	128,035,676,160	16,383	16	63	250,069,680
256 GB	256,060,514,304	16,383	16	63	500,118,192
512 GB	512,110,190,592	16383	16	63	1,000,215,216
1 TB	1.024.209.543.168	16383	16	63	2,000,409,264

\*Display of total bytes varies from file systems, which means not all of the bytes can be used for storage.

\*\*Notes: 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.

LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

### 4.2 Performance

Performance of SM230-M280 is listed below in Table 4-2.

**Table 4-2** Performance Specifications

Performance	Capacity					
	32 GB	64 GB	128 GB	256 GB	512 GB	1 TB
<b>Sequential Read* (MB/s)</b>	480	480	475	475	460	435
<b>Sequential Write* (MB/s)</b>	165	210	445	440	485	490
<b>Seq. Read QD32* (MB/s)</b>	560	555	555	555	560	560
<b>Seq. Write QD32* (MB/s)</b>	270	230	445	445	510	520
<b>Random Read IOPS** (4K)</b>	23,000	22,000	33,000	33,000	41,000	41,000
<b>Random Write IOPS** (4K)</b>	15,000	18,000	37,000	40,000	62,000	63,000

Note:

Results may differ from various flash configurations or host system setting, and are measured on the environment without TCG Opal configurations. If measured on the environment configured with TCG Opal settings, performance may slightly decrease due to additional processing of hardware encryption.

\*Sequential performance is based on CrystalDiskMark 5.2.1 with file size 1,000MB.

\*\*Random performance measured using IOMeter with Queue Depth 32.

### 4.3 Environmental Specifications

Environmental specifications of SM230-M280 product are shown in Table 4-3.

**Table 4-3** Environmental Specifications

Item	Specifications
Operating temp.	0°C to 70°C (Standard); -40°C to 85°C (Extended)
Non-operating temp.	-40°C to 100°C
Operating vibration	7.69 GRMS, 20~2000 Hz/random (compliant with MIL-STD-810G)
Non-operating vibration	4.02 GRMS, 15~2000 Hz/random (compliant with MIL-STD-810G)
Operating shock	50G, 11ms
Non-operating shock	1500G, 0.5ms (compliant with MIL-STD-883K)

Note: This Environmental Specification table indicates the conditions for testing the device. Real world usages may affect the results.

### 4.4 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in SM230-M280. The prediction result for SM230-M280 is more than 1,000,000 hours.

Note: The MTBF is predicated and calculated based on “Telcordia Technologies Special Report, SR-332, Issue 2” method.

### 4.5 Certification and Compliance

SM230-M280 complies with the following standards:

- CE
- FCC
- RoHS Recast
- MIL-STD-810

## 5. Flash Management

### 5.1 Error Correction/Detection

SM230-M280 implements a hardware ECC scheme, based on the BCH algorithm. It can detect and correct up to 40 bits error in 1K bytes.

### 5.2 Bad Block Management

Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. When host performs program/erase command on a block, bad block may appear in Status Register. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, page mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

### 5.3 Global Wear Leveling

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Global wear leveling is an important mechanism that levels out the wearing of all blocks so that the wearing-down of all blocks can be almost evenly distributed. This will increase the lifespan of SSDs.

### 5.4 Power Failure Management

Power Failure Management plays a crucial role when experiencing unstable power supply. Power disruption may occur when users are storing data into the SSD. In this urgent situation, the controller would run multiple write-to-flash cycles to store the metadata for later block rebuilding. This urgent operation requires about several milliseconds to get it done. At the next power up, the firmware will perform a status tracking to retrieve the mapping table and resume previously programmed NAND blocks to check if there is any incompleteness of transmission.

### 5.5 ATA Secure Erase

ATA Secure Erase is an ATA disk purging command currently embedded in most of the storage drives. Defined in ATA specifications, (ATA) Secure Erase is part of Security Feature Set that allows storage drives to erase all user data areas. The erase process usually runs on the firmware level as most of the ATA-based storage media currently in the market are built-in with this command. ATA Secure Erase can securely wipe out the user data in the drive and protects it from malicious attack.

## 5.6 TRIM

TRIM is a SATA command that helps improve the read/write performance and efficiency of solid-state drives (SSD). The command enables the host operating system to inform SSD controller which blocks contain invalid data, mostly because of the erase commands from host. The invalid will be discarded permanently and the SSD will retain more space for itself.

## 5.7 Flash Translation Layer – Page Mapping

Page mapping is an advanced flash management technology whose essence lies in the ability to gather data, distribute the data into flash pages automatically, and then schedule the data to be evenly written. Page-level mapping uses one page as the unit of mapping. The most important characteristic is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different sizes of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. Thus, page mapping is adopted to increase random access speed and improve SSD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

## 5.8 DEVSLP (DevSleep or DEVSLP) Mode (optional)

Device Sleep is a feature that allows SATA devices to enter a low power mode by designating pin 38 as DEVSLP signal with an aim to reducing power consumption.



## 5.9 Hyper Cache Technology

Apacer proprietary Hyper Cache technology, a non-volatile SLC write cache, provides excellent performance to handle various scenarios in industrial use.

Using this method, a portion of the available capacity is being treated as SLC (1bit-per-cell) NAND flash memory in the Multi-Level Cell (MLC) models, two bits per cell technology, consists of a number of low and high pages. Apacer Hyper Cache Technology collects low pages for extraordinary performance, called Hyper Cache mode. And, the rest of high pages are combined together and performs normal MLC performance, called MLC mode. When data is written to SSD, the firmware will direct the data to Hyper Cache mode, thus improving the write speeds drastically.

## 5.10 SATA Power Management

By complying with SATA 6.0 Gb/s specifications, the SSD supports the following SATA power saving modes:

- ACTIVE: PHY ready, full power, Tx & Rx operational
- PARTIAL: Reduces power, resumes in under 10  $\mu$ s (microseconds)
- SLUMBER: Reduces power, resumes in under 10 ms (milliseconds)
- HIPM: Host-Initiated Power Management
- DIPM: Device-Initiated Power Management
- AUTO-SLUMBER: Automatic transition from partial to slumber.
- Device Sleep (DevSleep or DEVSLP): PHY powered down; power consumption  $\leq$  5 mW; host assertion time  $\leq$  10 ms; exit timeout from this state  $\leq$  20 ms (unless specified otherwise in SATA Identify Device Log).

Note:

1. The behaviors of power management features would depend on host/device settings.
2. Device Sleep mode is optional, depending on product ordering selections.

## 6. Security & Reliability Features

### 6.1 TCG Opal

Developed by the Trusted Computing Group (TCG), an organization whose members work together to formulate industry standards, Opal is a set of security specifications used for applying hardware-based encryption to storage devices.

Hardware encryption has many advantages. First of all, it transfers the computational load of the encryption process to dedicated processors, reducing the stress on the host system's CPU. In addition, storage devices complying with Opal specifications are self-encryption devices. Opal specifications also feature boot authentication. When the drive is being accessed, the shadow MBR will request the drive password at boot. The drive will only unlock and decrypt if the correct password is supplied. The other feature is LBA-specific permissions. Users are assigned different permissions for LBA ranges created by the device administrator. Each LBA range is password-protected and can only be accessed by users with the correct key to perform permitted actions (read/write/erase).

### 6.2 Advanced Encryption Standard

Advanced Encryption Standard (AES) is a specification for the encryption of electronic data. AES has been adopted by the U.S. government since 2001 to protect classified information and is now widely implemented in embedded computing applications. The AES algorithm used in software and hardware is symmetric so that encrypting/decrypting requires the same encryption key. Without the key, the encrypted data is inaccessible to ensure information security.

Notably in flash memory applications, AES 256-bit hardware encryption is the mainstream to protect sensitive or confidential data. The hardware encryption provides better performance, reliability, and security than software encryption. It uses a dedicated processor, which is built inside the controller, to process the encryption and decryption. This enormously shortens the processing time and makes it efficient.

### 6.3 Thermal Sensor

Apacer Thermal Sensor is a digital temperature sensor with serial interface. By using designated pins for transmission, storage device owners are able to read temperature data.

### 6.4 Thermal Management Technique

Thermal management technique can monitor the temperature of the SSD equipped with a built-in thermal sensor via S.M.A.R.T. commands. This method can ensure the temperature of the device stays within temperature limits by drive throttling, i.e. reducing the speed of the drive when the device temperature reaches the threshold level, so as to prevent overheating, guarantee data reliability, and prolong product lifespan. When the temperature exceeds the maximum threshold level, thermal throttling will be triggered to reduce performance step by step to prevent hardware components from being damaged. Performance is only permitted to drop to the extent necessary for recovering a stable temperature to cool down the device's temperature. Once the temperature decreases to the minimum threshold value, transfer speeds will rise back to its optimum performance level.

## 7. Software Interface

### 7.1 Command Set

This section defines the software requirements and the format of the commands the host sends to SM230-M280. Commands are issued to SM230-M280 by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command register.

**Table 7-1** Command Set

Code	Command	Code	Command
E5h	Check Power Mode	F4h	Security Erase Unit
06h	Data Set Management	F5h	Security Freeze Lock
92h	Download Microcode	F1h	Security Set Password
90h	Execute Device Diagnostic	F2h	Security Unlock
E7h	Flush Cache	70h	Seek
EAh	Flush Cache EXT	EFh	Set Features
ECh	Identify Device	C6h	Set Multiple Mode
E3h	Idle	E6h	Sleep
E1h	Idle Immediate	B0h	SMART
91h	Initialize Device Parameters	E2h	Standby
E4h	Read Buffer	E0h	Standby Immediate
C8h	Read DMA	E8h	Write Buffer
25h	Read DMA EXT	CAh	Write DMA
60h	Read FPDMA Queued	35h	Write DMA EXT
C4h	Read Multiple	3Dh	Write DMA FUA EXT
29h	Read Multiple EXT	61h	Write FPDMA Queued
2Fh	Read Log EXT	3Fh	Write Log EXT
47h	Read Log DMA EXT	57h	Write Log DMA EXT
20h	Read Sector	C5h	Write Multiple
24h	Read Sector EXT	39h	Write Multiple EXT
40h	Read Verify Sectors	CEh	Write Multiple FUA EXT
42h	Read Verify Sectors EXT	30h	Write Sector
10h	Recalibrate	34h	Write Sector EXT
F6h	Security Disable Password	45h	Write Uncorrectable EXT
F3h	Security Erase Prepare		

**Table 7-2** Trusted Computing Feature Set

Code	Command	Code	Command
5Ch	Trusted Receive	5Eh	Trusted Send
5Dh	Trusted Receive DMA	5Fh	Trusted Send DMA

Note: This feature set is only applicable to products implemented with AES and Opal functions.

## 7.2 S.M.A.R.T.

S.M.A.R.T. is an abbreviation for Self-Monitoring, Analysis and Reporting Technology, a self-monitoring system that provides indicators of drive health as well as potential disk problems. It serves as a warning for users from unscheduled downtime by monitoring and displaying critical drive information. Ideally, this should allow taking proactive actions to prevent drive failure and make use of S.M.A.R.T. information for future product development reference.

Apacer devices use the standard SMART command B0h to read data out from the drive to activate our S.M.A.R.T. feature that complies with the ATA/ATAPI specifications. S.M.A.R.T. Attribute IDs shall include initial bad block count, total later bad block count, maximum erase count, average erase count, power on hours and power cycle. When the S.M.A.R.T. Utility running on the host, it analyzes and reports the disk status to the host before the device reaches in critical condition.

Note: Attribute IDs may vary from product models due to various solution design and supporting capabilities.

Apacer memory products come with S.M.A.R.T. commands and subcommands for users to obtain information of drive status and to predict potential drive failures. Users can take advantage of the following commands/subcommands to monitor the health of the drive.

Code	SMART Subcommand
D0h	READ DATA
D1h	READ ATTRIBUTE THRESHOLDS
D2h	Enable/Disable Attribute Autosave
D4h	Execute Off-line Immediate
D5h	Read Log (optional)
D6h	Write Log (optional)
D8h	Enable Operations
D9h	Disable operations
DAh	Return Status

**General SMART attribute structure**

Byte	Description
0	ID (Hex)
1 – 2	Status flag
3	Value
4	Worst
5*-11	Raw Data

\*Byte 5: LSB

SMART attribute ID list

ID (Hex)	Attribute Name	Note
9 (0x09)	Power-on hours	General
12 (0x0C)	Power cycle count	General
163 (0xA3)	Max. erase count	General
164 (0xA4)	Avg. erase count	General
166 (0xA6)	Total later bad block count	General
167 (0xA7)	SSD Protect Mode	0: R/W, 3: Read Only
168 (0xA8)	SATA PHY Error Count	Command Fail Count
175 (0xAF)	Bad Cluster Table Count	ECC Fail Count
192 (0xC0)	Unexpected Power Loss Count	ATA Standby Command
194 (0xC2)	Temperature	PCB Temperature
241 (0xF1)	Total sectors of write	LBA

## 8. Electrical Specifications

### 8.1 Operating Voltage

Table 8-1 lists the supply voltage for SM230-M280.

**Table 8-1** Operating Range

Item	Range
Supply Voltage	3.3V ± 5% (3.135-3.465V)

### 8.2 Power Consumption

Table 8-2 lists the power consumption for SM230-M280.

**Table 8-2** Power Consumption

Mode \ Capacity	32 GB	64 GB	128 GB	256 GB	512 GB	1 TB
<b>Active (mA)</b>	605	630	480	710	675	685
<b>Idle (mA)</b>	125	125	125	125	125	120

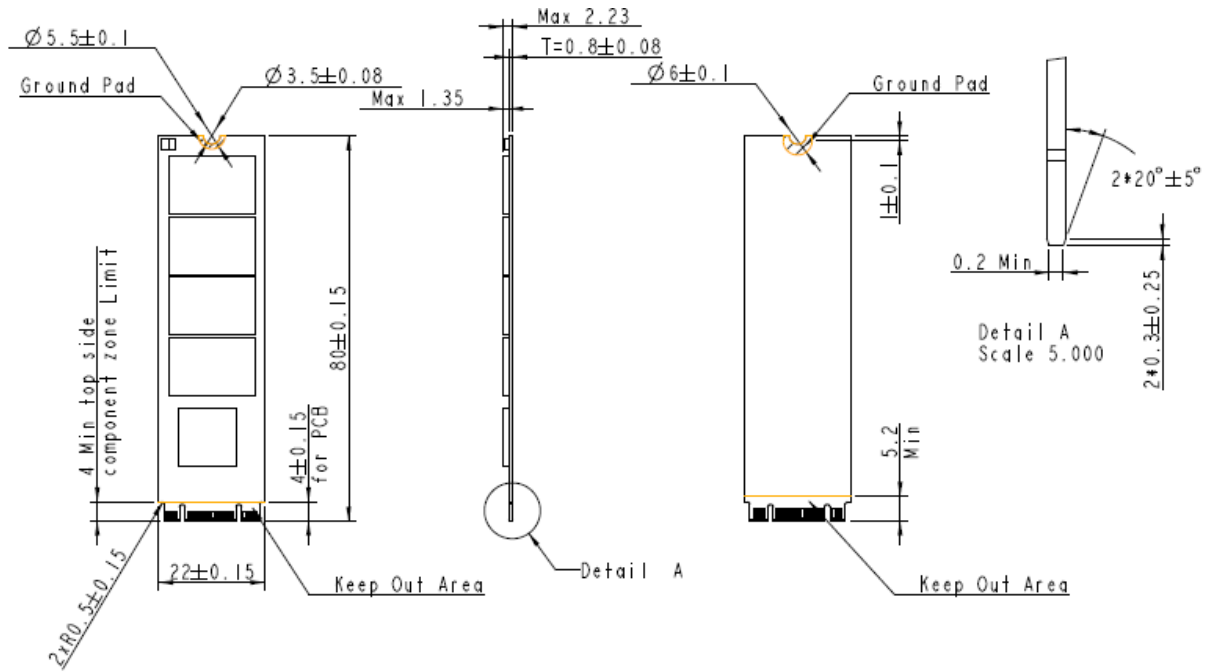
Note:

\*All values are typical and may vary depending on flash configurations or host system settings.

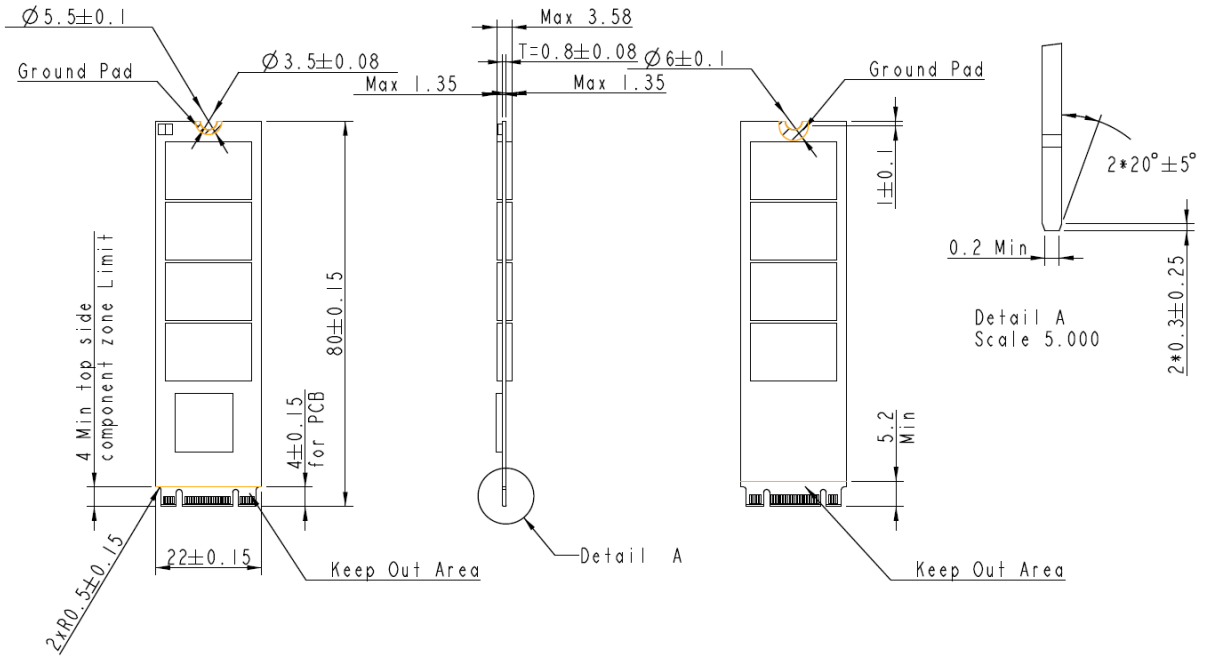
\*\*Active power is an average power measurement performed using CrystalDiskMark with 128KB sequential read/write transfers.

## 9. Physical Characteristics

### 9.1 Single Side

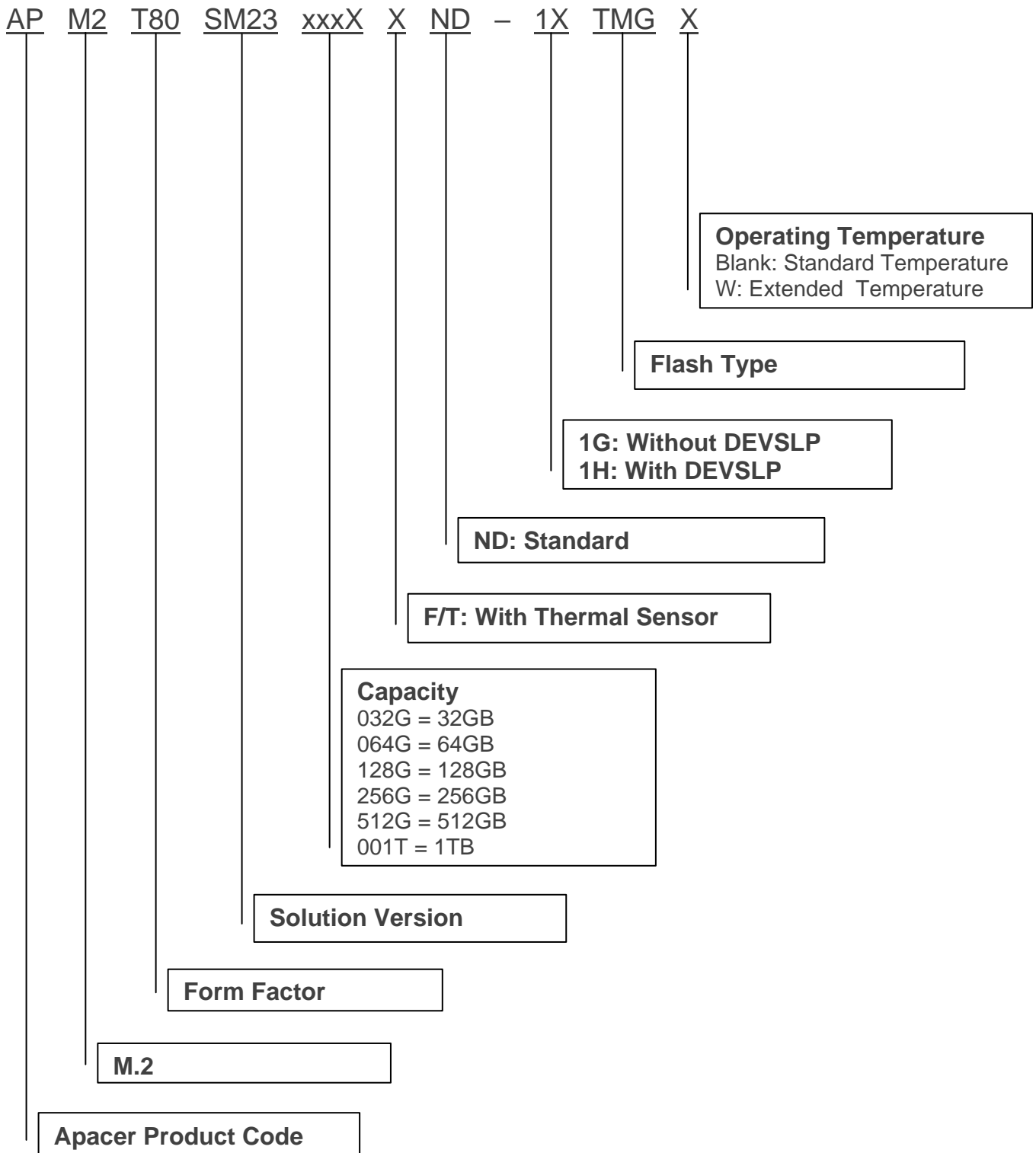


## 9.2 Double Side



## 10. Product Ordering Information

### 10.1 Product Code Designations



## 10.2 Valid Combinations

### 10.2.1 Standard Temperature + Thermal Sensor

Capacity	No DEVSLP	DEVSLP
32GB	APM2T80SM23032GTND-1GTMG	APM2T80SM23032GFND-1HTMG
64GB	APM2T80SM23064GTND-1GTMG	APM2T80SM23064GFND-1HTMG
128GB	APM2T80SM23128GTND-1GTMG	APM2T80SM23128GFND-1HTMG
256GB	APM2T80SM23256GTND-1GTMG	APM2T80SM23256GFND-1HTMG
512GB	APM2T80SM23512GTND-1GTMG	APM2T80SM23512GFND-1HTMG
1TB*	APM2T80SM23001TTND-1GTMG	APM2T80SM23001TFND-1HTMG

### 10.2.2 Extended Temperature + Thermal Sensor

Capacity	No DEVSLP	DEVSLP
32GB	APM2T80SM23032GTND-1GTMGW	APM2T80SM23032GFND-1HTMGW
64GB	APM2T80SM23064GTND-1GTMGW	APM2T80SM23064GFND-1HTMGW
128GB	APM2T80SM23128GTND-1GTMGW	APM2T80SM23128GFND-1HTMGW
256GB	APM2T80SM23256GTND-1GTMGW	APM2T80SM23256GFND-1HTMGW
512GB	APM2T80SM23512GTND-1GTMGW	APM2T80SM23512GFND-1HTMGW
1TB*	APM2T80SM23001TTND-1GTMGW	APM2T80SM23001TFND-1HTMGW

**Note:**

1. Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.
2. 1TB model does not support TCG Opal but AES function only.

## Revision History

Revision	Date	Description	Remark
1.0	11/30/2017	Official release	
1.1	12/1/2017	Added valid combinations with thermal sensor support (9.2.3 and 9.2.4 sections)	
1.2	12/19/2017	<ul style="list-style-type: none"> <li>- Categorized capacities into single side and double side on Features page</li> <li>- Added a note on Features page for Security Function that TCG Opal is not supported on 1TB model</li> <li>- Added a note to explain that the current performance results are measured on the environment without TCG Opal configurations at 4.2 Performance</li> <li>- Changed Thermal Management Technique feature from optional to standard</li> <li>- Removed valid combinations without thermal sensor support</li> </ul>	
1.3	2/22/2018	<ul style="list-style-type: none"> <li>- Added a note to 9.2 Valid Combinations to explain that TCG Opal is not supported on 1TB model but AES only</li> <li>- Removed the "optional" remark from security features including TCG Opal and AES</li> </ul>	
1.4	4/30/2018	<ul style="list-style-type: none"> <li>- Changed "Features" to "Specifications Overview"</li> <li>- Added Reliability section to Specifications Overview page</li> <li>- Added 6. Security &amp; Reliability Features</li> <li>- Modified single-side dimensions at Form Factor on Specifications Overview page and 9.1 Single Side</li> </ul>	

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