Apacer

RoHS Compliant

Micro Solid State Drive

SV170-µSSD Product Specifications

August 7, 2018

Version 1.0

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Apacer

Specifications Overview:

- **Standard Serial ATA Interface**
  - SATA 6.0 Gbps interface compliance
  - ATA-compatible command set
- **Capacity**
  - 30 GB
- **Performance***
  - Burst read/write: 600 MB/sec
  - Sequential read: Up to 295 MB/sec
  - Sequential write: Up to 130 MB/sec
  - Random read (4K): Up to 20,000 IOPS
  - Random write (4K): Up to 30,000 IOPS
- **Flash Management**
  - Low-Density Parity-Check (LDPC) Code
  - Global Wear Leveling
  - Flash bad-block management
  - Flash Translation Layer: Page Mapping
  - S.M.A.R.T.
  - Power Failure Management
  - ATA Secure Erase
  - Device Sleep
  - TRIM
  - Hyper Cache Technology
- **Reliability**
  - End-to-End Data Protection
- **NAND Flash Type:** 3D TLC (BiCS3)
- **MTBF:** >1,000,000 hours
- **Endurance (in drive writes per day: DWPD)**
  - 30 GB: 3 DWPD
- **Temperature Range**
  - Operating: 0°C to 70°C
  - Storage: -40°C to 100°C
- **Supply Voltage**
  - 3.3V ± 5%
  - 5V ± 5%
- **Power Consumption***

  @3.3V
  - Active mode: 260 mA
  - Idle mode:95 mA

  @5V
  - Active mode: 185 mA
  - Idle mode:80 mA
- **SATA Power Management**
  - Partial mode
  - Slumber mode
  - Device Sleep mode
- **Package**
  - 16 x 20 x 1.4, unit : mm
  - 156 Ball
- **Form Factor**
  - JEDEC MO-276
  - Net Weight: 0.76
- **RoHS Compliant**

*The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings.

Table of Contents

1. General Descriptions

Apacer Micro SSD (Micro SATA Disk Chip, µSSD) presents a revolutionary breakthrough of NAND flash storage technology. This micro sized SSD delivers all the technological benefits in NAND based storage solution with ultra speed SATA 6.0 Gbps interface in an embedded BGA form factor, compatible with JEDEC MO-276. Formed in a size of an IC chip, the performance level can reach up to 295 MB/s for read and 130 MB/s for write. With its micro-size and ultra speed, the µSDD is definitely the ideal storage solution for high performance demand mobile devices.

2. Functional Block

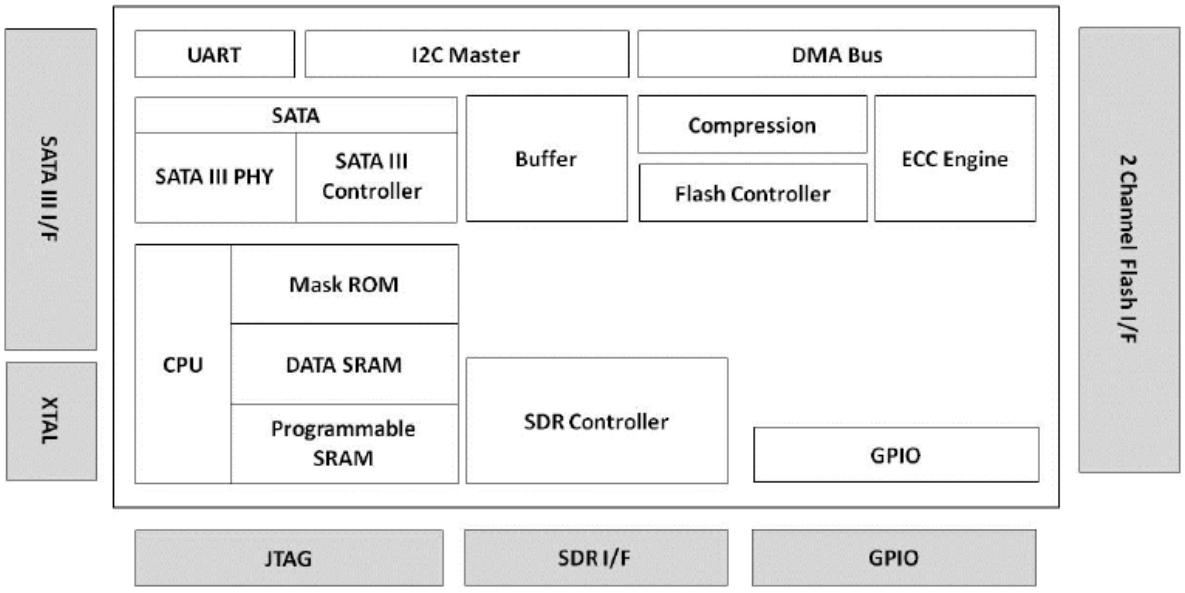
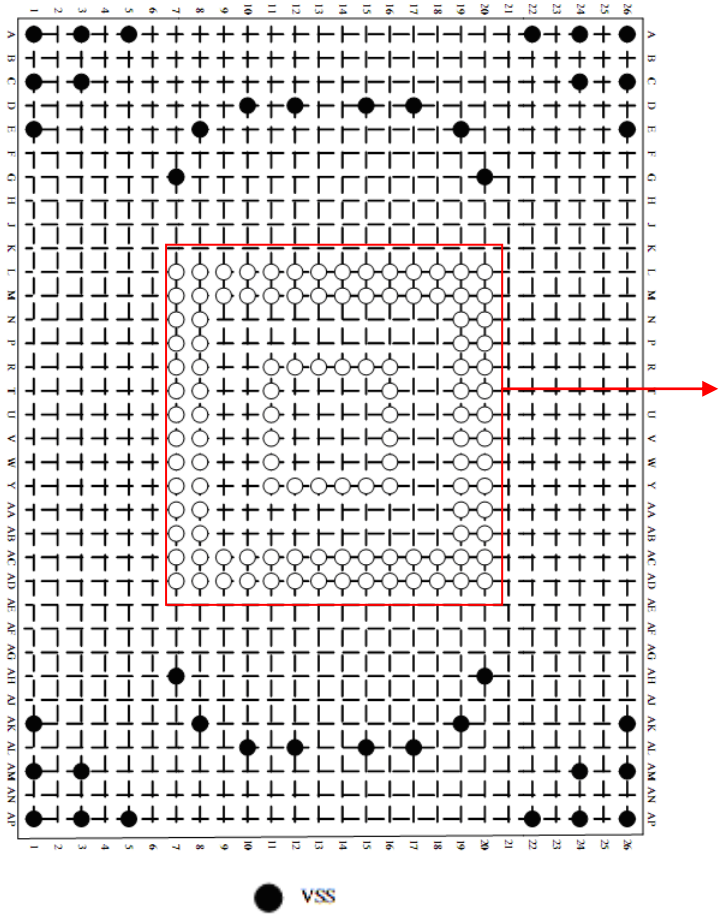


Figure 2-1 Functional Block Diagram

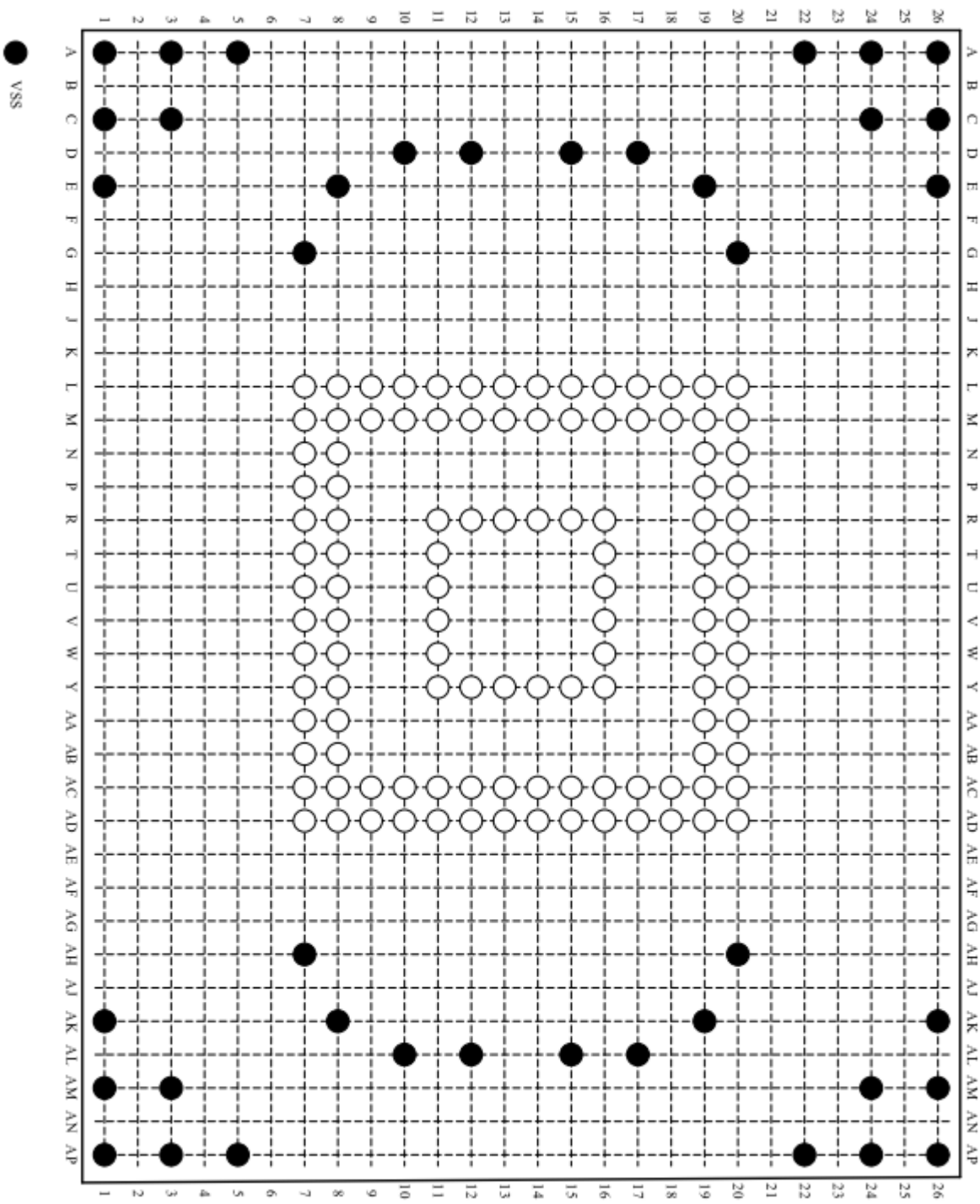
3. Pin Assignments

Top View



Pin Allocations

Top View (enlarged image)



Pin Allocations (enlarged image)

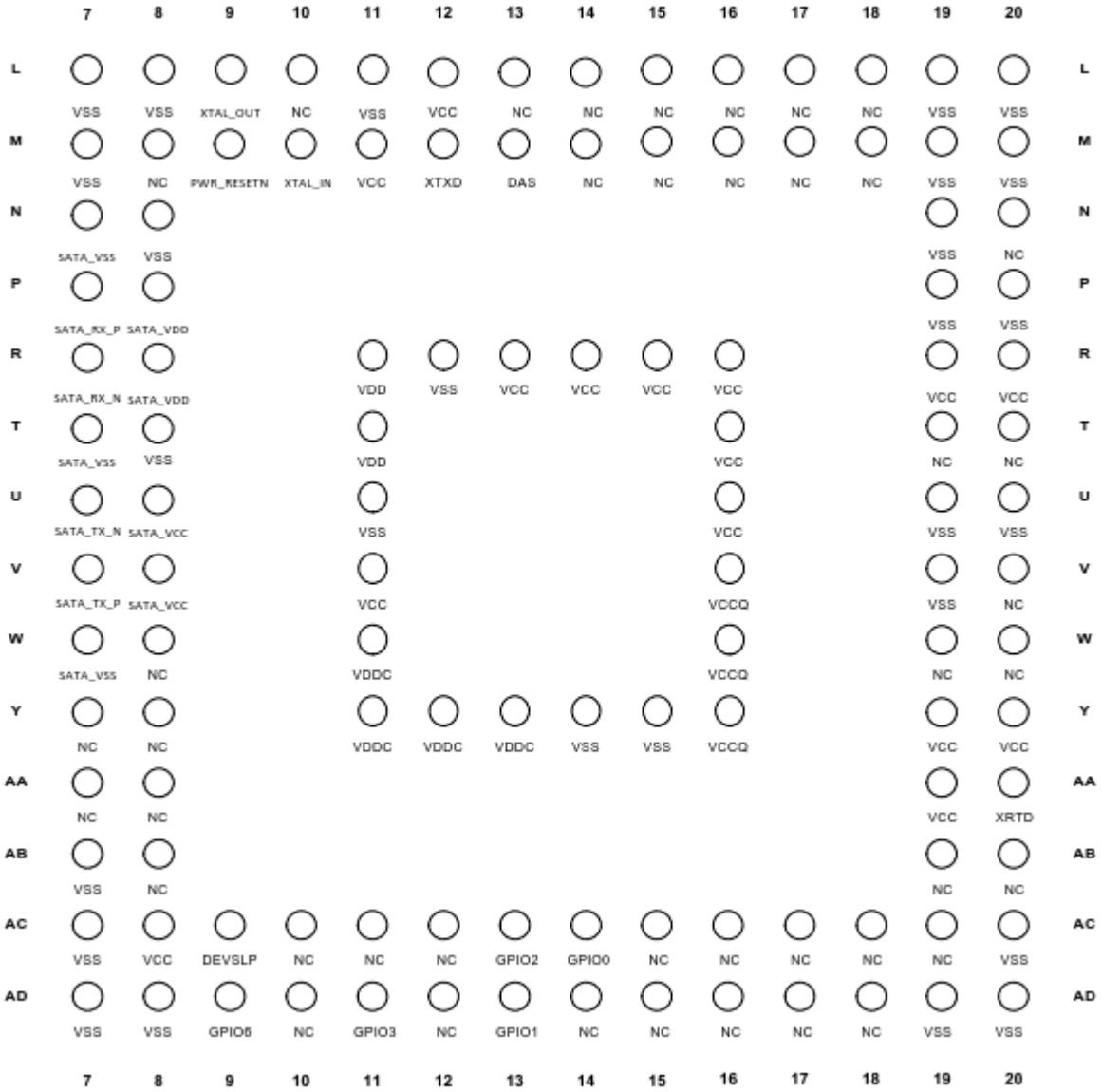


Table 3-1 Pin Description

Pin Name (Bottom view)	BGA156 (Top view)	Pin Type	PU/PD	Description
UART/GPIO				
XTXD XRXD	M12 AA20	O I	PU 75K	UART transmit/receive port (For Apacer internal debug use)
GPIO2*	AC14	IO	PU 75K	General purpose input/output pins
GPIO3*	AD9			
GPIO6*	AC13			
GPIO7*	AD11			
GPIO13*	AD13			
SATA Interface Signals				
SATA_RX_N SATA_RX_P	R7 P7	I		Differential signal pair A. SATA device receive signal differential pair
SATA_TX_N SATA_TX_P	U7 V7	O		Differential signal pair B. SATA device transmit signal differential pair
DAS	M13	O		Device activity signal
SATA_VCC	U8 V8			+3.3V
Control Signals				
XTAL_IN XTAL_OUT	M10 L9	I O		Crystal input/output pin (30MHz)
PWR_RESETN	M9	I		Hardware reset, low active**
Power Supply Signals				
VCC	L12, M11, R13, R14, R15, R16, R19, R20, T16, U16, V11, Y19, Y20, AA19, AC8			+3.3V
VDDC	W11, Y11, Y12, Y13			+1.2V***
VCCQ	V16, W16, Y16			+1.8V
GND Signals				
VSS	R12, U11, L7, L8, M7, N7, T7, W7, L11, L19, L20, M19, M20, N19, P19, AC20, AD20, AD19, AD8, AD7, T8, Y14, Y15, U19, P20, U20, V19, AC7, N8, A1, C1, E1, AK1, AM1, AP1, A3, C3, AM3, AP3, A5, AP5, G7, AH7, E8, AK8, D10, AL10, D12, AL12, D15, AL15,		Ground	

	D17, AL17, E19, AK19, G20, AH20, A22, AP22, A24, C24, AM24, AP24, A26, C26, E26, AK26, AM26, AP26			
Other Signals				
DEVSLP	AC9	I	PU 69.8K & PD 75K	Device Sleep, high active (normal is low)
NC	P8, R8, L15, L16, L17, L18, AA7, AA8, AB7, AB8, AB19, AB20, AC10, AC11, AC12, AC15, AC16, AC17, AC18, AC19, AD10, AD12, AD14, AD15, AD16, AD17, AD18, L10, M16, M17, M8, T19, T20, W19, W8, Y7, Y8, L13, L14, M14, M15, M18, N20, V20, W20, R11, T11			DNU

Note:
*The GPIO pins are non-connected by default. For specific configurations for the GPIO pins, such as Apacer Security Features, please consult with Apacer product managers or sales representatives for further details.
**There is an internal Power On Reset at ball #M9 and power on sequence of internal POR is 22ms.
***1.2V power is not required to be supplied by external power source but is provided by SV170-µSSD itself by design.

4. Product Specifications

4.1 Capacity

Capacity specifications of SV170-µSSD are available as shown in Table 4-1. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

Table 4-1 Capacity Specifications

Capacity	Total bytes*	Cylinders	Heads	Sectors	Max LBA
30 GB	30,016,659,456	16,383	16	63	58,626,288

*Display of total bytes varies from file systems, which means not all of the bytes can be used for storage.
**Notes: 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.
LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

4.2 Performance

Performance of SV170-µSSD is listed below in Table 4-2.

Table 4-2 Performance Specifications

Performance \ Capacity	30 GB
Sequential Read* (MB/s)	295
Sequential Write* (MB/s)	130
Random Read IOPS (4K)**	20,000
Random Write IOPS (4K)**	30,000

Note:
Results may differ from various flash configurations or host system setting.
*Sequential performance is based on CrystalDiskMark 5.2.1 with file size 1,000MB.
**Random performance measured using IOMeter with Queue Depth 32.

4.3 Environmental Specifications

Environmental specifications of SV170-µSSD product are shown in Table 4-3.

Table 4-3 Environmental Specifications

Item	Specifications
Operating temp.	0°C to 70°C
Non-operating temp.	-40°C to 85°C
ESD (Electrostatic Discharge)*	23°C, 49% (RH)
Acoustic	0dB

*Device functions are affected, but EUT will be back to its normal or operational state automatically.

4.4 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in SV170-µSSD. The prediction result for SV170-µSSD is more than 1,000,000 hours.

Note: The MTBF is predicated and calculated based on “Telcordia Technologies Special Report, SR-332, Issue 2” method.

4.5 Certification and Compliance

SV170-µSSD complies with the following standards:

- CE
- FCC
- RoHS
- BSMI

4.6 Endurance

The endurance of a storage device is predicted by Drive Writes Per Day based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

Table 4-4 Drive Writes Per Day

Capacity	Drive Writes Per Day
30 GB	3

Note:

- This estimation complies with JEDEC random client workload.
- Flash vendor guaranteed 3D NAND TLC P/E cycle: 3K*
- WAF may vary from capacity, flash configurations and writing behavior on each platform.
- 1 Terabyte = 1,024GB
- DWPD (Drive Writes Per Day) is calculated the number of times that user can overwrite the entire capacity of an SSD per day of its lifetime during the warranty period. (3D NAND TLC warranty: 2 years)

5. Flash Management

5.1 Error Correction/Detection

SV170-μSSD implements a hardware ECC scheme, based on the Low Density Parity Check (LDPC). LDPC is a class of linear block error correcting code which has apparent coding gain over BCH code because LDPC code includes both hard decoding and soft decoding algorithms. With the error rate decreasing, LDPC can extend SSD endurance and increase data reliability while reading raw data inside a flash chip.

5.2 Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. Thus, this device implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

5.3 Global Wear Leveling

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Global wear leveling is an important mechanism that levels out the wearing of all blocks so that the wearing-down of all blocks can be almost evenly distributed. This will increase the lifespan of SSDs.

5.4 Flash Translation Layer – Page Mapping

Page mapping is an advanced flash management technology whose essence lies in the ability to gather data, distribute the data into flash pages automatically, and then schedule the data to be evenly written. Page-level mapping uses one page as the unit of mapping. The most important characteristic is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different sizes of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. Thus, page mapping is adopted to increase random access speed and improve SSD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

5.5 Hyper Cache Technology

Apacer proprietary Hyper Cache technology, a non-volatile SLC write cache, provides excellent performance to handle various scenarios in industrial use.

Using this method, a portion of the available capacity is being treated as SLC (1bit-per-cell) NAND flash memory in the TLC models, two bits per cell technology, consists of a number of low and high pages. Apacer Hyper Cache Technology collects low pages for extraordinary performance, called Hyper Cache mode. And, the rest of high pages are combined together and performs normal TLC performance, called TLC mode. When data is written to SSD, the firmware will direct the data to Hyper Cache mode, thus improving the write speeds drastically.

5.6 Power Failure Management

Power Loss Protection is a mechanism to prevent data loss during unexpected power failure. DRAM is a volatile memory and frequently used as temporary cache or buffer between the controller and the NAND flash to improve the SSD performance. However, one major concern of the DRAM is that it is not able to keep data during power failure. Accordingly, SV170-µSSD applies the flushing mechanism which requests the controller to transfer data to the cache. For this SV170-µSSD, SDR performs as a cache, and its sizes include 8MB or 32MB. Only when the data is fully committed to the NAND flash will the controller send acknowledgement to the host. Such implementation can prevent false-positive performance and the risk of power cycling issues.

Additionally, it is critical for a controller to shorten the time the in-flight data stays in the cache. Thus, SV170-µSSD applies an algorithm to reduce the amount of data resides in the cache to provide a better performance by allowing incoming data to only have a “pit stop” in the cache and then move to the NAND flash at once. If the flash is jammed due to particular file sizes (random 4K), the cache will be treated as an “organizer”, consolidating incoming data into groups before written into the flash to improve write amplification.

In sum, with this power failure management, SV170-µSSD proves to provide the reliability required by consumer, industrial, and enterprise-level application.

5.7 ATA Secure Erase

ATA Secure Erase is an ATA disk purging command currently embedded in most of the storage drives. Defined in ATA specifications, (ATA) Secure Erase is part of Security Feature Set that allows storage drives to erase all user data areas. The erase process usually runs on the firmware level as most of the ATA-based storage media currently in the market are built-in with this command. ATA Secure Erase can securely wipe out the user data in the drive and protects it from malicious attack.

5.8 TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks all the time.

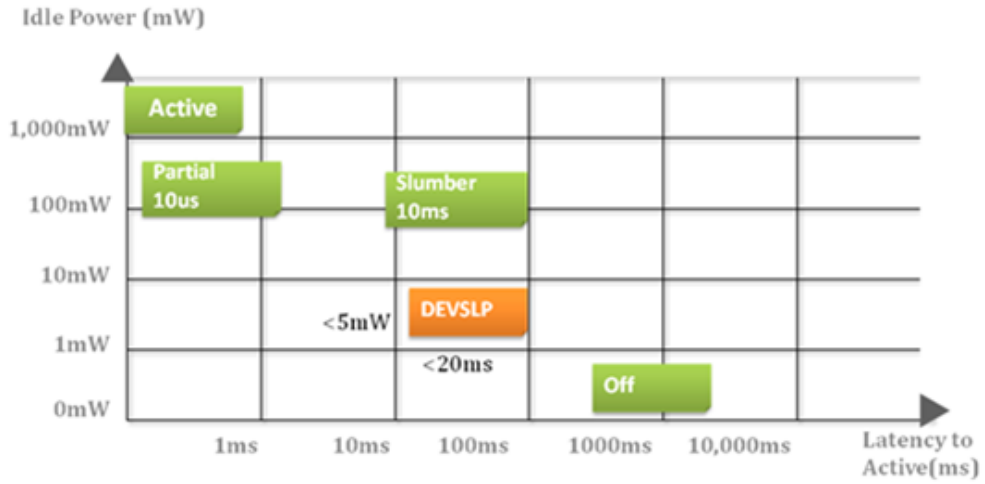
5.9 S.M.A.R.T.

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

5.10 DEVSLP (DevSleep or DEVSLP) Mode

Device Sleep is a feature that allows SATA devices to enter a low power mode by designating pin 44 as DEVSLP signal with an aim to reducing power consumption.

Note: With DEVSLP mode enabled, power consumption is under 10mw.



5.11 SATA Power Management

By complying with SATA 6.0 Gb/s specifications, the SSD supports the following SATA power saving modes:

- ACTIVE: PHY ready, full power, Tx & Rx operational
- PARTIAL: Reduces power, resumes in under 10 µs (microseconds)
- SLUMBER: Reduces power, resumes in under 10 ms (milliseconds)
- DEVSLP (Device Sleep): triggered by interface signal, PHY might be powered down, the device in a almost shut down state, consuming less power than Slumber mode, host support required for this mode

Note: The behaviors of power management features would depend on host/device settings.

6. Security & Reliability Features

6.1 End-to-End Data Protection

End-to-End Data Protection is a feature implemented in Apacer SSD products that extends error control to cover the entire path from the host computer to the drive and back, and ensure data integrity at multiple points in the path to enable reliable delivery of data transfers. Unlike ECC which does not exhibit the ability to determine the occurrence of errors throughout the process of data transmission, End-to-End Data Protection allows SSD controller to identify an error created anywhere in the path and report the error to the host computer before it is written to the drive. This error-checking and error-reporting mechanism therefore guarantees the trustworthiness and reliability of the SSD.

7. Software Interface

7.1 Command Set

Table 7-1 Command Set

Code	Command	Code		Command
00h	NOP	C9h		Read DMA without Retry
06h	Data Set Management	CAh		Write DMA
10h-1Fh	Recalibrate	CBh		Write DMA without Retry
20h	Read Sectors	CEh		Write Multiple FUA EXT
21	Read Sectors without Retry	E0h		Standby Immediate
24h	Read Sectors EXT	E1h		Idle Immediate
25h	Read DMA EXT	E2h		Standby
27h	Read Native Max Address EXT	E3h		Idle
29h	Read Multiple EXT	E4h		Read Buffer
2Fh	Read Log EXT	E5h		Check Power Mode
30h	Write Sectors	E6h		Sleep
31h	Write Sectors without Retry	E7h		Flush Cache
34h	Write Sectors EXT	E8h		Write Buffer
35h	Write DMA EXT	E9h		READ BUFFER DMA
37h	Set Native Max Address EXT	EAh		Flush Cache EXT
38h	CFA Write Sectors without Erase	EBh		Write Buffer DMA
39h	Write Multiple EXT	ECh		Identify Device
3Dh	Write DMA FUA EXT	EFh		Set Features
3Fh	Write Long EXT	EFh	02h	Enable volatile write cache
40h	Read Verify Sectors	EFh	03h	Set transfer mode
41h	Read Verify Sectors without Retry	EFh	05h	Enable the APM feature set
42h	Read Verify Sectors EXT	EFh	10h	Enable use of SATA feature set
44h	Zero EXT	EFh	10h 02h	Enable DMA Setup FIS Auto-Activate optimization
45h	Write Uncorrectable EXT	EFh	10h 03h	Enable Device-initiated interface power state (DIPM) transitions
47h	Read Log DMA EXT	EFh	10h 06h	Enable Software Settings Preservation (SSP)
57h	Write Log DMA EXT	EFh	10h 07h	Enable Device Automatic Partial to Slumber transitions
60h	Read FPDMA Queued	EFh	10h 09h	Enable Device Sleep
61h	Write FPDMA Queued	EFh	55h	Disable read look-ahead
70h-7Fh	Seek	EFh	66h	Disable reverting to power-on defaults

Code		Command	Code			Command
90h		Execute Device Diagnostic	EFh	82h		Disable volatile write cache
91h		Initialize Device Parameters	EFh	85h		Disable the APM feature set
92h		Download Microcode	EFh	90h		Disable use of SATA feature set
93h		Download Microcode DMA	EFh	90h	02h	Disable DMA Setup FIS Auto-Activate optimization
B0h		SMART	EFh	90h	03h	Disable Device-initiated interface power state (DIPM) transitions
B0h	D0h	SMART READ DATA	EFh	90h	06h	Disable Software Settings Preservation (SSP)
B0h	D1h	SMART READ ATTRIBUTE THRESHOLDS	EFh	90h	07h	Disable Device Automatic Partial to Slumber transitions
B0h	D2h	SMART ENABLE/DISABILE ATTRIBUTE AUTOSAVE	EFh	90h	09h	Disable Device Sleep
B0h	D3h	SMART SAVE ATTRIBUTE VALUES	EFh	AAh		Enable read look-ahead
B0h	D4h	SMART EXECUTE OFF-LINE IMMEDIATE	EFh	CCh		Enable reverting to power-on defaults
B0h	D5h	SMART READ LOG	F1h			Security Set Password
B0h	D6h	SMART WRITE LOG	F2h			Security Unlock
B0h	D8h	SMART ENABLE OPERATIONS	F3h			Security Erase Prepare
B0h	D9h	SMART DISABLE OPERATIONS	F4h			Security Erase Unit
B0h	DAh	SMART RETURN STATUS	F5h			Security Freeze Lock
B0h	DBh	SMART ENABLE/DISABILE AUTOMATIC OFF-LINE	F6h			Security Disable Password
B1h		Device Configuration	F8h			Read Native Max Address
B4h		Sanitize	F9h			Set Max Address
C4h		Read Multiple	F9h	01h		SET MAX SET PASSWORD
C5h		Write Multiple	F9h	02h		SET MAXLOCK
C6h		Set Multiple Mode	F9h	03h		SET MAX UNLOCK
C8h		Read DMA	F9h	04h		SET MAX FREEZE LOCIK

7.2 S.M.A.R.T.

S.M.A.R.T. is an abbreviation for Self-Monitoring, Analysis and Reporting Technology, a self-monitoring system that provides indicators of drive health as well as potential disk problems. It serves as a warning for users from unscheduled downtime by monitoring and displaying critical drive information. Ideally, this should allow taking proactive actions to prevent drive failure and make use of S.M.A.R.T. information for future product development reference.

Apacer devices use the standard SMART command B0h to read data out from the drive to activate our S.M.A.R.T. feature that complies with the ATA/ATAPI specifications. S.M.A.R.T. Attribute IDs shall include initial bad block count, total later bad block count, maximum erase count, average erase count, power on hours and power cycle. When the S.M.A.R.T. Utility running on the host, it analyzes and reports the disk status to the host before the device reaches in critical condition.

Note: Attribute IDs may vary from product models due to various solution design and supporting capabilities.

Apacer memory products come with S.M.A.R.T. commands and subcommands for users to obtain information of drive status and to predict potential drive failures. Users can take advantage of the following commands/subcommands to monitor the health of the drive.

Code	SMART Subcommand
D0h	READ DATA
D1h	READ ATTRIBUTE THRESHOLDS
D2h	Enable/Disable Attribute Autosave
D4h	Execute Off-line Immediate
D5h	Read Log (optional)
D6h	Write Log (optional)
D8h	Enable Operations
D9h	Disable operations
DAh	Return Status

General SMART attribute structure

Byte	Description
0	ID (Hex)
1 – 2	Status flag
3	Value
4	Worst
5*-11	Raw Data

*Byte 5: LSB

SMART attribute ID list

ID (Hex)	Attribute Name
9 (0x09)	Power-on hours
12 (0x0C)	Power cycle count
163 (0xA3)	Max. erase count
164 (0xA4)	Avg. erase count
166 (0xA6)	Total later bad block count
167 (0xA7)	SSD Protect Mode (vendor specific)
168 (0xA8)	SATA PHY Error Count
171 (0xAB)	Program fail count
172 (0xAC)	Erase fail count
175 (0xAF)	Bad Cluster Table Count
192 (0xC0)	Unexpected Power Loss Count
194 (0xC2)	Temperature
231 (0xE7)	Lifetime left
241 (0xF1)	Total sectors of write

8. Electrical Specifications

8.1 Operating Voltage

Table 8-1 lists the supply voltage for SV170-µSSD.

Table 8-1 Operating Range

Parameter	Voltage	Range
VCC	3.3V	3.135V ~ 3.465V
VCCQ	5V	4.75 ~ 5.25V

8.2 Power Consumption

Table 8-2 and 8-3 list the power consumption for SV170-µSSD.

Table 8-2 Power Consumption Based on 3.3V

Mode \ Capacity	30 GB
Active (mA)	260
Idle (mA)	95

Table 8-3 Power Consumption Based on 5V

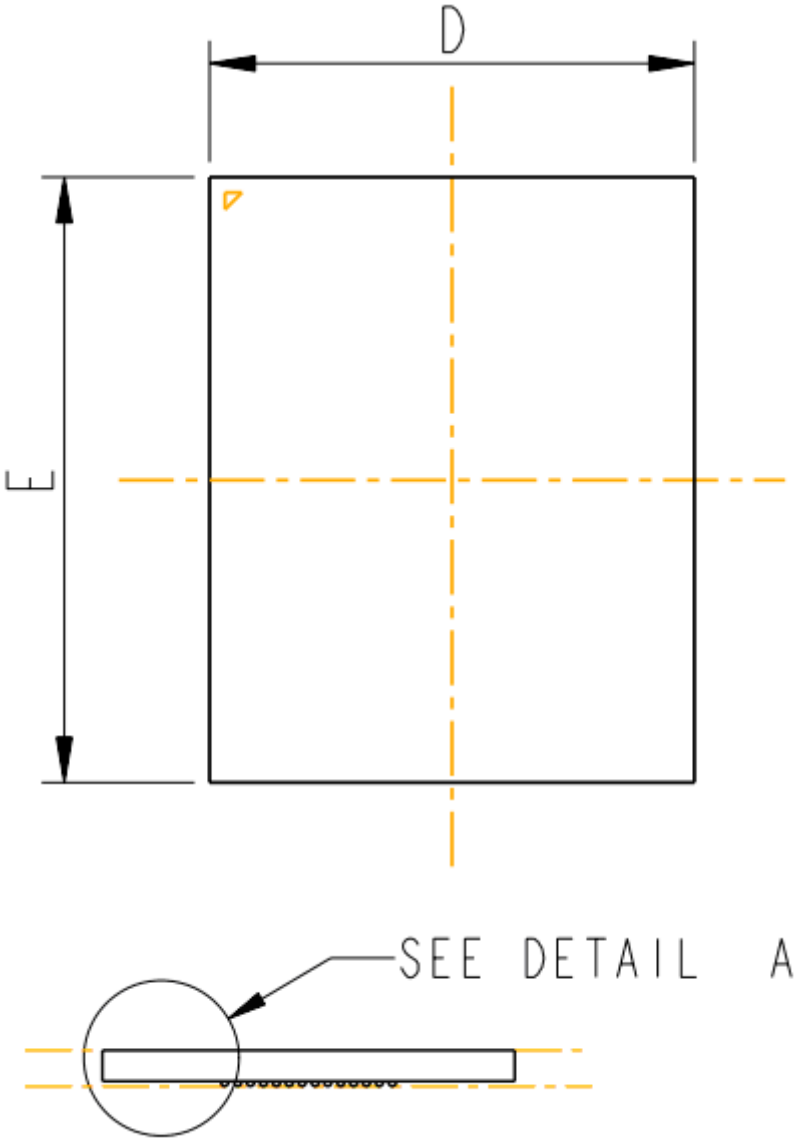
Mode \ Capacity	30 GB
Active (mA)	185
Idle (mA)	80

Note:
*All values are typical and may vary depending on flash configurations or host system settings.
**Active power is an average power measurement performed using CrystalDiskMark with 128KB sequential read/write transfers.

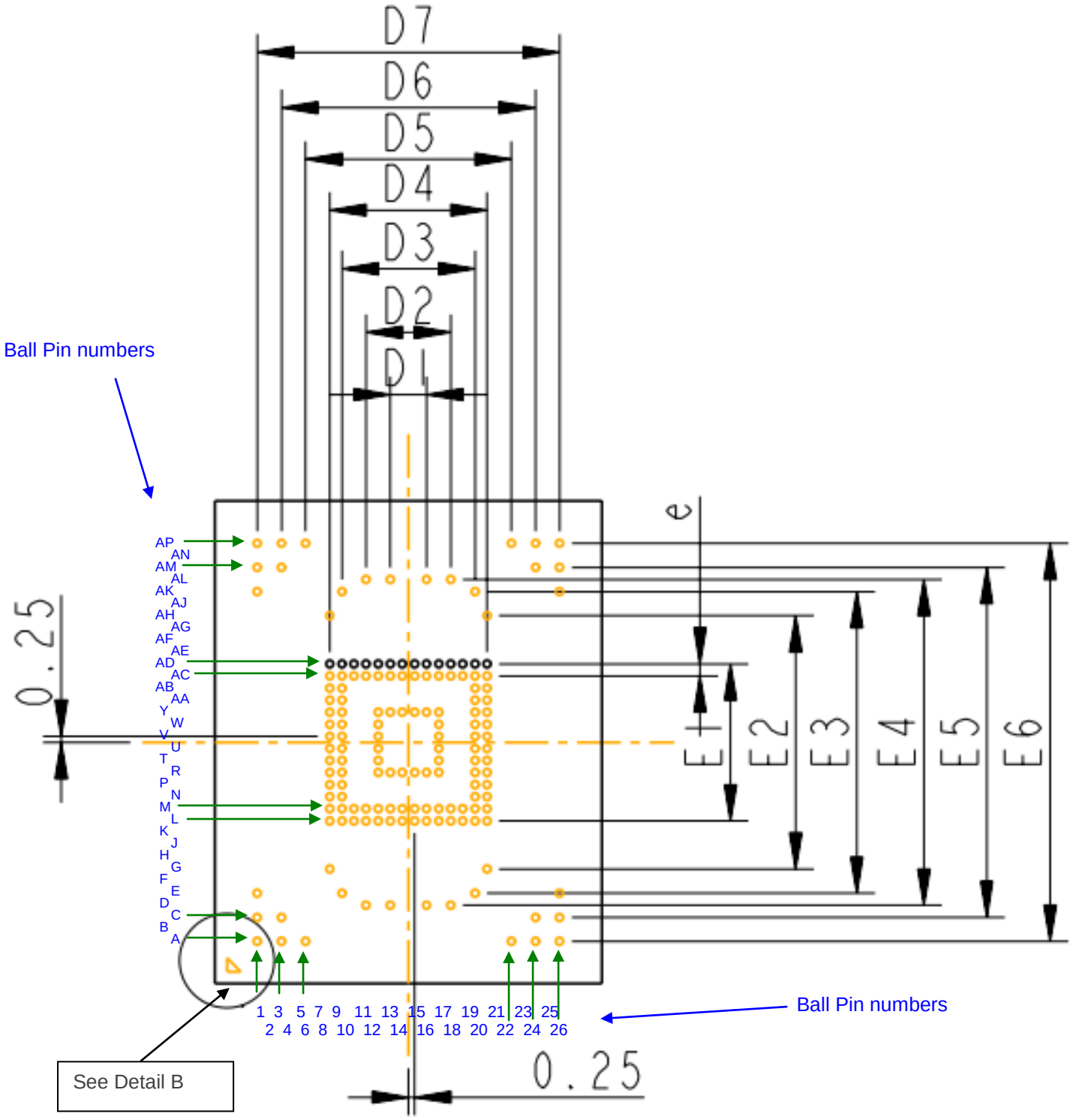
9. Physical Characteristics

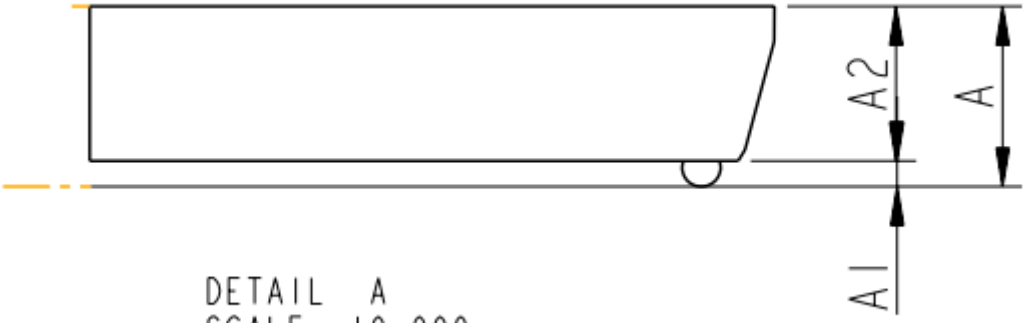
9.1 Dimensions

Top View

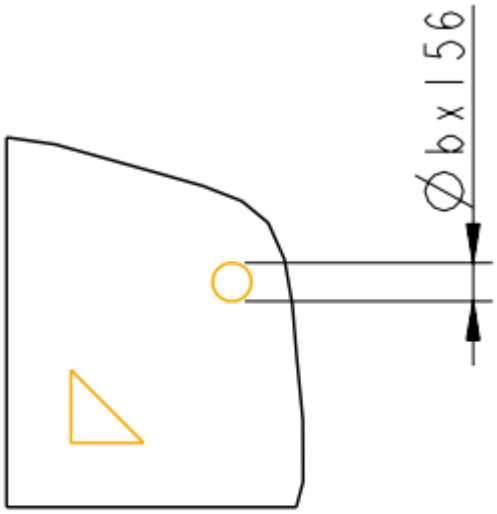


Bottom View





DETAIL A
SCALE 10.000



DETAIL B
SCALE 10.000

Symbol	Dimension		
	MIN	NOM	MAX
A	---	---	1.40
A1	0.15	---	---
A2	---	---	1.20
D	15.85	16	16.15
E	19.85	20	20.15
D1	---	1.5	---
D2	---	3.5	---
D3	---	5.5	---
D4	---	6.5	---
D5	---	8.5	---
D6	---	10.5	---
D7	---	12.5	---
E1	---	6.5	---
E2	---	10.5	---
E3	---	12.5	---
E4	---	13.5	---
E5	---	14.5	---
E6	---	16.5	---
e	---	0.50	---
b	0.25	0.30	0.35

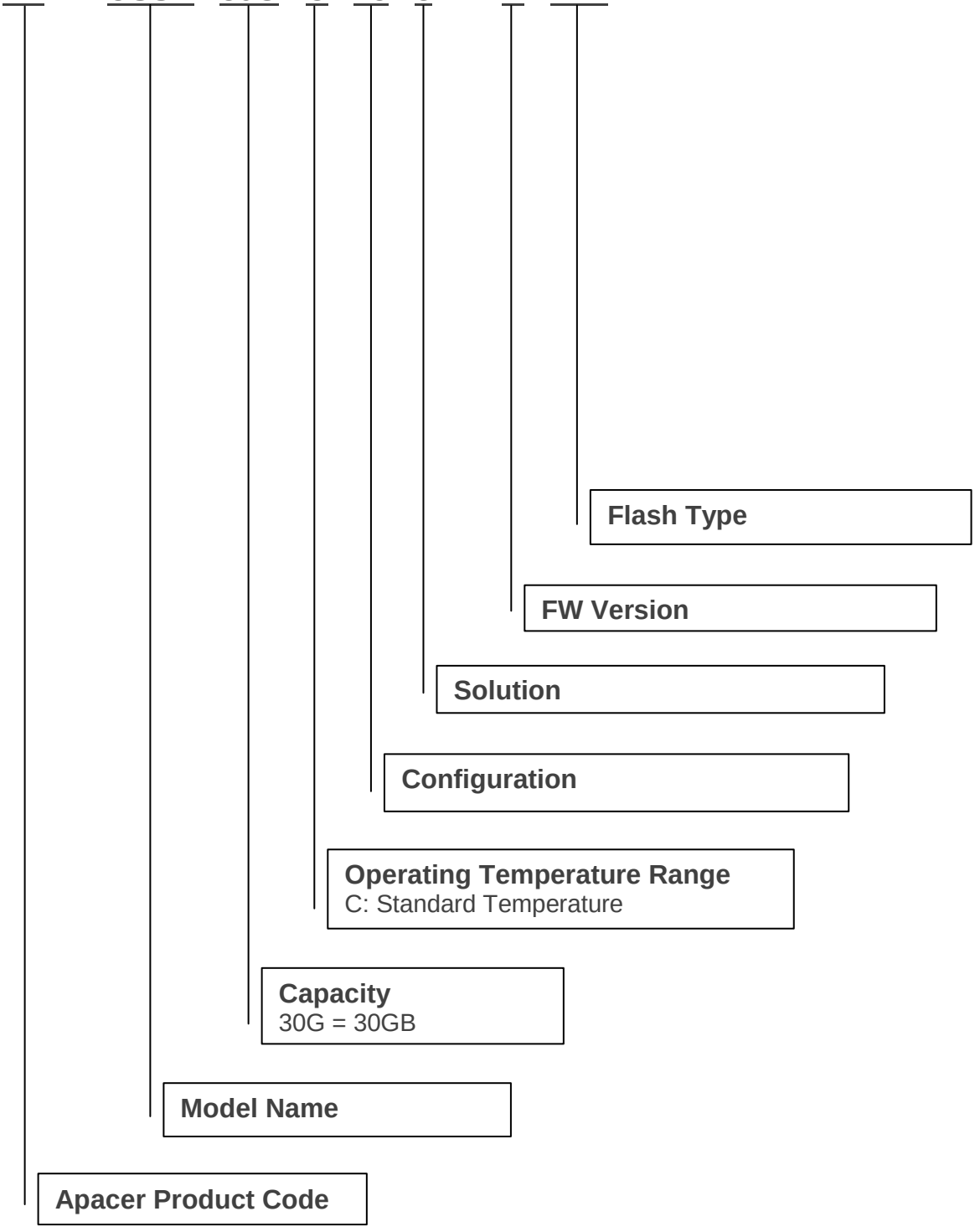
9.2 Net Weight

Capacity	Net Weight (g)
30GB	0.76

10. Product Ordering Information

10.1 Product Code Designations

AP - USSD 30G C 15 8 – D PTL



10.2 Valid Combinations

Capacity	Part Number
30GB	AP-USSD30GC158-DPTL

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Revision History

Revision	Description	Date
1.0	Official release	8/7/2018

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