RoHS Compliant

SATA-Disk Chip 4

Product Specifications

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Version 1.6

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Features:

- **Standard Serial ATA 2.6 (Gen. 2)**
  - Serial ATA 2.6 (Gen. 2)
  - SATA Ⅱ, 3.0 Gbps
  - ATA command set compatible
- **Connector type**
  - Standard 18/32 pin 600mil DIP
- **Form factor**
  - DIP form factor*
  - Dimension: 42.6x19.3x5.7, unit: mm
- **Power consumption (typical)****
  - Supply voltage: 3.3V
  - Active mode: 360 mA
  - Idle mode: 120 mA
- **Performance****
  - Burst transfer rate: 300 MB/sec
  - Sustained read: 85 MB/sec
  - Sustained write: 80 MB/sec
- **Capacity**
  - 1, 2, 4, 8, 16, 32 GB
- **NAND Flash Type:** SLC
- **Temperature ranges**
  - Operation: -40℃ to 85℃ (-40° ~ 185℉)
  - Storage: -40℃ to 100℃ (-40° ~ 212℉)
- **Intelligent endurance design**
  - Built-in hardware BCH ECC, correcting 16-bit or 24-bit error per 512-byte data sector
  - Static/dynamic Wear-Leveling scheme
  - Flash Bad-Block Management
  - Power Failure Management
  - ATA Secure Erase
  - S.M.A.R.T. technology
- **Shock & Vibration*****
  - Shock: 1500 (G)
  - Vibration: 15 (G)
- **MTBF:** >2,000,000 hours
- **RoHS compliant**

*Soldering the SDC4 (both hand and SMT reflow) will void the warranty
**Varies from capacities. The values for the power consumption and performances presented are typical and may vary depending on different settings and platforms.
***Non-operating

Table of Contents

1. General Description

Apacer's SATA-Disk Chip (SDC) is a high performance, embedded flash memory data storage system. This product is designed for embedded flash storage applications with expanded functionality and is a cost-effective replacement for a conventional IDE hard disk drive. Packaged in a 600 mil 32 or 18 round pin DIP form factor for easy and cost-effective mounting to a system motherboard, SDC offers reliable resistance to shock and vibration. Featuring technologies like ECC and Flash Bad Block Management, Apacer SSDs ensure data integrity and extended lifetime for blocks, making it one of the most compact and robust storage devices for PC/104 stackable applications.

In addition, SDC adopts the static wear-leveling scheme to allow uniform use of all storage blocks, significantly increasing the lifetime of a flash media and optimizing the disk performance as well. SDC provides the S.M.A.R.T. feature complying to the SATA Rev.2.6, ATA/ATAPI-7 specifications and uses the standard SMART command B0h to read data from the drive. This feature protects the user from unscheduled downtime by monitoring and storing critical drive performance. Featuring technologies like ECC and Flash Bad Block Management, Apacer SSDs ensure data integrity and extended lifetime for blocks, making it one of the most compact and robust storage devices for PC/104.

2. Functional Block

The SATA-Disk Chip (SDC) includes the SATA and Flash Management controllers, and flash media, as well as the SATA standard interface. Figure 2-1 shows the functional block diagram.

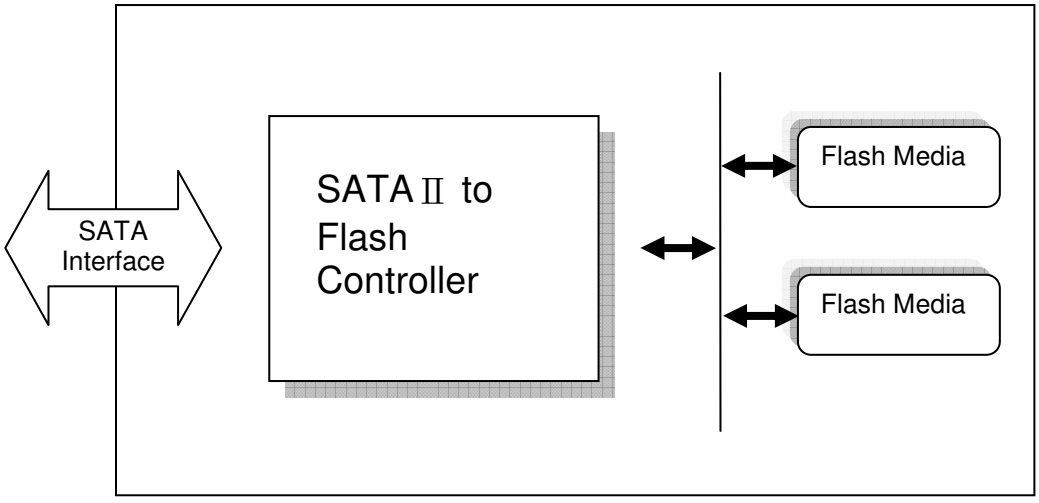


Figure 2-1: Functional block diagram

3. Functional Specifications

3.1 ATA Mode Support

The SATA-Disk Chip supports the following ATA operating modes:

- Supports up to PIO Mode-4
- Supports up to Multi-word DMA Mode-2
- Supports up to Ultra DMA Mode-5

3.2 Performance

Performance of SATA-Disk Chip is shown in table 3-1

Table 3-1: Performance specifications

Capacity / Performance	1 GB	2 GB	4 GB	8 GB	16 GB	32 GB
Sustained read (MB/s)	38	75	80	80	85	85
Sustained write (MB/s)	12	28	55	55	80	80

Note: Performances vary from flash configurations or host system settings.

3.3 Capacity Specification

Capacity specification of the SDC product family is available as shown in Table 3-2. It lists the specific capacity, the default numbers of logical cylinders and heads, and the number of logical sectors per track for each product line.

Table 3-2 Capacity specification

Capacity	Total Bytes	Cylinders	Heads	Sectors	Max LBA
1 GB	1,011,032,064	1,959	16	63	1,974,672
2 GB	2,011,226,112	3,897	16	63	3,928,176
4 GB	4,011,614,208	7,773	16	63	7,835,184
8 GB	8,012,390,400	15,525	16	63	15,649,200
16 GB	16,013,942,784	16383	16	63	31,277,232
32 GB	32,017,047,552	16,383	16	63	62,533,296

*Display of total bytes varies from file systems, which means not all of the bytes can be used for storage.
**Notes: 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.
LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

3.4 Environmental Specifications

Environmental specification of the SATA-Disk Chip (SDC) product family follows the MIL-STD-810F standards, as shown in Table 2-3.

Table 2-3: Environmental specifications

Environment		Specification
Temperature	Operation	-40℃ to 85℃
	Storage	-40℃ to 100℃
Vibration (operating)		20~2000(Hz), 7.69(g rms), random wave
Vibration (non-operating)		10~2000(Hz), 15(G), sine wave, X, Y, Z axis
Shock (operating)		50(G), 11(ms), half-sine wave, ±X, ±Y, ±Z axis
Shock (non-operating)		1500(G), 0.5(ms), half-sine wave, ±X, ±Y, ±Z axis

3.5 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in SDC4. The prediction result for SDC4 is more than 2,000,000 hours.

Notes about the MTBF:

The MTBF is predicated and calculated based on “Telcordia Technologies Special Report, SR-332, Issue 2” method.

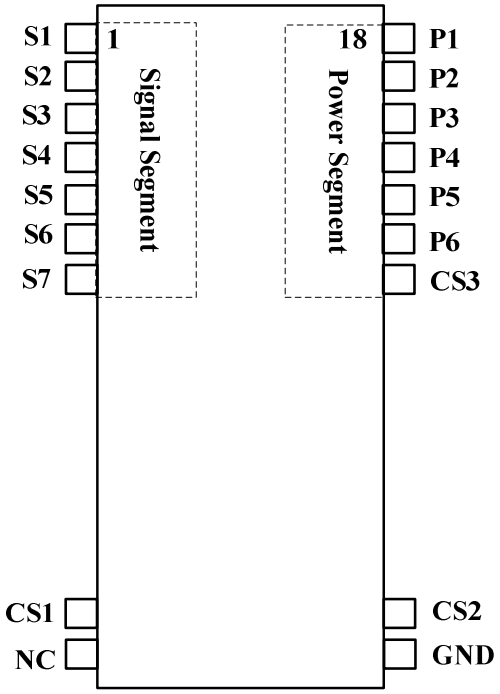
3.6 Certification and Compliance

SDC4 complies with the following standards:

- CE
- FCC
- RoHS
- MIL-STD-202 and MIL-STD-810

4. Pin Assignments

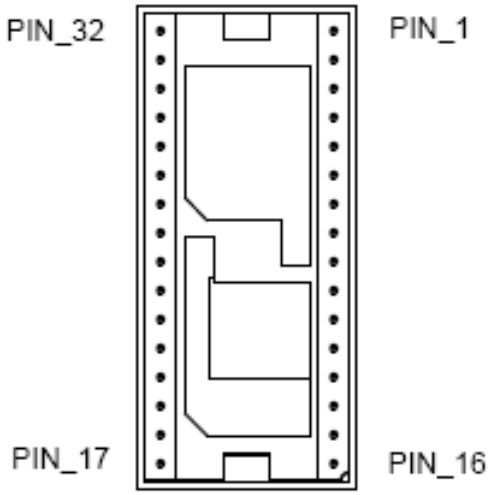
4.1 18 pins (7x2 + 2x2)



Pin	Name	Type*	Pin	Name	Type*
1	S1	GND	10	GND	GND
2	S2	RX+	11	CS2	Data Act.
3	S3	RX-	12	CS3	RS/WP
4	S4	GND	13	P6	NA
5	S5	TX-	14	P5	NA
6	S6	TX+	15	P4	NA
7	S7	GND	16	P3	NA
8	CS1	PHY RDY	17	P2	GND
9	NC	-	18	P1	VCC3.3

*RS: Reserved

4.2 32 pins (16x2)



Pin	Name	Type*	Pin	Name	Type*
1	S1	GND	17	GND	GND
2	S2	RX+	18	CS7	Data Act.
3	S3	RX-	19	CS8	RS
4	S4	GND	20	CS9	RS
5	S5	TX-	21	CS10	RS
6	S6	TX+	22	CS11	RS
7	S7	GND	23	CS12	RS
8	NC	-	24	CS13	RS
9	GND	GND	25	CS14	RS
10	CS1	RS1	26	CS15	RS/WP
11	CS2	RS	27	P6	NA
12	CS3	RS	28	P5	NA
13	CS4	RS	29	P4	NA
14	CS5	RS	30	P3	NA
15	CS6	PHY RDY	31	P2	GND
16	NC	-	32	P1	VCC3.3

*RS: Reserved

5. Flash Management

5.1 Error Correction/Detection

SDC implements a hardware ECC scheme, based on the BCH algorithm. It can detect and correct up to 16 bits or 24 bits error in 512 bytes.

5.2 Bad Block Management

Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. When host performs program/erase command on a block, bad block may appear in Status Register. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, block mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

5.3 Wear Leveling

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Wear leveling is an important mechanism that level out the wearing of blocks so that the wearing-down of blocks can be almost evenly distributed. This will increase the lifespan of SSDs. Commonly used wear leveling types are Static and Dynamic.

5.4 Power Failure Management

Power Failure Management plays a crucial role when experiencing unstable power supply. Power disruption may occur when users are storing data into the SSD. In this urgent situation, the controller would run multiple write-to-flash cycles to store the metadata for later block rebuilding. This urgent operation requires about several milliseconds to get it done. At the next power up, the firmware will perform a status tracking to retrieve the mapping table and resume previously programmed NAND blocks to check if there is any incompleteness of transmission.

5.5 ATA Secure Erase

AATA Secure Erase is an ATA disk purging command currently embedded in most of the storage drives. Defined in ATA specifications, (ATA) Secure Erase is part of Security Feature Set that allows storage drives to erase all user data areas. The erase process usually runs on the firmware level as most of the ATA-based storage media currently in the market are built-in with this command. ATA Secure Erase can securely wipe out the user data in the drive and protects it from malicious attack.

5.6 S.M.A.R.T.

S.M.A.R.T. is an abbreviation for Self-Monitoring, Analysis and Reporting Technology, a self-monitoring system that provides indicators of drive health as well as potential disk problems. It serves as a warning for users from unscheduled downtime by monitoring and displaying critical drive information. Ideally, this should allow taking proactive actions to prevent drive failure and make use of S.M.A.R.T. information for future product development reference.

Apacer devices use the standard SMART command B0h to read data out from the drive to activate our S.M.A.R.T. feature that complies with the ATA/ATAPI specifications. S.M.A.R.T. Attribute IDs shall include initial bad block count, total later bad block count, maximum erase count, average erase count, power on hours and power cycle. When the S.M.A.R.T. Utility running on the host, it analyzes and reports the disk status to the host before the device reaches in critical condition.

Note: attribute IDs may vary from product models due to various solution design and supporting capabilities.

6. Software Interface

6.1 Command Set

This section defines the software requirements and the format of the commands the host sends to the SATA-Disk Chip (SDC). Commands are issued to the SDC by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command register.

Table 5-1: Command set (1 of 2)

Command	Code
Check-Power-Mode	E5H
Execute-Drive-Diagnostic	90H
Flush-Cache	E7H
Identify-Drive	ECH
Idle	E3H
Idle-Immediate	E1H
Initialize-Drive-Parameters	91H
Read-DMA	C8H or C9H
Read-Multiple	C4H
Read-Sector(s)	20H or 21H
Read-Verify-Sector(s)	40H or 41H
Recalibrate	10H
Security-Disable-Password	F6H
Security-Erase-Prepare	F3H
Security-Erase-Unit	F4H
Security-Freeze-Lock	F5H
Security-Set-Password	F1H
Security-Unlock	F2H
Seek	7XH
Set-Features	EFH

Table 5-1: Command set (2 of 2)

Command	Code
Set-Multiple-Mode	C6H
Sleep	E6H
SMART	B0H
Standby	E2H
Standby-Immediate	E0H
Write-DMA	CAH
Write-Multiple	C5H
Write-Sector(s)	30H

7. Electrical Specification

Table 7-1: Operating range

Range	Ambient Temperature	3.3V (typical)
Standard	0℃ to +70℃	3.135 ~ 3.465V
Extended Temperature	-40℃ to 85℃	

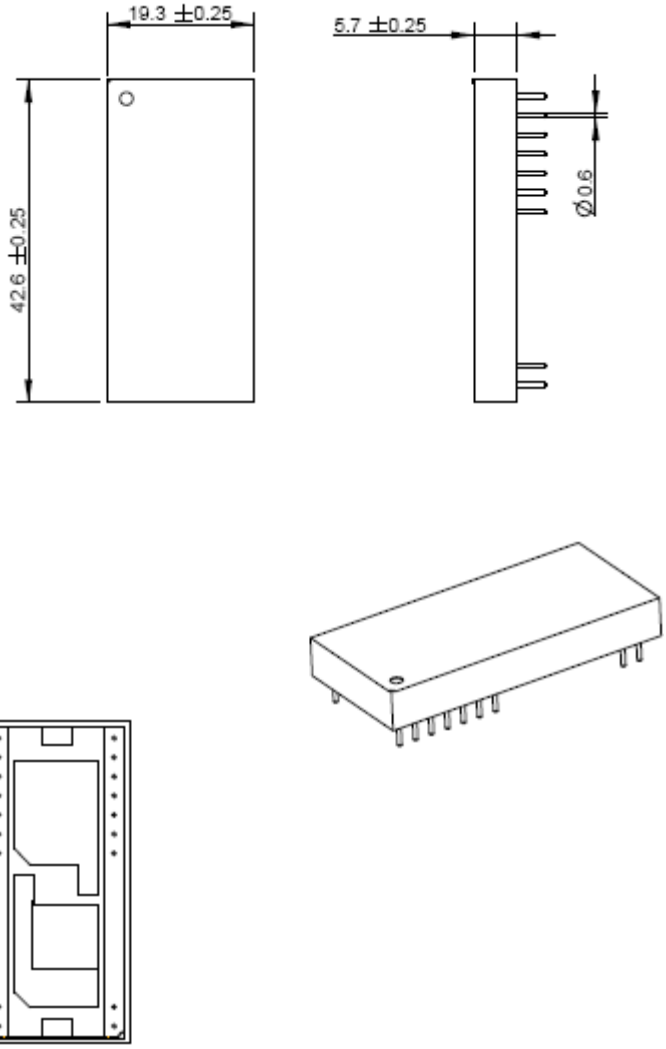
Table 7-2: Typical power consumption

Capacity / Modes	1 GB	2 GB	4 GB	8 GB	16 GB	32 GB
Active (mA)	200	271	320	320	340	355
Idle (mA)	100	110	110	113	120	110

Note: Results may differ from various flash configurations or host system settings.

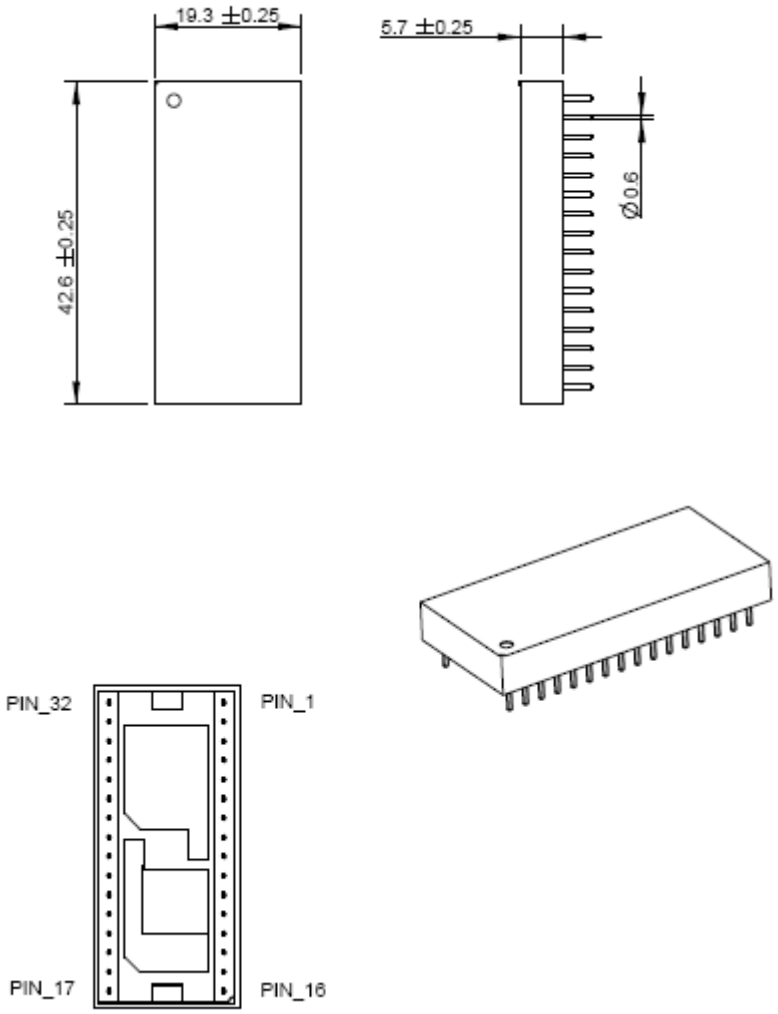
8. Physical Characteristics

18 Pins (7x2, 2x2)



Unit: mm
Tolerance: ± 0.25

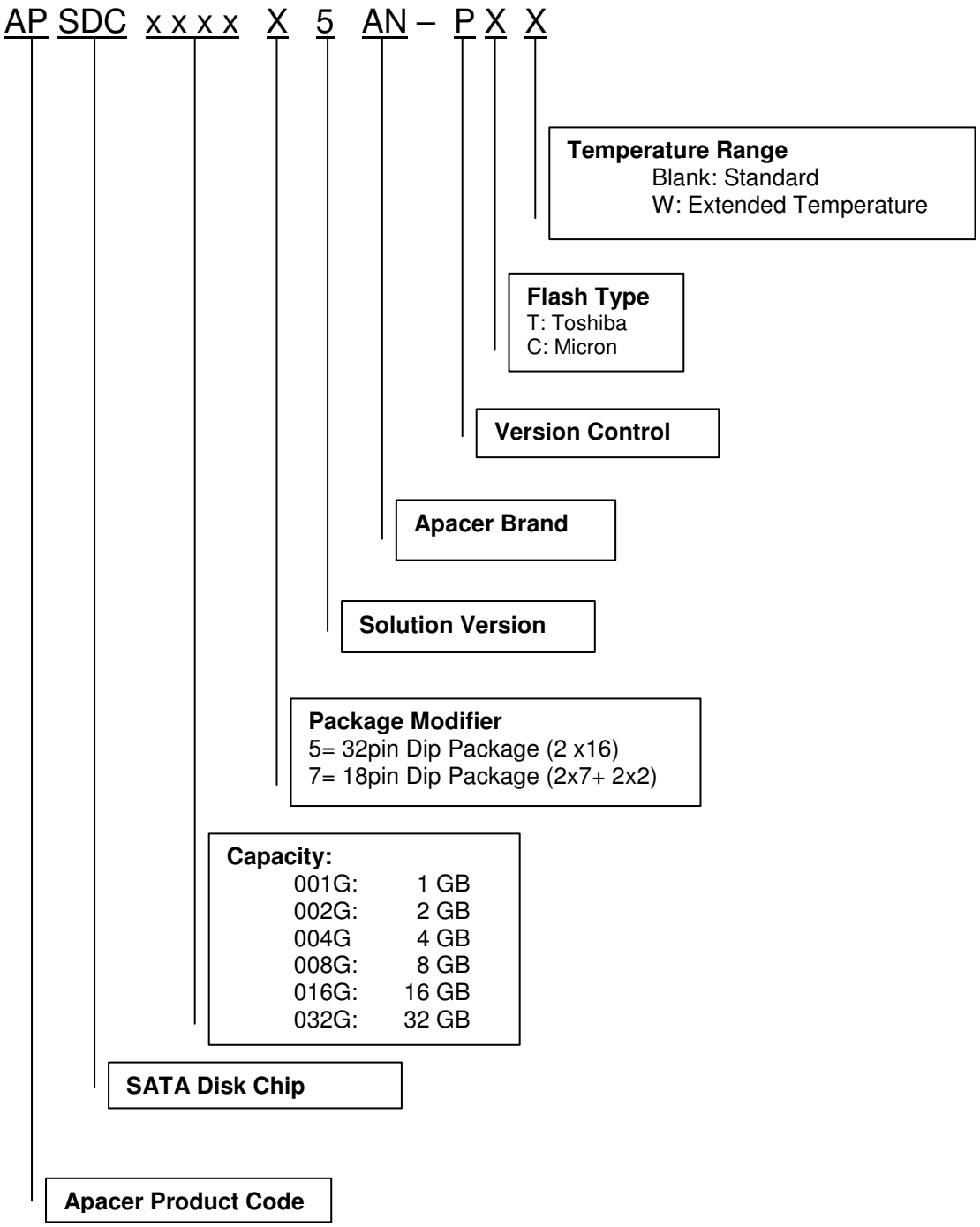
32 Pins (16x2)



Unit: mm
Tolerance: ± 0.25

9. Product Ordering Information

9.1 Product Code Designations



9.2 Valid Combinations

9.2.1 SDC4 32pin (2 x 16 pin)

Capacity	Standard	Extended Temperature
1GB	APSDC001G55AN-PT	APSDC001G55AN-PTW
2GB	APSDC002G55AN-PT	APSDC002G55AN-PTW
4GB	APSDC004G55AN-PT	APSDC004G55AN-PTW
8GB	APSDC008G55AN-PT	APSDC008G55AN-PTW
16GB	APSDC016G55AN-PC	APSDC016G55AN-PCW
32GB	APSDC032G55AN-PC	APSDC032G55AN-PCW

9.2.2 SDC4 18pin (2x7 + 2x2pin)

Capacity	Standard	Extended Temperature
1GB	APSDC001G75AN-PT	APSDC001G75AN-PTW
2GB	APSDC002G75AN-PT	APSDC002G75AN-PTW
4GB	APSDC004G75AN-PT	APSDC004G75AN-PTW
8GB	APSDC008G75AN-PT	APSDC008G75AN-PTW
16GB	APSDC016G75AN-PC	APSDC016G75AN-PCW
32GB	APSDC032G75AN-PC	APSDC032G75AN-PCW

Note: Please consult with Apacer sales representatives for availabilities.

10. Appendix – Notes for the Warranty

Soldering (both hand and SMT reflow) the SDC will void the warranty.

Revision History

Revision	Date	Description	Remark
1.0	12/14/2011	Official release	
1.1	1/16/2012	Revised capacity information	
1.2	03/23/2012	Revised S.M.A.R.T information	
1.3	09/28/2012	Updated Product Ordering Information due to firmware upgrade	
1.4	10/31/2012	Added 1GB capacity	
1.5	04/10/2013	Added warranty note	
1.6	05/17/2013	Updated Product Ordering Information due to firmware upgrade	

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