Apacer

RoHS Compliant

# PCI Express Flash Drive

## PV120-M280 Product Specifications


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# Specifications Overview:

- **PCIe Interface**
  - Compliant with NVMe 1.2
  - Compatible with PCIe Gen3 x2 interface
- **Capacity**
  - Single side: 120, 240 GB
  - Double side: 480, 960 GB
- **Performance***
  - Interface burst read/write: 2 GB/sec
  - Sequential read: up to 1,710 MB/sec
  - Sequential write: up to 1,065 MB/sec
  - Random read (4K): up to 157,000 IOPS
  - Random write (4K): up to 182,000 IOPS
- **Flash Management**
  - Low-Density Parity-Check (LDPC) Code
  - Global Wear Leveling
  - Flash bad-block management
  - Flash Translation Layer: Page Mapping
  - S.M.A.R.T.
  - Power Failure Management
  - TRIM
  - Hyper Cache Technology
  - Over-Provisioning
  - DataRAID™
- **Security**
  - Trusted Computing Group (TCG) Opal 2.0 (optional)
  - AES 256-bit hardware encryption
- **NAND Flash Type:** 3D TLC (BiCS3)
- **MTBF:** >3,000,000 hours
- **Endurance (in drive writes per day : DWPD)**
  - 120 GB: 1.49 DWPD
  - 240 GB: 1.62 DWPD
  - 480 GB: 1.27 DWPD
  - 960 GB: 0.95 DWPD
- **Temperature Range**
  - Operating:
    Standard: 0°C to 70°C
    Wide: -40°C to 85°C
  - Storage: -40°C to 100°C
- **Supply Voltage**
  - 3.3 V ± 5%
- **Power Consumption***
  - Active mode: 1,275 mA
  - Idle mode: 150 mA
- **Connector Type**
  - 75-pin M.2 module pinout
- **Power Management**
  - Supports APST
  - Supports ASPM L1.2
- **DRAM Cache for Enhanced Random Performance**
- **Reliability**
  - Thermal Sensor
  - Thermal Throttling
  - End-to-End Data Protection
  - CoreGlacier™**
- **Form Factor**
  - M.2 2280 single side, B+M key: 120, 240 GB
  - M.2 2280 double side, B+M key: 480, 960 GB
  - Dimensions:
    Standard temp.: 80.00 x 22.00 x 3.38, unit: mm
    Wide temp.: 80.00 x 22.00 x 4.10, unit: mm
  - Net Weight:
    Standard temp.: 7.3 g ± 5%
    Wide temp.: 9.8 g ± 5%
- **LED Indicators for Drive Behavior**
- **RoHS Compliant**

*Varies from capacities. The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings.
**Only supported on wide temperature series

# Table of Contents

# 1. General Descriptions

Apacer PV120-M280 (M.2 2280) is the next generation modularized Solid State Drive (SSD) with the shape of all new M.2 form factor, aimed to be the more suitable for mobile and compact computers with standard width at only 22.00 mm. PV120-M280 appears in M.2 2280 mechanical dimensions and is believed to be the leading add-in storage solution for future host computing systems.

The M.2 SSD is designed with PCIe-based connector pinouts, providing full compliance with the latest PCIe Gen3 x2 interface specifications. Aside from PCIe compliance, PV120-M280 delivers exceptional performance and power efficiency. On the other hand, the extreme thin and light form factor makes PV120-M280 the ideal choice for mobile computing systems, which appears to be the trend in near future.

Regarding reliability, PV120-M280 is built with a powerful PCIe controller that supports on-the-module ECC as well as efficient wear leveling scheme. In terms of power efficiency, PV120-M280 is compliant with PCIe Gen3 x2 interface standard so that it can operate on power management modes, which greatly save on power consumption.

In terms of security, Advanced Encryption Standard (AES) and Trusted Computing Group (TCG) Opal ensure data security and provide users with a peace of mind knowing their data is safeguarded against unauthorized use at all times. Furthermore, with End-to-End Data Protection, data integrity can be assured at multiple points in the path to enable reliable delivery of data transfers.

# 2. Functional Block

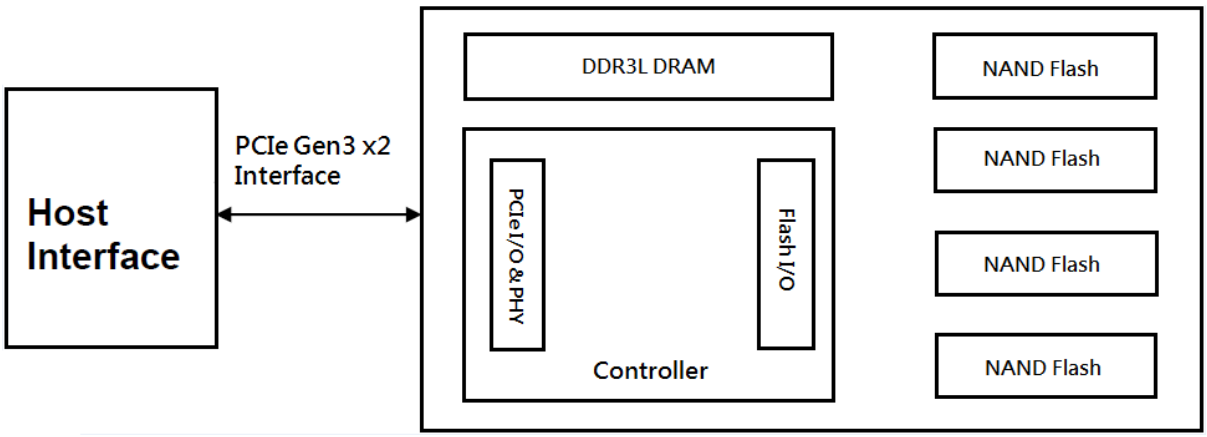



**Figure 2-1** Functional Block Diagram

# 3. Pin Assignments

This connector does not support hot plug capability. There are a total of 75 pins. 12 pin locations are used for mechanical key locations; this allows such a module to plug into both Key B and Key M connectors.

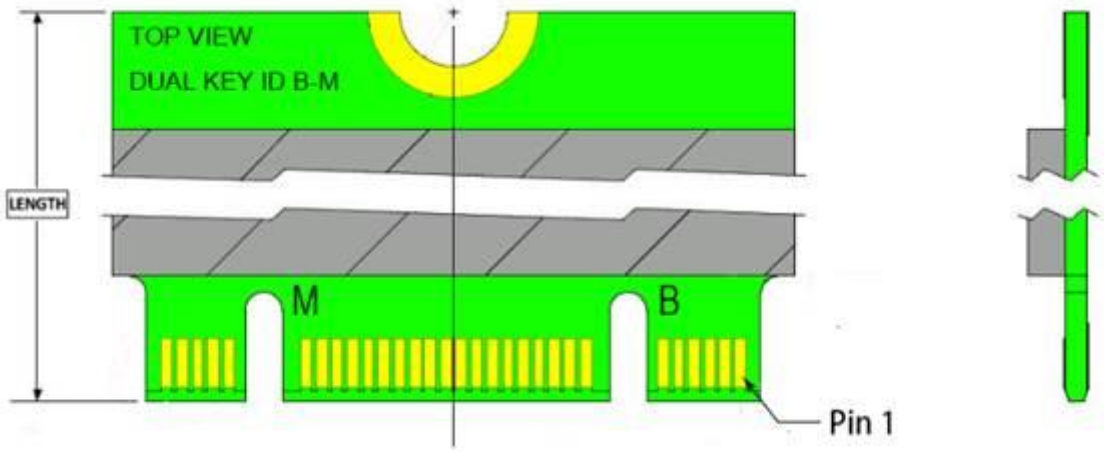



**Table 3-1** Pin Assignments

| Pin | Type | Description |
|---|---|---|
| 1 | GND | CONFIG_3 = GND |
| 2 | 3.3V | 3.3V source |
| 3 | GND | Ground |
| 4 | 3.3V | 3.3V source |
| 5 | N/C | No connect |
| 6 | N/C | No connect |
| 7 | N/C | No connect |
| 8 | N/C | No connect |
| 9 | N/C | No connect |
| 10 | DAS/DSS | Device Activity Signal/Disable Staggered Spin-up |
| 11 | N/C | No connect |
| 12 | (removed for key) | Mechanical notch B |
| 13 | (removed for key) | Mechanical notch B |
| 14 | (removed for key) | Mechanical notch B |
| 15 | (removed for key) | Mechanical notch B |
| 16 | (removed for key) | Mechanical notch B |
| 17 | (removed for key) | Mechanical notch B |
| 18 | (removed for key) | Mechanical notch B |
| 19 | (removed for key) | Mechanical notch B |
| 20 | N/C | No connect |
| 21 | GND | CONFIG_0=GND |
| 22 | N/C | No connect |
| 23 | N/C | No connect |
| 24 | N/C | No connect |
| 25 | N/C | No connect |
| 26 | N/C | No connect |
| 27 | GND | Ground |
| 28 | N/C | No connect |
| 29 | PETn1 | PCIe TX Differential signal defined by the PCI Express M.2 spec |
| 30 | N/C | No connect |
| 31 | PETp1 | PCIe TX Differential signal defined by the PCI Express M.2 spec |

**Table 3-1** Pin Assignments

| Pin | Type | Description |
|---|---|---|
| 32 | N/C | No connect |
| 33 | GND | Ground |
| 34 | N/C | No connect |
| 35 | PERn1 | PCIe RX Differential signal defined by the PCI Express M.2 spec |
| 36 | N/C | No connect |
| 37 | PERp1 | PCIe RX Differential signal defined by the PCI Express M.2 spec |
| 38 | N/C | No connect |
| 39 | GND | Ground |
| 40 | SMB_CLK (I/O)(0/1.8V) | SMBus Clock; Open Drain with pull-up on platform |
| 41 | PETn0 | PCIe TX Differential signal defined by the PCI Express M.2 spec |
| 42 | SMB_DATA (I/O)(0/1.8V) | SMBus Data; Open Drain with pull-up on platform. |
| 43 | PETp0 | PCIe TX Differential signal defined by the PCI Express M.2 spec |
| 44 | ALERT#(O) (0/1.8V) | Alert notification to master; Open Drain with pull-up on platform; Active low. |
| 45 | GND | Ground |
| 46 | N/C | No connect |
| 47 | PERn0 | PCIe RX Differential signal defined by the PCI Express M.2 spec |
| 48 | N/C | No connect |
| 49 | PERp0 | PCIe RX Differential signal defined by the PCI Express M.2 spec |
| 50 | PERST#(I)(0/3.3V) | PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification. |
| 51 | GND | Ground |
| 52 | CLKREQ#(I/O)(0/3.3V) | Clock Request is a reference clock request signal as defined by the PCIe Mini CEM specification; Also used by L1 PM Sub-states. |
| 53 | REFCLKn | PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec. |
| 54 | PEWAKE#(I/O)(0/3.3V) | PCIe PME Wake.<br>Open Drain with pull up on platform; Active Low. |
| 55 | REFCLKp | PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec. |
| 56 | Reserved for MFG DATA | Manufacturing Data line. Used for SSD manufacturing only.<br>Not used in normal operation.<br>Pins should be left N/C in platform Socket. |
| 57 | GND | Ground |
| 58 | Reserved for MFG CLOCK | Manufacturing Clock line. Used for SSD manufacturing only.<br>Not used in normal operation.<br>Pins should be left N/C in platform Socket. |
| 59 | (removed for key) | Mechanical notch M |
| 60 | (removed for key) | Mechanical notch M |
| 61 | (removed for key) | Mechanical notch M |
| 62 | (removed for key) | Mechanical notch M |
| 63 | (removed for key) | Mechanical notch M |
| 64 | (removed for key) | Mechanical notch M |
| 65 | (removed for key) | Mechanical notch M |
| 66 | (removed for key) | Mechanical notch M |
| 67 | NC | No connect (used for other purposes) |
| 68 | SUSCLK(32KHz) (I)(0/3.3V) | 32.768 kHz clock supply input that is provided by the platform chipset to reduce power and cost for the module. |
| 69 | NC | CONFIG_1 = No connect |
| 70 | 3.3V | Supply pin, 3.3V |
| 71 | GND | Ground |
| 72 | 3.3V | Supply pin, 3.3V |
| 73 | GND | Ground |
| 74 | 3.3V | Supply pin, 3.3V |
| 75 | CONFIG_2 | Ground |

# 4. Product Specifications

## 4.1 Capacity

Capacity specifications of PV120-M280 are available as shown in Table 4-1. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

**Table 4-1** Capacity Specifications

| Capacity | Total bytes* | Cylinders | Heads | Sectors | Total LBA |
|---|---|---|---|---|---|
| 120 GB | 120,034,123,776 | 16,383 | 16 | 63 | 234,441,648 |
| 240 GB | 240,057,409,536 | 16,383 | 16 | 63 | 468,862,128 |
| 480 GB | 480,103,981,056 | 16,383 | 16 | 63 | 937,703,088 |
| 960 GB | 960,197,124,096 | 16,383 | 16 | 63 | 1,875,385,008 |

*Display of total bytes varies from file systems, which means not all of the bytes can be used for storage.
**Notes: 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.
LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

## 4.2 Performance

Performance of PV120-M280 is listed below in Table 4-2.

**Table 4-2** Performance Specifications

| Performance \ Capacity | 120 GB | 240 GB | 480 GB | 960 GB |
|---|---|---|---|---|
| **Sequential Read* (MB/s)** | 1,515 | 1,695 | 1,710 | 1,710 |
| **Sequential Write* (MB/s)** | 490 | 950 | 1,055 | 1,065 |
| **Random Read IOPS** (4K)** | 82,000 | 129,000 | 157,000 | 147,000 |
| **Random Write IOPS** (4K)** | 105,000 | 165,000 | 182,000 | 174,000 |

Note:
Results may differ from various flash configurations or host system setting.
*Sequential performance is based on CrystalDiskMark 5.2.1 with file size 1,000MB.
**Random performance measured using IOMeter with Queue Depth 32.

## 4.3 Environmental Specifications

Environmental specifications of PV120-M280 are shown in Table 4-3.

**Table 4-3** Environmental Specifications

| Environment | Specifications |
|---|---|
| Temperature | 0°C to 70°C (Standard); -40°C to 85°C (Wide) |
| | -40°C to 100°C (Non-operating) |
| Vibration | Operation: 7.69 (Grms), 20~2000(Hz)/random (compliant with MIL-STD-810G) |
| | Non-operation: 4.02 (Grms), 15~2000(Hz)/random (compliant with MIL-STD-810G) |
| Shock | Operation: Acceleration, 50(G)/11ms/half sine (compliant with MIL-STD-202G) |
| | Non-operation: Acceleration,1,500(G)/0.5(ms)/half sine (compliant with MIL-STD-883K) |

Note: Shock and Vibration specifications are subject to change without notice.

## 4.4 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in PV120-M280. The prediction result for PV120-M280 is more than 3,000,000 hours.

Note: The MTBF is predicated and calculated based on “Telcordia Technologies Special Report, SR-332, Issue 3” method.

## 4.5 Certification and Compliance

PV120-M280 complies with the following standards:

- FCC
- CE
- RoHS
- MIL-STD-810

## 4.6 Endurance

The endurance of a storage device is predicted by Drive Writes Per Day based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

**Table 4-4** Drive Writes Per Day

| Capacity | Drive Writes Per Day |
|---|---|
| 120 GB | 1.49 |
| 240 GB | 1.62 |
| 480 GB | 1.27 |
| 960 GB | 0.95 |

Note:

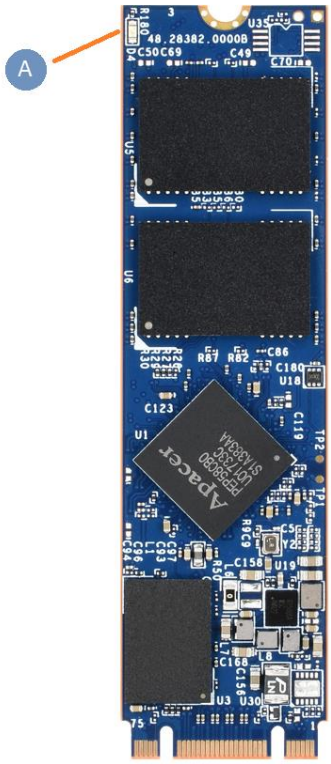
- This estimation complies with JEDEC random client workload.
- Flash vendor guaranteed 3D NAND TLC P/E cycle: 3K
- WAF may vary from capacity, flash configurations and writing behavior on each platform.
- 1 Terabyte = 1,024GB
- DWPD (Drive Writes Per Day) is calculated based on the number of times that user overwrites the entire capacity of an SSD per day of its lifetime during the warranty period. (3D NAND TLC warranty: 2 years)

## 4.7 LED Indicator Behavior

The behavior of the PV120-M280 LED indicators is described in Table 4-5.

**Table 4-5** LED Behavior

| Location | LED | Description |
|---|---|---|
| LED A | DAS | LED blinks when the drive is being accessed |



# 5. Flash Management

## 5.1 Error Correction/Detection

PV120-M280 implements a hardware ECC scheme, based on the Low Density Parity Check (LDPC). LDPC is a class of linear block error correcting code which has apparent coding gain over BCH code because LDPC code includes both hard decoding and soft decoding algorithms. With the error rate decreasing, LDPC can extend SSD endurance and increase data reliability while reading raw data inside a flash chip.

## 5.2 Bad Block Management

Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, page mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

## 5.3 Global Wear Leveling

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Global wear leveling is an important mechanism that levels out the wearing of all blocks so that the wearing-down of all blocks can be almost evenly distributed. This will increase the lifespan of SSDs.

## 5.4 Flash Translation Layer – Page Mapping

Page mapping is an advanced flash management technology whose essence lies in the ability to gather data, distribute the data into flash pages automatically, and then schedule the data to be evenly written. Page-level mapping uses one page as the unit of mapping. The most important characteristic is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different sizes of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. Thus, page mapping is adopted to increase random access speed and improve SSD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

## 5.5 Power Failure Management

Power Failure Management plays a crucial role when power supply becomes unstable. Power disruption may occur when users are storing data into the SSD, leading to instability in the drive. However, with Power Failure Management, a firmware protection mechanism will be activated to scan pages and blocks once power is resumed. Valid data will be transferred to new blocks for merging and the mapping table will be rebuilt. Therefore, data reliability can be reinforced, preventing damage to data stored in the NAND Flash.

Note: The controller unit of this product model is designed with a DRAM as a write cache for improved performance and data efficiency. Though unlikely to happen in most cases, the data cached in the volatile DRAM might be potentially affected if a sudden power loss takes place before the cached data is flushed into non-volatile NAND flash memory.

## 5.6 TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks all the time.

## 5.7 Hyper Cache Technology

Apacer proprietary Hyper Cache technology uses a portion of the available capacity as SLC (1bit-per-cell) NAND flash memory, called Hyper cache mode. When data is written to SSD, the firmware will direct the data to Hyper Cache mode, providing excellent performance to handle various scenarios in industrial use.

## 5.8 Over-Provisioning

Over-Provisioning (OP) is a certain portion of the SSD capacity exclusively for increasing Garbage Collection (GC) efficiency, especially when the SSD is filled to full capacity or performs a heavy mixed-random workload. OP has the advantages of providing extended life expectancy, reliable data integrity, and high sustained write performance.

## 5.9 DataRAID™

Apacer's DataRAID algorithm applies an additional level of protection and error-checking. Using this algorithm, a certain amount of space is given over to aggregating and resaving the existing parity data used for error checking. So, in the event that data becomes corrupted, the parity data can be compared to the existing uncorrupted data and the content of the corrupted data can be rebuilt.

# 6. Security & Reliability Features

## 6.1 Advanced Encryption Standard

Advanced Encryption Standard (AES) is a specification for the encryption of electronic data. AES has been adopted by the U.S. government since 2001 to protect classified information and is now widely implemented in embedded computing applications. The AES algorithm used in software and hardware is symmetric so that encrypting/decrypting requires the same encryption key. Without the key, the encrypted data is inaccessible to ensure information security.

Notably in flash memory applications, AES 256-bit hardware encryption is the mainstream to protect sensitive or confidential data. The hardware encryption provides better performance, reliability, and security than software encryption. It uses a dedicated processor, which is built inside the controller, to process the encryption and decryption. This enormously shortens the processing time and makes it efficient.

## 6.2 TCG Opal (optional)

Developed by the Trusted Computing Group (TCG), an organization whose members work together to formulate industry standards, Opal is a set of security specifications used for applying hardware-based encryption to storage devices.

Hardware encryption has many advantages. First of all, it transfers the computational load of the encryption process to dedicated processors, reducing the stress on the host system's CPU. In addition, storage devices complying with Opal specifications are self-encryption devices. Opal specifications also feature boot authentication. When the drive is being accessed, the shadow MBR will request the drive password at boot. The drive will only unlock and decrypt if the correct password is supplied. The other feature is LBA-specific permissions. Users are assigned different permissions for LBA ranges created by the device administrator. Each LBA range is password-protected and can only be accessed by users with the correct key to perform permitted actions (read/write/erase).

## 6.3 Thermal Sensor

Apacer Thermal Sensor is a digital temperature sensor with serial interface. By using designated pins for transmission, storage device owners are able to read temperature data.

## 6.4 Thermal Throttling

Thermal throttling can monitor the temperature of the SSD equipped with a built-in thermal sensor via S.M.A.R.T. commands. This method can ensure the temperature of the device stays within temperature limits by drive throttling, i.e. reducing the speed of the drive when the device temperature reaches the threshold level, so as to prevent overheating, guarantee data reliability, and prolong product lifespan. When the temperature exceeds the maximum threshold level, thermal throttling will be triggered to reduce performance step by step to prevent hardware components from being damaged. Performance is only permitted to drop to the extent necessary for recovering a stable temperature to cool down the device’s temperature. Once the temperature decreases to the minimum threshold value, transfer speeds will rise back to its optimum performance level.

## 6.5 End-to-End Data Protection

End-to-End Data Protection is a feature implemented in Apacer SSD products that extends error control to cover the entire path from the host computer to the drive and back, and that ensures data integrity at multiple points in the path to enable reliable delivery of data transfers. Unlike ECC which does not exhibit the ability to determine the occurrence of errors throughout the process of data transmission, End-to-End Data Protection allows SSD controller to identify an error created anywhere in the path and report the error to the host computer before it is written to the drive. This error-checking and error-reporting mechanism therefore guarantees the trustworthiness and reliability of the SSD.

## 6.6 CoreGlacier™

In many applications, SSDs are subject to challenging conditions. If the working environment is already hot, and the SSD's operation causes it to increase in temperature as well, the result could be damage to the hardware or corrupted data. In cases like this, leading industrial manufacturers know to turn to Apacer. Apacer developed CoreGlacier, a heatsink that distributes dissipation in isolated components with no thermal diffusion, to prevent heat-related damage from occurring.

# 7. Software Interface

## 7.1 Command Set

Table 7-1 summarizes the commands supported by PV120-M280.

**Table 7-1** Admin Commands

| Opcode | Command Description |
|---|---|
| 00h | Delete I/O Submission Queue |
| 01h | Create I/O Submission Queue |
| 02h | Get Log Page |
| 04h | Delete I/O Completion Queue |
| 05h | Create I/O Completion Queue |
| 06h | Identify |
| 08h | Abort |
| 09h | Set Features |
| 0Ah | Get Features |
| 0Ch | Asynchronous Event Request |
| 10h | Firmware Activate |
| 11h | Firmware Image Download |

**Table 7-2** Admin Commands – NVM Command Set Specific

| Opcode | Command Description |
|---|---|
| 80h | Format NVM |
| 81h | Security Send* |
| 82h | Security Receive* |

*Only available on products with TCG Opal support.

**Table 7-3** NVM Commands

| Opcode | Command Description |
|---|---|
| 00h | Flush |
| 01h | Write |
| 02h | Read |
| 04h | Write Uncorrectable |
| 05h | Compare |
| 08h | Write Zeroes |
| 09h | Dataset Management |

## 7.2 S.M.A.R.T.

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

**Table 7-5** SMART (02h)

| Byte | Length | Description |
|---|---|---|
| 0 | 1 | Critical Warning |
| 1-2 | 2 | Composite Temperature |
| 3 | 1 | Available Spare |
| 4 | 1 | Available Spare Threshold |
| 5 | 1 | Percentage Used |
| 6-31 | 26 | Reserved |
| 32-47 | 16 | Data Units Read |
| 48-63 | 16 | Data Units Written |
| 64-79 | 16 | Host Read Commands |
| 80-95 | 16 | Host Write Commands |
| 96-111 | 16 | Controller Busy Time |
| 112-127 | 16 | Power Cycles |
| 128-143 | 16 | Power On Hours |
| 144-159 | 16 | Unsafe Shutdowns |
| 160-175 | 16 | Media and Data Integrity Errors |
| 176-191 | 16 | Number of Error Information Log Entries |
| 192-195 | 4 | Warning Composite Temperature Time |
| 196-199 | 4 | Critical Composite Temperature Time |
| 200-201 | 2 | Temperature Sensor 1 |
| 202-203 | 2 | Temperature Sensor 2 |
| 204-205 | 2 | Temperature Sensor 3 |
| 206-207 | 2 | Temperature Sensor 4 |
| 208-209 | 2 | Temperature Sensor 5 |
| 210-211 | 2 | Temperature Sensor 6 |
| 212-213 | 2 | Temperature Sensor 7 |
| 214-215 | 2 | Temperature Sensor 8 |
| 216-511 | 296 | Reserved |

**Table 7-5** SMART (C0h)

| Byte | Length | Description |
|---|---|---|
| 2-255 | 254 | Reserved |
| 256-257 | 2 | SSD Protect Mode |
| 258-261 | 4 | ECC Fail Count |
| 262-273 | 12 | Reserved |
| 274-277 | 4 | Total Later Bad Block Count |
| 278-281 | 4 | Max Erase Count |
| 282-285 | 4 | Average Erase Count |
| 286-289 | 4 | Program Fail Count |
| 290-293 | 4 | Erase Fail Count |
| 294-301 | 8 | FlashWriteSector |
| 302-511 | 210 | Reserved |

# 8. Electrical Specifications

## 8.1 Operating Voltage

Table 8-1 lists the supply voltage for PV120-M280.

**Table 8-1** Operating Range

| Item | Range |
|---|---|
| Supply Voltage | 3.3V ± 5% |

## 8.2 Power Consumption

Table 8-2 lists the power consumption for PV120-M280.

**Table 8-2** Power Consumption

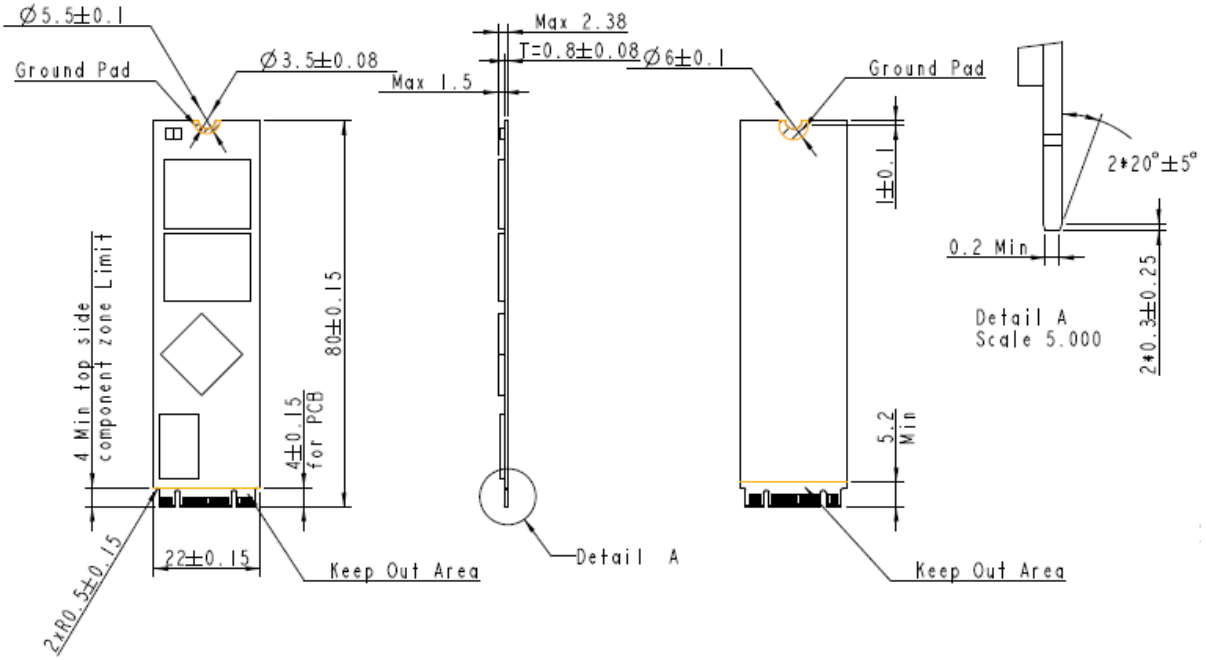
| Capacity / Mode | 120 GB | 240 GB | 480 GB | 960 GB |
|---|---|---|---|---|
| **Active (mA)** | 885 | 1,005 | 1,040 | 1,275 |
| **Idle (mA)** | 140 | 140 | 140 | 150 |

Note:
*All values are typical and may vary depending on flash configurations or host system settings.
**Active power is an average power measurement performed using CrystalDiskMark with 128KB sequential read/write transfers.

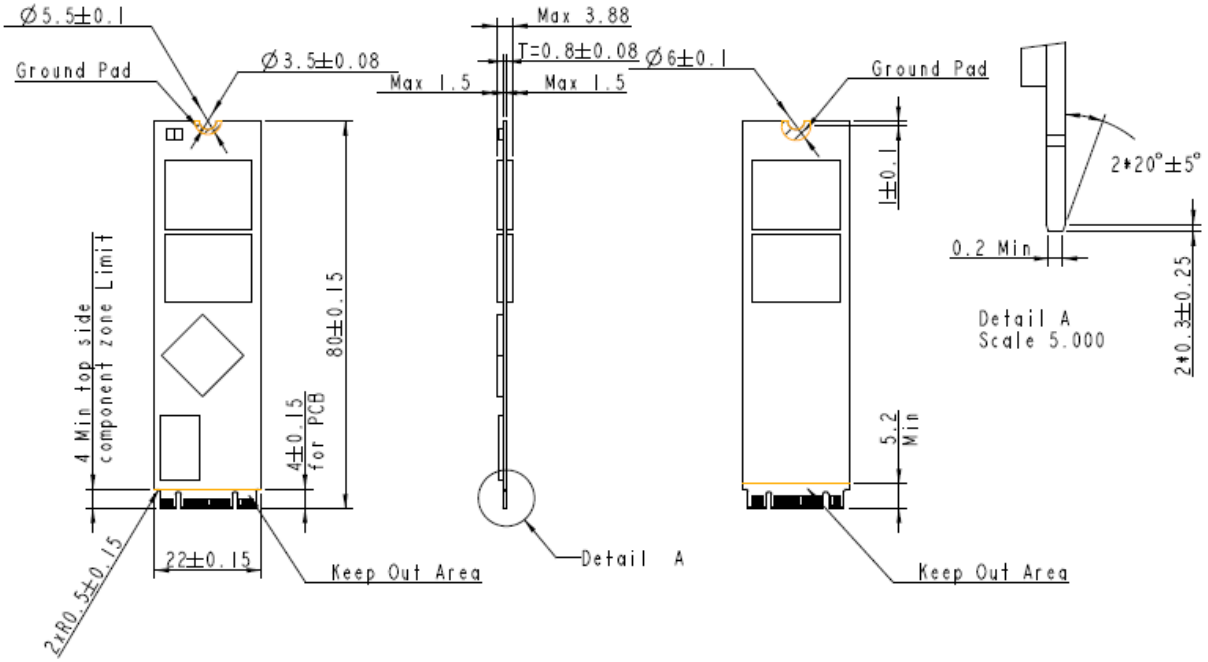
# 9. Physical Characteristics

## 9.1 Standard Temperature

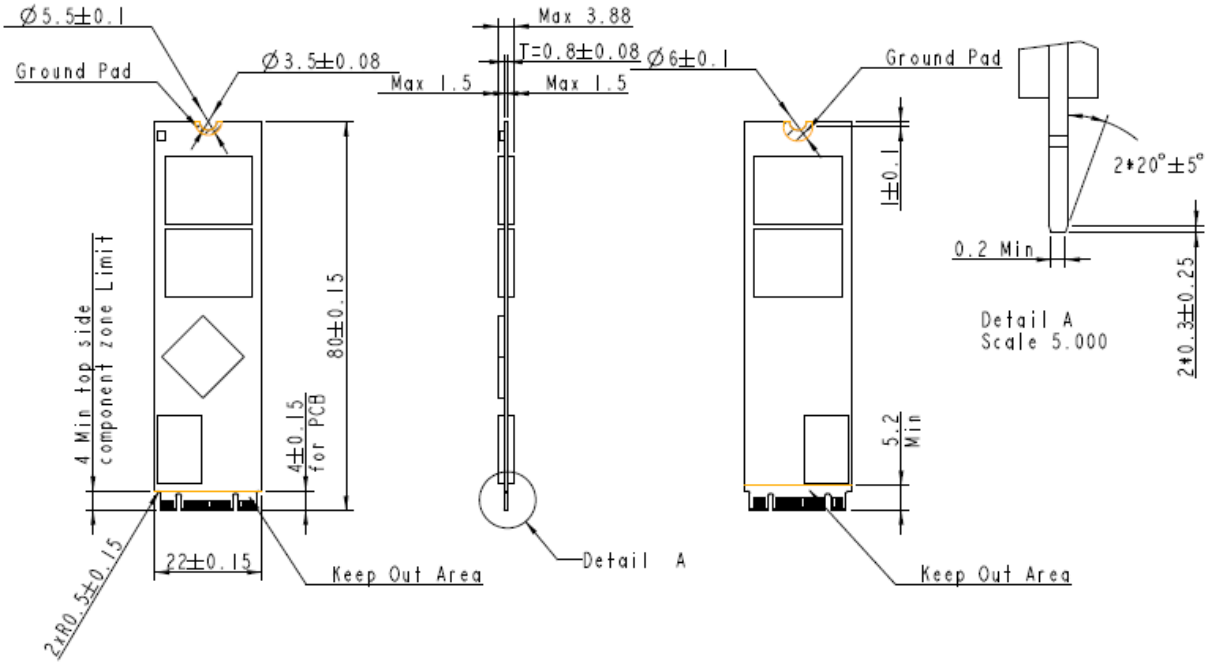
### 9.1.1 120-240GB




### 9.1.2 480GB

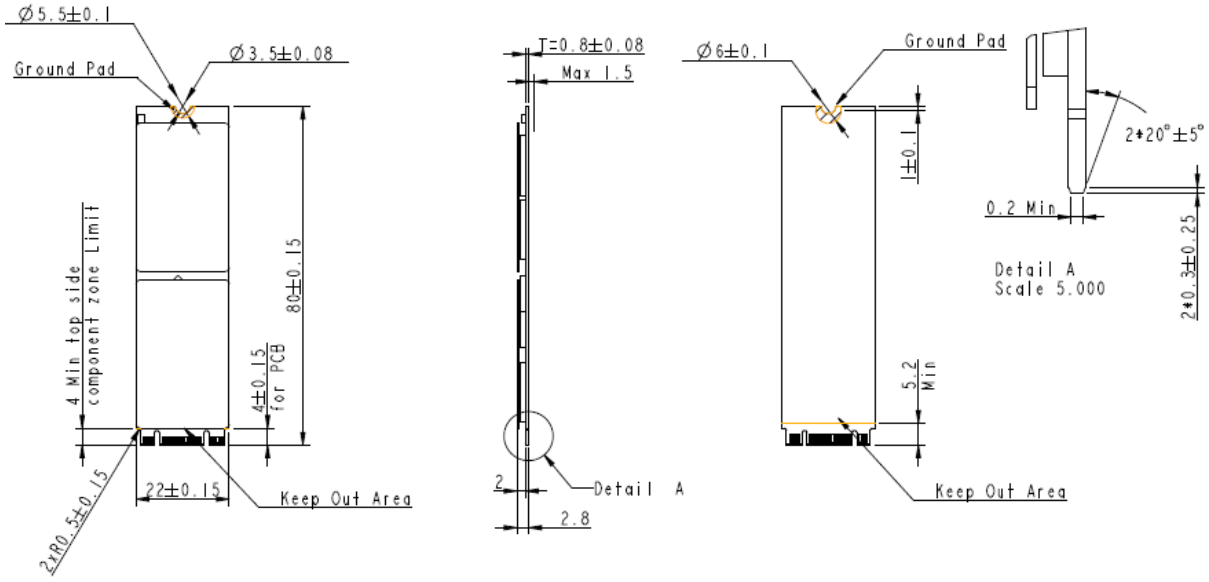


### 9.1.3 960GB

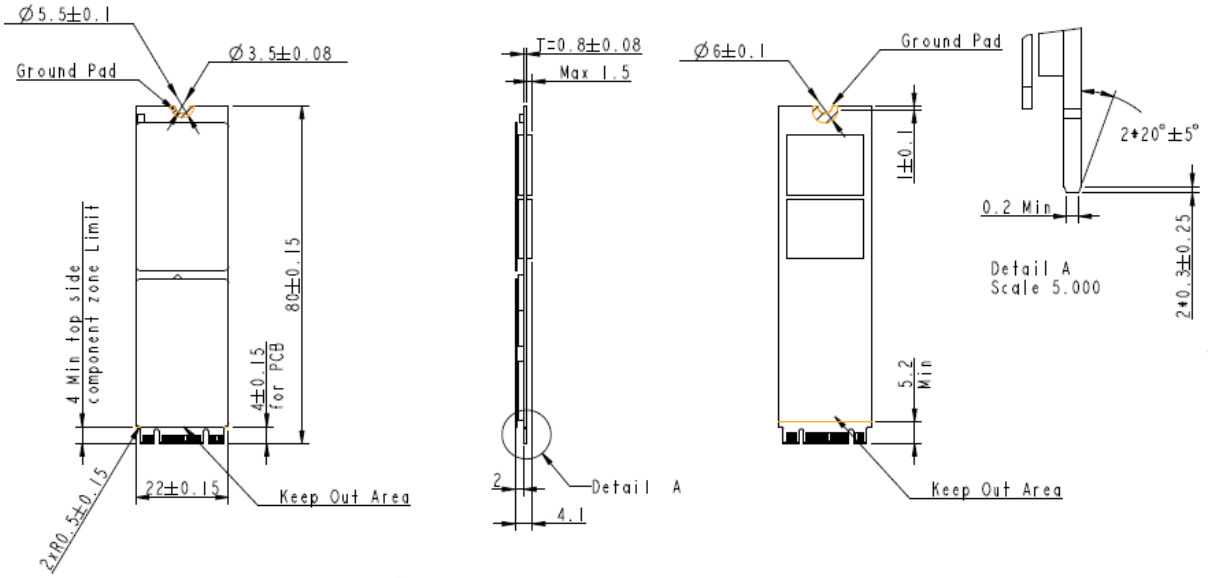



## 9.2 Wide Temperature

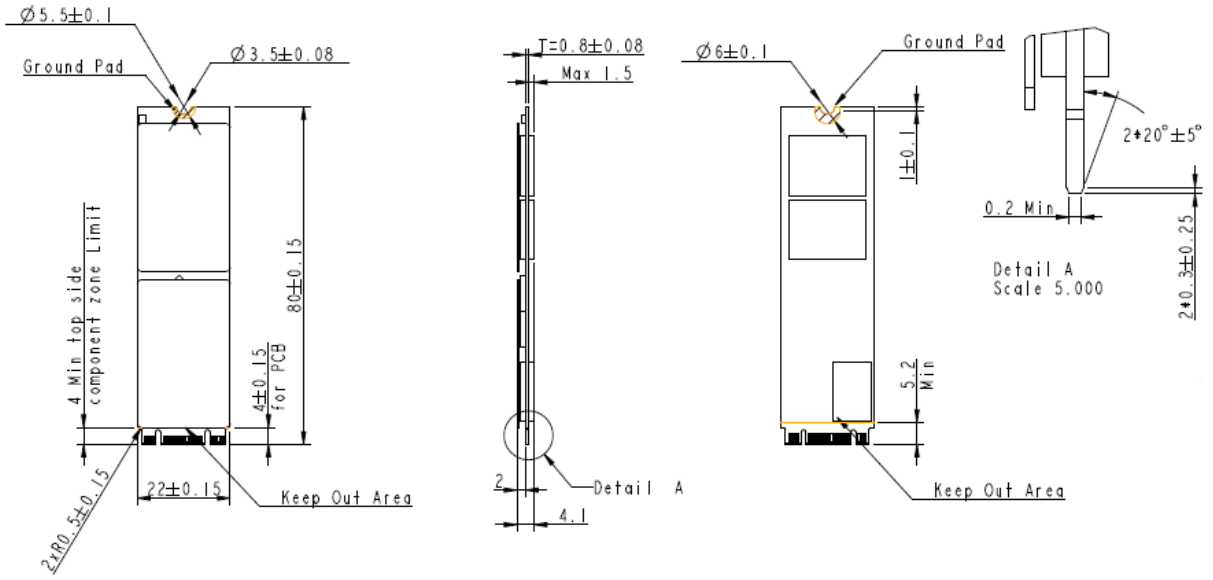
### 9.2.1 120-240GB



### 9.2.2 480GB




### 9.2.3 960GB



## 9.3 Net Weight

**Table 9-1** Net Weight

| Standard Temperature | |
|---|---|
| **Capacity** | **Net Weight (g ± 5%)** |
| 120GB | 5.4 |
| 240GB | 5.5 |
| 480GB | 6.3 |
| 960GB | 7.3 |
| **Wide Temperature** | |
| **Capacity** | **Net Weight (g ± 5%)** |
| 120GB | 8.0 |
| 240GB | 8.0 |
| 480GB | 8.8 |
| 960GB | 9.8 |

# 10. Product Ordering Information

## 10.1 Product Code Designations

| Code | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | B | 9 | 2 | . | X | X | 5 | X | X | X | . | X | X | X | X | X |

| | |
|---|---|
| **Code 1-3<br>(Product Line & form factor)** | PCIe M280 |
| **Code 5-6<br>(Model/Solution)** | 12: PV120-M280<br>A1: PV120-M280 with TCG Opal |
| **Code 7-8<br>(Product Capacity)** | 5H: 120GB<br>5J: 240GB<br>5K: 480GB<br>5L: 960GB |
| **Code 9<br>(Flash Type & Product Temp)** | G: 3D TLC Standard temperature<br>H: 3D TLC Wide temperature |
| **Code 10<br>(Product Spec)** | A: Single side B+M key<br>B: Double side B+M key<br>P: Single Side B+M key with metal pad<br>Q: Double Side B+M Key with metal pad |
| **Code 12-14<br>(Version Number)** | Random numbers generated by system |
| **Code 15-16<br>(Firmware Version)** | 05: Standard<br>04: TCG Opal |

## 10.2 Valid Combinations

### 10.2.1 Standard

| Capacity | Standard Temperature | Wide Temperature |
|---|---|---|
| 120GB | B92.125HGA.00205 | B92.125HHP.00105 |
| 240GB | B92.125JGA.00205 | B92.125JHP.00105 |
| 480GB | B92.125KGB.00205 | B92.125KHQ.00105 |
| 960GB | B92.125LGB.00105 | B92.125LHQ.00105 |

### 10.2.2 TCG Opal (optional)

| Capacity | Standard Temperature | Wide Temperature |
|---|---|---|
| 120GB | B92.A15HGA.00104 | B92.A15HHP.00104 |
| 240GB | B92.A15JGA.00104 | B92.A15JHP.00104 |
| 480GB | B92.A15KGB.00104 | B92.A15KHQ.00104 |
| 960GB | B92.A15LGB.00104 | B92.A15LHQ.00104 |

**Note:** Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

# Revision History

| Revision | Description | Date |
|---|---|---|
| 0.1 | Preliminary release | 3/19/2019 |
| 0.2 | - Revised “SATA-based” appearing in the first sentence of the second paragraph at 1. General Descriptions to “PCIe-based”<br>- Added JESD-219A to the first note at 4.6 Endurance<br>- Added DataRAID™ to Flash Management on Specifications Overview page<br>- Added 5.9 DataRAID™<br>- Removed DataDefender support<br>- Updated the length and description of byte 262-269 to 8 and Reserved respectively at Table 7-5 SMART (C0h) | 3/28/2019 |
| 1.0 | - Completed endurance rating for Endurance on Specifications Overview page and 4.6 Endurance<br>- Updated Performance on Specifications Overview page and 4.2 Performance<br>- Removed TCG Opal 2.0 support | 4/16/2019 |
| 1.1 | - Changed compliance version to NVMe from 1.3 to 1.2 for PCIe Interface on Specifications Overview page<br>- Added Power Failure Management support<br>- Updated length and description of bytes 2-255 and 262-273 for Table 7-5 SMART (C0h) | 5/2/2019 |
| 1.2 | - Added 960GB support<br>- Updated endurance rating for Endurance on Specifications Overview page and 4.6 Endurance | 5/13/2019 |
| 1.3 | Removed wide temperature support | 8/22/2019 |
| 1.4 | - Added product photo to the cover page<br>- Added wide temperature support<br>- Added CoreGlacier to Reliability on Specifications Overview page<br>- Added Net Weight to Form Factor on Specifications Overview page<br>- Updated shock and vibration specs at 4.3 Environmental Specifications<br>- Updated the note for 4.4 Mean Time Between Failures (MTBF)<br>- Updated technology description for 5.5 Power Failure Management<br>- Added 6.5 CoreGlacier<br>- Updated mechanical specs for 9. Physical Characteristics<br>- Added 9.3 Net Weight<br>- Updated 10. Product Ordering Information by adding wide temperature information | 10/31/2019 |

| Revision | Description | Date |
|---|---|---|
| 1.5 | Updated form factor from M.2 2280-S3/D5-B-M to M.2 2280 single/double side, B+M key on Specifications Overview page | 11/6/2019 |
| 1.6 | - Added TCG Opal to Security section on Specifications Overview page<br>- Added 6.2 TCG Opal Section<br>- Added a note to Table 7-2 Admin Commands – NVM Command Set Specific<br>- Updated 10. Product Ordering Information by adding A1 codes 5-6 and 04 to codes 15-16 | 1/21/2020 |
| 1.7 | Updated 10. Product Ordering Information by changing codes 15-16 for standard series from 03 to 05 due to FW update | 2/27/2020 |
| 1.8 | - Updated MTBF on Specifications Overview page and 4.4 Mean Time Between Failures (MTBF) by changing it from >1,000,000 hours to >3,000,000 hours<br>- Updated Table 4-1 by changing max LBA to total LBA<br>- Added a note regarding DRAM cache to 5.5 Power Failure Management | 8/4/2020 |

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