Apacer

RoHS Recast Compliant

PCI Express Flash Drive

PM110-M280 Product Specifications

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Version 1.4

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Features:

- **PCIe Interface**
  - Compliant with NVMe 1.2
  - Compatible with PCIe I/II/III x 4 interface
- **Capacity**
  - 128, 256, 512 GB
- **Performance***
  - Interface burst read/write: 4 GB/sec
  - Sequential read: up to 2,780 MB/sec
  - Sequential write: up to 1,405 MB/sec
  - Random read (4K): up to 293,000 IOPS
  - Random write (4K): up to 194,000 IOPS
- **Flash Management**
  - Built-in hardware ECC
  - Global Wear Leveling
  - Flash bad-block management
  - S.M.A.R.T.
  - Power Failure Management
  - TRIM
- **NAND Flash Type:** MLC
- **MTBF:** >1,000,000 hours
- **Endurance (Est.)**
  - 128 GB: 157 TBW
  - 256 GB: 314 TBW
  - 512 GB: 628 TBW
- **Temperature Range**
  - Operating: 0°C to 70°C
  - Storage: -40°C to 100°C
- **Supply Voltage**
  - 3.3 V ± 5%
- **Power Consumption***
  - Active mode: 1,605 mA
  - Idle mode: 345 mA
- **Connector Type**
  - 75-pin M.2 module pinout
- **Form Factor**
  - M.2 2280 form factor
  - Dimensions: 80.00 x 22.00 x 3.80, unit: mm
- **Thermal Sensor**
- **Thermal Management Technique (optional)**
- **End-to-End Data Protection**
- **RoHS Compliant**

*Varies from capacities. The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings.

Table of Contents

1. Product Descriptions

1.1 Introduction

Apacer PM110-M280 (M.2 2280) is the next generation modularized Solid State Drive (SSD) with the shape of all new M.2 form factor, aimed to be the more suitable for mobile and compact computers with standard width at only 22.00 mm. PM110-M280 appears in M.2 2280 mechanical dimensions and is believed to be the leading add-in storage solution for future host computing systems.

The M.2 SSD is designed with SATA-based connector pinouts, providing full compliance with the latest PCIe Gen3 x4 interface specifications. Aside from PCIe compliance, PM110-M280 delivers exceptional performance and power efficiency. On the other hand, the extreme thin and light form factor makes PM110-M280 the ideal choice for mobile computing systems, which appears to be the trend in near future.

Regarding reliability, PM110-M280 is built with a powerful PCIe controller that supports on-the-module ECC as well as efficient wear leveling scheme. In terms of power efficiency, PM110-M280 is compliant with PCIe Gen 3 x4 interface standard so that it can operate on power management modes, which greatly save on power consumption.

1.2 Capacity

Table 1-1 Capacity Specifications

Capacity	Total bytes*	Cylinders	Heads	Sectors	Max LBA
128 GB	128,035,676,160	16,383	16	63	250,069,680
256 GB	256,060,514,304	16,383	16	63	500,118,192
512 GB	512,110,190,592	16,383	16	63	1,000,215,216

*Display of total bytes varies from file systems, which means not all of the bytes can be used for storage.
**Notes: 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.
LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

1.3 Performance

Performance of PM110-M280 is listed below in Table 1-2.

Table 1-2 Performance Specifications

Performance \ Capacity	128 GB	256 GB	512 GB
Sequential Read* (MB/s)	2,475	2,780	2,780
Sequential Write* (MB/s)	735	1,390	1,405
Random Read IOPS (4K)**	138,000	293,000	288,000
Random Write IOPS (4K)**	100,000	142,000	194,000

Note:
Results may differ from various flash configurations or host system setting.
*Sequential performance is based on CrystalDiskMark 5.2.1 with file size 1,000MB.
**Random performance measured using IOMeter with Queue Depth 32.

1.4 Pin Assignments

This connector does not support hot plug capability. There are a total of 75 pins. 12 pin locations are used for mechanical key locations; this allows such a module to plug into Key M connectors.

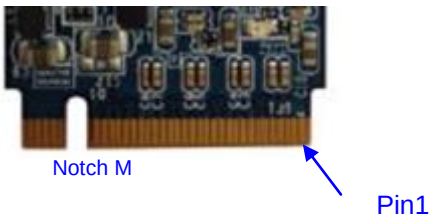


Table 1-3 Pin Assignments

Pin	PCIe Pin	Description
1	GND	Ground
2	3.3V	3.3V source
3	GND	Ground
4	3.3V	3.3V source
5	PETn3	PCIe TX Differential signal defined by the PCI Express M.2 spec
6	N/C	No connect
7	PETp3	PCIe TX Differential signal defined by the PCI Express M.2 spec
8	N/C	No connect
9	GND	Ground
10	LED1#(O)	Status indicators via LED devices
11	PERn3	PCIe RX Differential signal defined by the PCI Express M.2 spec
12	3.3V	3.3V source
13	PERp3	PCIe RX Differential signals defined by the PCI Express M.2 spec
14	3.3V	3.3V source
15	GND	Ground
16	3.3V	3.3V source
17	PETn2	PCIe TX Differential signal defined by the PCI Express M.2 spec
18	3.3V	3.3V source
19	PETp2	PCIe TX Differential signal defined by the PCI Express M.2 spec
20	N/C	No connect
21	GND	Ground
22	N/C	No connect
23	PERn2	PCIe RX Differential signal defined by the PCI Express M.2 spec
24	N/C	No connect
25	PERp2	PCIe RX Differential signal defined by the PCI Express M.2 spec
26	N/C	No connect
27	GND	Ground
28	N/C	No connect
29	PETn1	PCIe TX Differential signal defined by the PCI Express M.2 spec
30	N/C	No connect
31	PETp1	PCIe TX Differential signal defined by the PCI Express M.2 spec
32	N/C	No connect
33	GND	Ground
34	N/C	No connect
35	PERn1	PCIe RX Differential signal defined by the PCI Express M.2 spec
36	N/C	No connect
37	PERp1	PCIe RX Differential signal defined by the PCI Express M.2 spec
38	N/C	No connect
39	GND	Ground
40	N/C	No connect
41	PETn0	PCIe TX Differential signal defined by the PCI Express M.2 spec
42	N/C	No connect
43	PETp0	PCIe TX Differential signal defined by the PCI Express M.2 spec

Table 1-3 Pin Assignments

Pin	PCIe Pin	Description
44	N/C	No connect
45	GND	Ground
46	N/C	No connect
47	PERn0	PCIe RX Differential signal defined by the PCI Express M.2 spec
48	N/C	No connect
49	PERp0	PCIe RX Differential signal defined by the PCI Express M.2 spec
50	PERST#(I)(0/3.3V)	PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification.
51	GND	Ground
52	CLKREQ#(I/O)(0/3.3V)	Clock Request is a reference clock request signal as defined by the PCIe Mini CEM specification; Also used by L1 PM Substates.
53	REFCLKn	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
54	PEWAKE#(I/O)(0/3.3V)	PCIe PME Wake. Open Drain with pull up on platform; Active Low.
55	REFCLKp	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
56	Reserved for MFG DATA	Manufacturing Data line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
57	GND	Ground
58	Reserved for MFG CLOCK	Manufacturing Clock line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
59	Module Key	Module Key
60	Module Key	
61	Module Key	
62	Module Key	
63	Module Key	
64	Module Key	
65	Module Key	
66	Module Key	
67	N/C	No connect
68	SUSCLK(32KHz) (I)(0/3.3V)	32.768 kHz clock supply input that is provided by the platform chipset to reduce power and cost for the module.
69	PEDET (NC-PCIe)	Host I/F Indication; No Connect for PCIe.
70	3.3V	3.3V source
71	GND	Ground
72	3.3V	3.3V source
73	GND	Ground
74	3.3V	3.3V source
75	GND	Ground

2. Software Interface

2.1 Command Set

Table 2-1 summarizes the commands supported by PM110-M280.

Table 2-1 Admin Commands

Opcode	Command Description
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Features
0Ah	Get Features
0Ch	Asynchronous Event Request
10h	Firmware Activate
11h	Firmware Image Download

Table 2-2 Admin Commands – NVM Command Set Specific

Opcode	Command Description
80h	Format NVM
81h	Security Send
82h	Security Receive

Table 2-3 NVM Commands

Opcode	Command Description
00h	Flush
01h	Write
02h	Read
04h	Write Uncorrectable
05h	Compare
08h	Write Zeroes
09h	Dataset Management

2.2 S.M.A.R.T.

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

3. Flash Management

3.1 Error Correction/Detection

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, this M.2 2280 SSD module applies the BCH ECC Algorithm, which can detect and correct errors occur during Read process, ensure data been read correctly, as well as protect data from corruption. This device can correct up to 120 bits error in 2K Bytes.

3.2 Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. Apacer implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

3.3 Global Wear Leveling

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Global wear leveling is an important mechanism that levels out the wearing of all blocks so that the wearing-down of all blocks can be almost evenly distributed. This will increase the lifespan of SSDs.

3.4 Power Failure Management

Power Failure Management plays a crucial role when experiencing unstable power supply. Power disruption may occur when users are storing data into the SSD. In this urgent situation, the controller would run multiple flush cycles to store the metadata for later block rebuilding. This urgent operation requires about several milliseconds to get it done. At the next power up, the firmware will perform a status tracking to retrieve the mapping table and resume previously programmed NAND blocks to check if there is any incompleteness of transmission.

3.5 TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks all the time

3.6 Thermal Sensor

Apacer Thermal Sensor is a digital temperature sensor with serial interface. By using designated pins for transmission, storage device owners are able to read temperature data.

3.7 Thermal Management Technique (optional)

Thermal management technique can monitor the temperature of the SSD equipped with a built-in thermal sensor via S.M.A.R.T. commands. This method can ensure the temperature of the device stays within temperature limits by drive throttling, i.e. reducing the speed of the drive when the device temperature reaches the threshold level, so as to prevent overheating, guarantee data reliability, and prolong product lifespan. When the temperature exceeds the maximum threshold level, thermal throttling will be triggered to reduce performance step by step to prevent hardware components from being damaged. Performance is only permitted to drop to the extent necessary for recovering a stable temperature to cool down the device's temperature. Once the temperature decreases to the minimum threshold value, transfer speeds will rise back to its optimum performance level.

3.8 End-to-End Data Protection

End-to-End Data Protection provides full error detection covering the whole data pass between the host computer system and the internal storage media. It ensures data integrity by protecting against possible data corruption in the NAND, SRAM, and DRAM memory. Protected information is attached to the data or may be LBA-rooted. In the SSD concept, it stays in the data, travelling from the host, through the SSD flash controller, and then to the NAND flash media. When the user reads the data later, the same protected information travels the same route back and eventually returns to the host computer system. This measure is implemented to ensure data correctness everywhere in the read/write route.

With End-To-End Protection, errors, especially soft errors, can be located and isolated at any point during the data read/write route. Once an error is detected, an immediate attempt will be made to correct it, and any uncorrectable error will be reported to the host. It is two-way security rather than one-way, which offers a more comprehensive detection and prevents ECC failure.

4. Environment Specifications

4.1 Environmental

Table 4-1 Environmental Specifications

Environment	Specifications
Temperature	0°C to 70°C (Operating)
	-40°C to 100°C (Storage)
Shock	1500G, 0.5ms
Vibration	20Hz~80Hz/1.52mm (frequency/displacement) 80Hz~2000Hz/20G (frequency/displacement) X, Y, Z axis/60mins each
Drop	80cm free fall, 6 face of each
Bending	≧20N, hold 1min/5times
Torque	0.5N-m or 5deg, hold 5min/5times
ESD	Pass

Note: Shock and Vibration specifications are subject to change without notice.

4.2 Mean Time Between Failures (MTBF)

MTBF, an acronym for Mean Time Between Failures, is a measure of a device's reliability. Its value represents the average time between a repair and the next failure. The measure is typically in units of hours. The higher the MTBF value, the higher the reliability of the device. The predicted result of this M.2 2280 device is higher than 1,000,000 hours.

4.3 Certification and Compliance

PM110-M280 complies with the following standards:

- FCC: CISPR22
- CE: EN55022
- BSMI 13438
- RoHS
- PCI Express Base 3.0
- UNH-IOL NVM Express Logo

4.4 Endurance (Est.)

The endurance of a storage device is predicted by Tera Bytes Written based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

Capacity	Tera Bytes Written
128 GB	157
256 GB	314
512 GB	628

Note:

- Samples are built using Toshiba 15nm Toggle MLC NAND flash.
- The measurement assumes the data written to the SSD for test is under a typical and constant rate.
- The measurement follows the standard metric: 1 TB (Terabyte) = 1,000 GB.
- The measurement follows JEDEC JESD-219 standard to test WAF.
- This estimation complies with JEDEC JESD-219, enterprise endurance workload of random data with payload size distribution.
- The endurance of SSD could be estimated based on user behavior, NAND endurance cycles, and write amplification factor. It is not guaranteed by flash vendor.

5. Electrical Specifications

5.1 Operating Voltage

Table 5-1 lists the supply voltage for PM110-M280.

Table 5-1 Operating Range

Item	Range
Supply Voltage	3.3V ± 5%

5.2 Power Consumption

Table 5-2 lists the power consumption for PM110-M280.

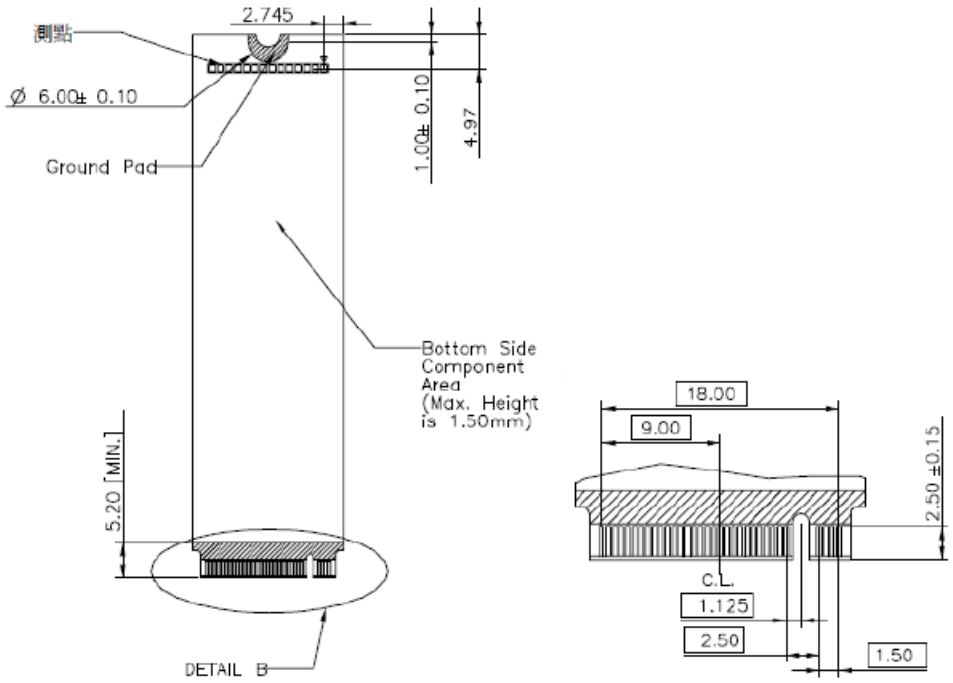
Table 7-2 Power Consumption

Mode \ Capacity	128 GB	256 GB	512 GB
Active (mA)	1,300	1,380	1,605
Idle (mA)	340	345	345

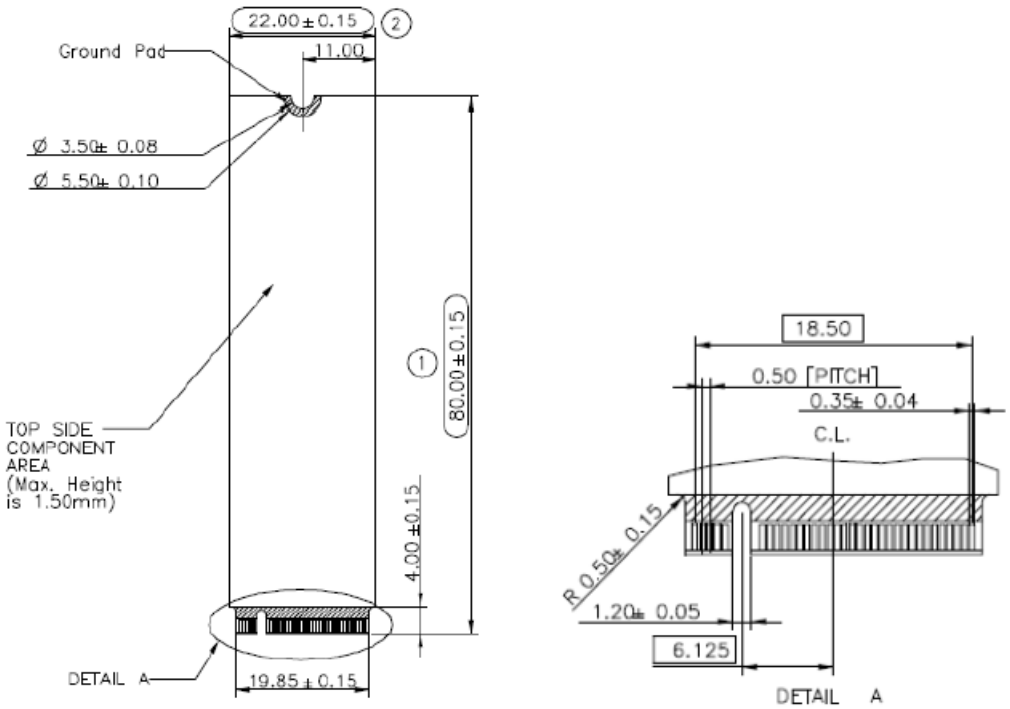
Note:
*All values are typical and may vary depending on flash configurations or host system settings.
**Active power is an average power measurement performed using CrystalDiskMark with 128KB sequential read/write transfers.

6. Physical Characteristics

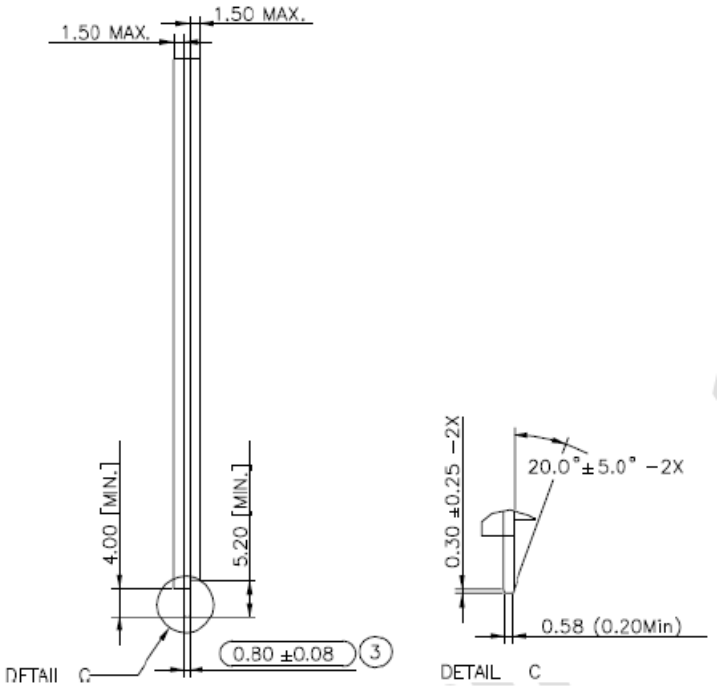
Bottom View



Top View



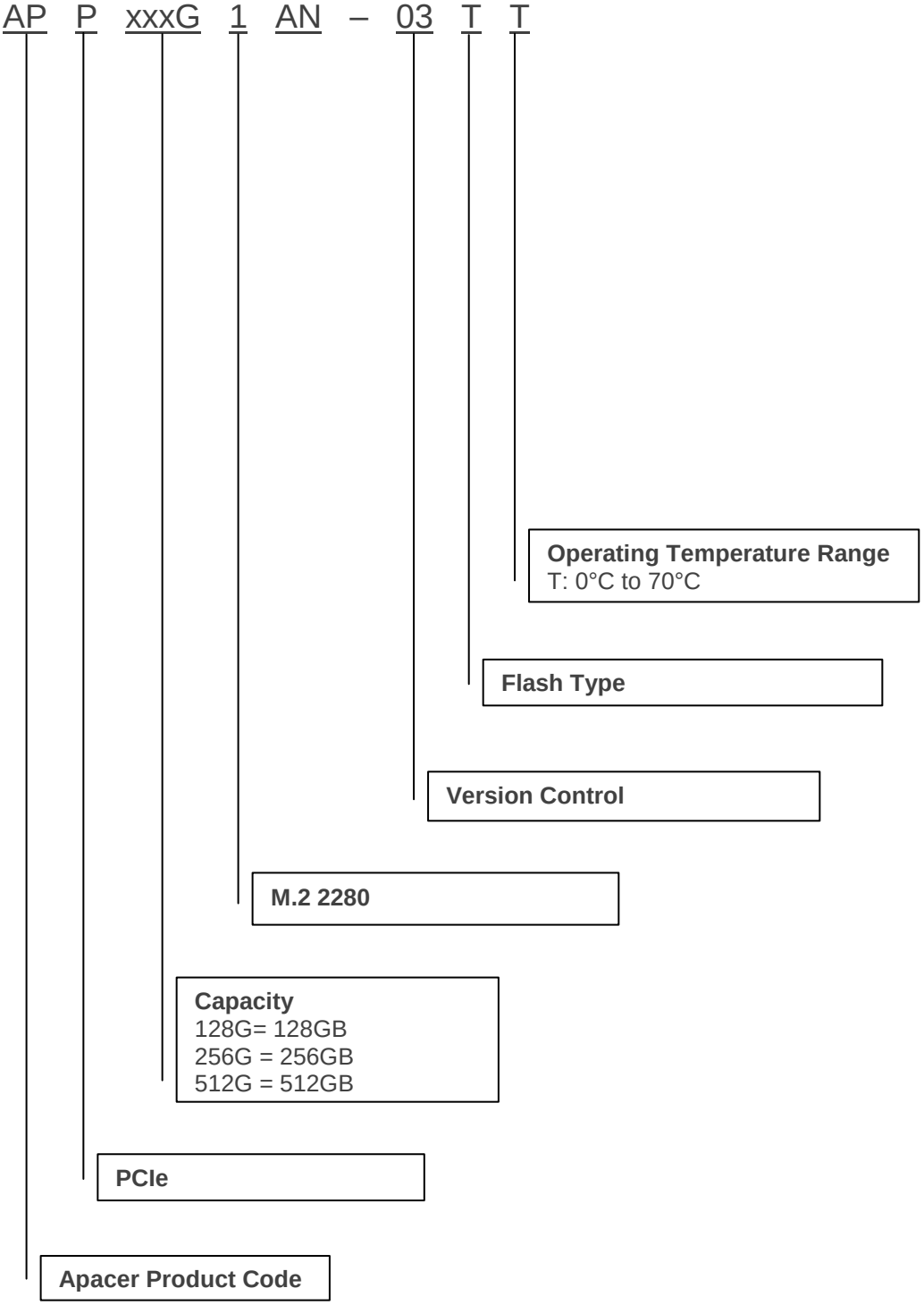
Side View



7. Product Ordering Information

7.1 Product Code Designations

AP P xxxG 1 AN – 03 T T



7.2 Valid Combinations

Capacity	Part Number
128GB	APP128G1AN-03TT
256GB	APP256G1AN-03TT
512GB	APP512G1AN-03TT

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Revision History

Revision	Description	Date
0.1	Preliminary release	10/19/2016
0.2	- Changed the model name from PM110-25 to PM110-M280 - Updated performance and power consumption values	10/28/2016
0.3	Revised SSD type from SATA to PCIe on cover page	11/8/2016
1.0	- Added product photo to Features page - Updated endurance ratings	12/21/2016
1.1	Added “Thermal Sensor/Thermal Throttling FW” and “End-to-End Data Protection” to Features page	1/5/2017
1.2	- Separated Thermal Throttling from Thermal Sensor on Features page - Revised ECC to 120 bits/2KB - Removed 3.6 Over Provision	1/11/2017
1.3	Added 3.7 Thermal Management Technique and 3.8 End-to-End Data Protection	4/13/2017
1.4	Updated product ordering information	10/13/2017

Global Presence

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