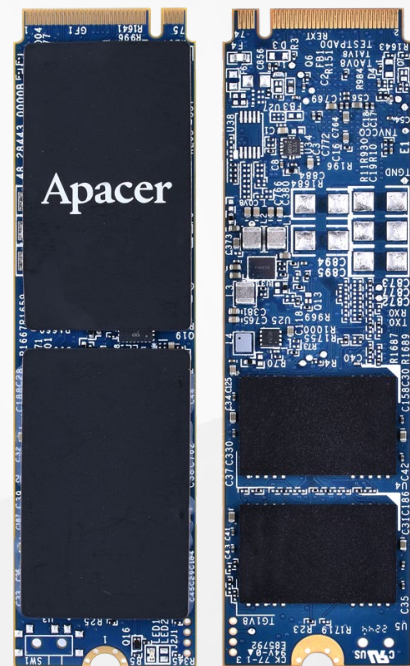


RoHS Compliant

PCI Express Flash Drive

Industrial PV250-M280 BiCS5 Product Specifications



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Version 2.0



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Specifications Overview:

- **PCIe Interface**
 - Compliant with PCI Express 4.0
 - Compliant with NVMe 2.0
 - Compatible with PCIe Gen4 x4 interface
- **Capacity**
 - 240, 480, 960, 1920, 3840 GB
- **Performance¹**
 - Interface burst read/write: 8 GB/sec
 - Sequential read: up to 3,675 MB/sec
 - Sequential write: up to 3,215 MB/sec
 - Random read (4K): up to 565,000 IOPS
 - Random write (4K): up to 560,000 IOPS
- **Flash Management**
 - Low-Density Parity-Check (LDPC) Code
 - Global Wear Leveling
 - Flash bad-block management
 - Flash Translation Layer: Page Mapping
 - DataDefender™
 - S.M.A.R.T.
 - TRIM
 - Hyper Cache Technology
 - Over-provisioning
 - SMART Read Refresh™
 - NVMe Secure Erase
- **NAND Flash Type: 3D TLC (BiCS5)**
- **MTBF: >3,000,000 hours**
- **Endurance (in drive writes per day: DWPD)**
 - 240 GB: 2.10 DWPD
 - 480 GB: 1.99 DWPD
 - 960 GB: 1.69 DWPD
 - 1920 GB: 2.13 DWPD
 - 3840 GB: 1.55 DWPD
- **Temperature Range**
 - Operating:
 - Standard: 0°C to 70°C
 - Wide²: -40°C to 85°C
 - Storage: -55°C to 100°C
- **Supply Voltage**
 - 3.3V ± 5%
- **Power Consumption¹**
 - Active mode (Max.): 1,595 mA
 - Idle mode: 240 mA
- **Power Management**
 - Supports APST
 - Supports ASPM L1.2
- **Connector Type**
 - 75-pin M.2 module pinout
- **NVMe Features³**
 - Supports HMB (Host Memory Buffer)
- **Security**
 - AES 256-bit hardware encryption
 - Trusted Computing Group (TCG) Opal 2.0 (optional)⁴
- **Reliability**
 - Thermal Sensor
 - Thermal Throttling
 - Sidfill
 - End-to-End Data Protection
 - CoreGlacier™
- **Physical Characteristics**
 - Form factor: Double-sided M.2 2280-M
 - Dimensions: 22.00 x 80.00 x 4.08_(max.), unit: mm
 - Net weight: 7.8g ± 5%
- **LED Indicators for Drive Behavior**
- **RoHS Compliant**

Notes:

1. Varies from capacities. The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings.
2. Not supported on 3840GB
3. Windows 10 (version 1703) onwards supports the HMB (Host Memory Buffer) function.
4. Not supported on 3840GB

Table of Contents

| | |
|---|-----------|
| 1. General Description | 4 |
| 2. Functional Block | 4 |
| 3. Pin Assignments..... | 5 |
| 4. Product Specifications..... | 8 |
| 4.1 Capacity..... | 8 |
| 4.2 Performance | 8 |
| 4.3 Environmental Specifications | 9 |
| 4.4 Mean Time Between Failures (MTBF) | 9 |
| 4.5 Certification and Compliance..... | 9 |
| 4.6 Endurance | 10 |
| 4.7 LED Indicator Behavior..... | 10 |
| 5. Flash Management | 11 |
| 5.1 Error Correction/Detection..... | 11 |
| 5.2 Bad Block Management | 11 |
| 5.3 Global Wear Leveling | 11 |
| 5.4 DataDefender™ | 11 |
| 5.5 TRIM..... | 11 |
| 5.6 Flash Translation Layer – Page Mapping..... | 12 |
| 5.7 Hyper Cache Technology | 12 |
| 5.8 Over-provisioning | 12 |
| 5.9 SMART Read Refresh™ | 12 |
| 5.10 NVMe Secure Erase..... | 12 |
| 6. NVMe Support Features | 13 |
| 6.1 Host Memory Buffer..... | 13 |
| 7. Security and Reliability Features | 14 |
| 7.1 Advanced Encryption Standard | 14 |
| 7.2 TCG Opal (optional) | 14 |
| 7.3 Thermal Sensor | 14 |
| 7.4 Thermal Throttling | 14 |
| 7.5 Sidefill | 15 |
| 7.6 End-to-End Data Protection..... | 15 |

| | |
|--|-----------|
| 7.7 CoreGlacier™ | 15 |
| 8. Software Interface | 16 |
| 8.1 Command Set..... | 16 |
| 8.2 S.M.A.R.T. | 17 |
| 9. Electrical Specifications..... | 19 |
| 9.1 Operating Voltage..... | 19 |
| 9.2 Power Consumption | 19 |
| 10. Mechanical Specifications | 20 |
| 11. Product Ordering Information..... | 22 |
| 11.1 Product Code Designations..... | 22 |
| 11.2 Valid Combinations..... | 23 |

1. General Description

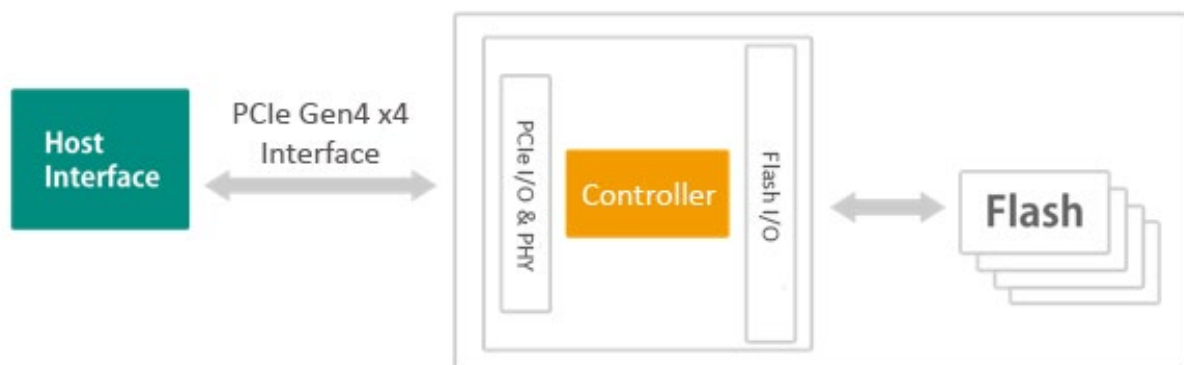
Apacer PV250-M280 is the fastest SSD designed as M.2 2280 mechanical dimensions which provides full compliance with PCIe Gen4 x4 interface and NVMe 2.0 specifications, allowing it to operate in power management modes and greatly save on power consumption. Built with a powerful PCIe controller that supports on-the-module ECC as well as efficient wear leveling scheme, PV250-M280 delivers exceptionally low latency and outstanding performance in data transfer. With the compact and high-speed storage, PV250-M280 is the ideal choice for larger, faster hosts deployed in a wide range of applications that require outstanding performance.

Utilizing 3D NAND for higher capacity up to 3840GB and providing more power efficiency than 2D NAND, PV250-M280 is not only implemented with LDPC (Low Density Parity Check) ECC engine to extend SSD endurance and increase data reliability, but also equipped with a built-in thermal sensor to monitor the temperature of the SSD via S.M.A.R.T commands and configured with thermal throttling to dynamically adjust frequency scaling to enhance data reliability and provide sustained performance while overheating. CoreGlacier is also available to keep temperatures low, while still allowing the drive to deliver high-speed performance. To increase product reliability and resistance to various thermal and mechanical shocks, PV250-M280 also provides Sidfill technology to ensure that products continue to operate normally in high vibration and under extreme environmental changes. For highly-intensive applications, End-to-End Data Protection ensures that data integrity can be assured at multiple points in the path to enable reliable delivery of data transfers.

In terms of security, Advanced Encryption Standard (AES) and Trusted Computing Group (TCG) Opal (optional) ensure data security and provide users with peace of mind knowing their data is safeguarded against unauthorized use at all times. PV250-M280 also adopts the latest page mapping file translation layer and comes with various implementations including flash block management, DataDefender, TRIM, power saving modes, Hyper Cache technology, over-provisioning, SMART Read Refresh, and NVMe secure erase.

With exceptional performance, trustable reliability, and enhanced data protection, PV250-M280 is definitely the ideal storage or cache solution for a variety of applications ranging from industrial, imaging, computing to enterprise markets.

2. Functional Block



Note: The actual number of NAND flash used on Apacer PV250-M280 varies from capacities. The illustration is for reference only.

Figure 2-1 Functional Block Diagram

3. Pin Assignments

This connector does not support hot plug capability. There are a total of 75 pins. 12 pin locations are used for mechanical key locations; this allows such a module to plug into Key M connectors.



Figure 3-1 Pin Connectors

Table 3-1 Pin Assignments

| Pin No. | Type | Description |
|---------|------------------------|--|
| 1 | GND | Ground |
| 2 | 3.3 V | 3.3V source |
| 3 | GND | Ground |
| 4 | 3.3 V | 3.3V source |
| 5 | PETn3 | PCIe TX Differential signal defined by the PCI Express M.2 spec |
| 6 | PWRDIS (I)(0/1.8/3.3V) | No connect |
| 7 | PETp3 | PCIe TX Differential signal defined by the PCI Express M.2 spec |
| 8 | PLN# (I)(0/1.8/3.3V) | No connect |
| 9 | GND | Ground |
| 10 | LED1# | Open drain, active low signal. These signals are used to allow the add-in card to provide status indicators via LED devices that will be provided by the system. |
| 11 | PERn3 | PCIe RX Differential signal defined by the PCI Express M.2 spec |
| 12 | 3.3 V | 3.3V source |
| 13 | PERp3 | PCIe RX Differential signals defined by the PCI Express M.2 spec |
| 14 | 3.3 V | 3.3V source |
| 15 | GND | Ground |
| 16 | 3.3 V | 3.3V source |
| 17 | PETn2 | PCIe TX Differential signal defined by the PCI Express M.2 spec |
| 18 | 3.3 V | 3.3V source |
| 19 | PETp2 | PCIe TX Differential signal defined by the PCI Express M.2 spec |

Table 3-1 Pin Assignments

| Pin No. | Type | Description |
|---------|----------------------------|--|
| 20 | NC | No connect |
| 21 | GND | Ground |
| 22 | VIO 1.8 V | No connect |
| 23 | PERn2 | PCIe RX Differential signal defined by the PCI Express M.2 spec |
| 24 | NC | No connect |
| 25 | PERp2 | PCIe RX Differential signal defined by the PCI Express M.2 spec |
| 26 | NC | No connect |
| 27 | GND | Ground |
| 28 | NC | No connect |
| 29 | PETn1 | PCIe TX Differential signal defined by the PCI Express M.2 spec |
| 30 | PLA_S3# (O)(0/1.8/3.3V) | No connect |
| 31 | PETp1 | PCIe TX Differential signal defined by the PCI Express M.2 spec |
| 32 | GND | Ground |
| 33 | GND | Ground |
| 34 | USB_D+ | No connect |
| 35 | PERn1 | PCIe RX Differential signal defined by the PCI Express M.2 spec |
| 36 | USB_D- | No connect |
| 37 | PERp1 | PCIe RX Differential signal defined by the PCI Express M.2 spec |
| 38 | GND | Ground |
| 39 | GND | Ground |
| 40 | SMB_CLK (I/O)(0/1.8V) | No connect |
| 41 | PETn0 | PCIe TX Differential signal defined by the PCI Express M.2 spec |
| 42 | SMB_DATA (I/O)(0/1.8V) | No connect |
| 43 | PETp0 | PCIe TX Differential signal defined by the PCI Express M.2 spec |
| 44 | ALERT# (O)(0/1.8V) | No connect |
| 45 | GND | Ground |
| 46 | NC | No connect |
| 47 | PERn0 | PCIe RX Differential signal defined by the PCI Express M.2 spec |
| 48 | NC | No connect |
| 49 | PERp0 | PCIe RX Differential signal defined by the PCI Express M.2 spec |
| 50 | PERST# (I)(0/1.8V/3.3V) | PE-Reset is a functional reset to the card as specification. defined by the PCIe Mini CEM |
| 51 | GND | Ground |
| 52 | CLKREQ# (I/O)(0/1.8V/3.3V) | Clock Request is a reference clock request signal as defined by the PCIe Mini CEM specification; Also used by L1 PM Substates. |
| 53 | REFCLKn | PCIe Reference Clock signals (100 MHz) spec. defined by the PCI Express M.2 |
| 54 | PEWAKE# (I/O)(0/1.8V/3.3V) | No connect |
| 55 | REFCLKp | PCIe Reference Clock signals (100 MHz) spec. defined by the PCI Express M.2 |
| 56 | Reserved for MFG_DATA | Reserved for Apacer use only ¹ |
| 57 | GND | Ground |
| 58 | Reserved for MFG_CLOCK | Reserved for Apacer use only ¹ |

Table 3-1 Pin Assignments

| Pin No. | Type | Description |
|---------|-------------------------|---|
| 59 | Module Key M | Module Key |
| 60 | Module Key M | Module Key |
| 61 | Module Key M | Module Key |
| 62 | Module Key M | Module Key |
| 63 | Module Key M | Module Key |
| 64 | Module Key M | Module Key |
| 65 | Module Key M | Module Key |
| 66 | Module Key M | Module Key |
| 67 | NC | Reserved for Apacer use only ¹ |
| 68 | SUSCLK (I)(0/1.8V/3.3V) | No connect |
| 69 | PEDET | No connect |
| 70 | 3.3 V | 3.3V source |
| 71 | GND | Ground |
| 72 | 3.3 V | 3.3V source |
| 73 | VIO_CFG (O) | Ground |
| 74 | 3.3 V | 3.3V source |
| 75 | GND | Ground |

Note:

1. Reserved by Apacer, please do not connect to a host.

4. Product Specifications

4.1 Capacity

Capacity specifications of PV250-M280 are available as shown in Table 4-1.

Table 4-1 Capacity Specifications

| Capacity | Total bytes | Total LBA |
|----------|-------------------|---------------|
| 240 GB | 240,057,409,536 | 468,862,128 |
| 480 GB | 480,103,981,056 | 937,703,088 |
| 960 GB | 960,197,124,096 | 1,875,385,008 |
| 1920 GB | 1,920,383,410,176 | 3,750,748,848 |
| 3840 GB | 3,840,755,982,336 | 7,501,476,528 |

Notes:

- Display of total bytes varies from operating systems.
- 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.
- LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

4.2 Performance

Performance of PV250-M280 is listed below in Table 4-2.

Table 4-2 Performance Specifications

| Capacity \ Performance | 240 GB | 480 GB | 960 GB | 1920 GB | 3840 GB |
|--------------------------------|---------|---------|---------|---------|---------|
| Sequential Read (MB/s) | 3,100 | 3,200 | 3,300 | 3,325 | 3,675 |
| Sequential Write (MB/s) | 1,600 | 2,825 | 3,000 | 3,020 | 3,215 |
| 4K Random Read (IOPS) | 100,800 | 380,000 | 559,000 | 560,000 | 565,000 |
| 4K Random Write (IOPS) | 296,000 | 549,000 | 558,000 | 559,000 | 560,000 |

Notes:

- Results may differ from various flash configurations or host system setting.
- Sequential read/write is based on CrystalDiskMark 8.0.4 with file size 1,000MB.
- Random read/write is measured using IOMeter with Queue Depth 128.

4.3 Environmental Specifications

Environmental specifications of PV250-M280 are shown in Table 4-3.

Table 4-3 Environmental Specifications

| Parameter | Type | Specifications |
|-------------|---------------|---|
| Temperature | Operating | 0°C to 70°C (Standard); -40°C to 85°C (Wide) |
| | Non-operating | -55°C to 100°C |
| Vibration | Operating | 7.69 GRMS, 20~2000 Hz/random (compliant with MIL-STD-810G) |
| | Non-operating | 4.02 GRMS, 15~2000 Hz/random (compliant with MIL-STD-810G) |
| Shock | Operating | Acceleration, 50(G)/11(ms)/half sine (compliant with MIL-STD-202G) |
| | Non-operating | Acceleration, 1500(G)/0.5(ms)/half sine (compliant with MIL-STD-883K) |

Note: This Environmental Specification table indicates the conditions for testing the device. Real world usages may affect the results.

4.4 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in PV250-M280. The prediction result for PV250-M280 is more than 3,000,000 hours.

Note: The MTBF is predicated and calculated based on “Telcordia Technologies Special Report, SR-332, Issue 3” method.

4.5 Certification and Compliance

PV250-M280 complies with the following standards:

- CE
- UKCA
- FCC
- RoHS
- MIL-STD-810G
- UL

4.6 Endurance

The endurance of a storage device is predicted by Drive Writes Per Day based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

Table 4-4 Endurance Specifications

| Capacity | Drive Writes Per Day |
|----------|----------------------|
| 240 GB | 2.10 |
| 480 GB | 1.99 |
| 960 GB | 1.69 |
| 1920 GB | 2.13 |
| 3840 GB | 1.55 |

Notes:

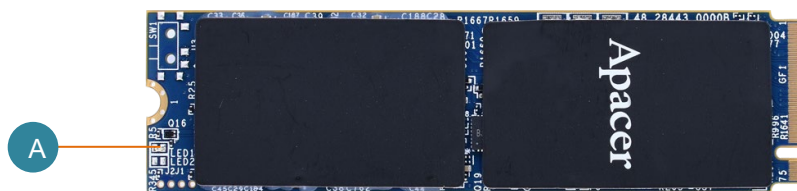
- This estimation complies with JEDEC JESD-219, enterprise endurance workload of random data with payload size distribution.
- Flash vendor guaranteed 3D NAND TLC P/E cycle: 3K
- WAF may vary from capacity, flash configurations and writing behavior on each platform.
- 1 Terabyte = 1,024GB
- DWPD (Drive Writes Per Day) is calculated based on the number of times that user overwrites the entire capacity of an SSD per day of its lifetime during the warranty period. (3D NAND TLC warranty: 3 years)

4.7 LED Indicator Behavior

The behavior of the PV250-M280 LED indicators is described in Table 4-5.

Table 4-5 LED Behavior

| Location | LED | Description |
|----------|-----|---|
| LED A | DAS | LED blinks when the drive is being accessed |



5. Flash Management

5.1 Error Correction/Detection

PV250-M280 implements a hardware ECC scheme, based on the Low Density Parity Check (LDPC). LDPC is a class of linear block error correcting code which has apparent coding gain over BCH code because LDPC code includes both hard decoding and soft decoding algorithms. With the error rate decreasing, LDPC can extend SSD endurance and increase data reliability while reading raw data inside a flash chip.

5.2 Bad Block Management

Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, page mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

5.3 Global Wear Leveling

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Global wear leveling is an important mechanism that levels out the wearing of all blocks so that the wearing-down of all blocks can be almost evenly distributed. This will increase the lifespan of SSDs.

5.4 DataDefender™

Apacer's DataDefender is an advanced technology of power failure management which combines both firmware and hardware mechanisms to ensure data integrity. When power disruption occurs, the low voltage detector will be triggered. When this happens, the SSD's protection mechanism is activated and cuts off data transmission from the host. Once the power supply is resumed, the firmware protection mechanism will ensure the integrity of the firmware as well as the data already written into the NAND flash media.

5.5 TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks all the time.

5.6 Flash Translation Layer – Page Mapping

Page mapping is an advanced flash management technology whose essence lies in the ability to gather data, distribute the data into flash pages automatically, and then schedule the data to be evenly written. Page-level mapping uses one page as the unit of mapping. The most important characteristic is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different sizes of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. Thus, page mapping is adopted to increase random access speed and improve SSD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

5.7 Hyper Cache Technology

Apacer proprietary Hyper Cache technology uses a portion of the available capacity as SLC (1bit-per-cell) NAND flash memory, called Hyper cache mode. When data is written to SSD, the firmware will direct the data to Hyper Cache mode, providing excellent performance to handle various scenarios in industrial use.

5.8 Over-provisioning

Over-provisioning (OP) is a certain portion of the SSD capacity exclusively for increasing Garbage Collection (GC) efficiency, especially when the SSD is filled to full capacity or performs a heavy mixed-random workload. OP has the advantages of providing extended life expectancy, reliable data integrity, and high sustained write performance.

5.9 SMART Read Refresh™

Apacer's SMART Read Refresh plays a proactive role in avoiding read disturb errors from occurring to ensure health status of all blocks of NAND flash. Developed for read-intensive applications in particular, SMART Read Refresh is employed to make sure that during read operations, when the read operation threshold is reached, the data is refreshed by re-writing it to a different block for subsequent use.

5.10 NVMe Secure Erase

NVMe Secure Erase is an NVMe drive sanitize command currently embedded in most of the storage drives. Defined in NVMe specifications, NVMe Secure Erase is part of Format NVM command that allows storage drives to erase all user data areas. The erase process usually runs on the firmware level as most of the NVMe-based storage media currently in the market are built-in with this command. NVMe Secure Erase can securely wipe out the user data in the drive and protects it from malicious attack.

6. NVMe Support Features

6.1 Host Memory Buffer

Host Memory Buffer (HMB) allows HOST to allocate system memory for SSD's exclusive use in order to provide better performance and endurance, especially for DRAMless solutions.

7. Security and Reliability Features

7.1 Advanced Encryption Standard

Advanced Encryption Standard (AES) is a specification for the encryption of electronic data. AES has been adopted by the U.S. government since 2001 to protect classified information and is now widely implemented in embedded computing applications. The AES algorithm used in software and hardware is symmetric so that encrypting/decrypting requires the same encryption key. Without the key, the encrypted data is inaccessible to ensure information security.

Notably in flash memory applications, AES 256-bit hardware encryption is the mainstream to protect sensitive or confidential data. The hardware encryption provides better performance, reliability, and security than software encryption. It uses a dedicated processor, which is built inside the controller, to process the encryption and decryption. This enormously shortens the processing time and makes it efficient.

7.2 TCG Opal (optional)

Developed by the Trusted Computing Group (TCG), an organization whose members work together to formulate industry standards, Opal is a set of security specifications used for applying hardware-based encryption to storage devices.

Hardware encryption has many advantages. First of all, it transfers the computational load of the encryption process to dedicated processors, reducing the stress on the host system's CPU. In addition, storage devices complying with Opal specifications are self-encryption devices. Opal specifications also feature boot authentication. When the drive is being accessed, the shadow MBR will request the drive password at boot. The drive will only unlock and decrypt if the correct password is supplied. The other feature is LBA-specific permissions. Users are assigned different permissions for LBA ranges created by the device administrator. Each LBA range is password-protected and can only be accessed by users with the correct key to perform permitted actions (read/write/erase).

7.3 Thermal Sensor

Apacer Thermal Sensor is a digital temperature sensor with serial interface. By using designated pins for transmission, storage device owners are able to read temperature data.

7.4 Thermal Throttling

Thermal throttling can monitor the temperature of the SSD equipped with a built-in thermal sensor via S.M.A.R.T. commands. This method can ensure the temperature of the device stays within temperature limits by drive throttling, i.e. reducing the speed of the drive when the device temperature reaches the threshold level, so as to prevent overheating, guarantee data reliability, and prolong product lifespan. When the temperature exceeds the maximum threshold level, thermal throttling will be triggered to reduce performance step by step to prevent hardware components from being damaged. Performance is only permitted to drop to the extent necessary for recovering a stable temperature to cool down the device's temperature. Once the temperature decreases to the minimum threshold value, transfer speeds will rise back to its optimum performance level.

7.5 Sidefill

Apacer's Sidefill technology strengthens the connections between solder joints and their board, making them more robust and vibration-resistant. It also allows for heat dissipation to offset thermal damage.

7.6 End-to-End Data Protection

End-to-End Data Protection is a feature implemented in Apacer SSD products that extends error control to cover the entire path from the host computer to the drive and back, and ensure data integrity at multiple points in the path to enable reliable delivery of data transfers. Unlike ECC which does not exhibit the ability to determine the occurrence of errors throughout the process of data transmission, End-to-End Data Protection allows SSD controller to identify an error created anywhere in the path and report the error to the host computer before it is written to the drive. This error-checking and error-reporting mechanism therefore guarantees the trustworthiness and reliability of the SSD.

7.7 CoreGlacier™

In many applications, SSDs are subject to challenging conditions. If the working environment is already hot, and the SSD's operation causes it to increase in temperature as well, the result could be damage to the hardware or corrupted data. In cases like this, leading industrial manufacturers know to turn to Apacer. Apacer developed CoreGlacier, a heatsink that distributes dissipation in isolated components with no thermal diffusion, to prevent heat-related damage from occurring.

8. Software Interface

8.1 Command Set

Table 8-1 summarizes the commands supported by PV250-M280.

Table 8-1 Admin Commands

| Opcode | Command Description |
|--------|-----------------------------|
| 00h | Delete I/O Submission Queue |
| 01h | Create I/O Submission Queue |
| 02h | Get Log Page |
| 04h | Delete I/O Completion Queue |
| 05h | Create I/O Completion Queue |
| 06h | Identify |
| 08h | Abort |
| 09h | Set Features |
| 0Ah | Get Features |
| 0Ch | Asynchronous Event Request |
| 10h | Firmware Commit |
| 11h | Firmware Image Download |
| 14h | Device Self-test |

Table 8-2 Admin Commands – NVM Command Set Specific

| Opcode | Command Description |
|--------|---------------------|
| 80h | Format NVM |
| 81h | Security Send |
| 82h | Security Receive |
| 84h | Sanitize |

Note: 81h and 82h are only applicable to models with TCG Opal support.

Table 8-3 NVM Commands

| Opcode | Command Description |
|--------|---------------------|
| 00h | Flush |
| 01h | Write |
| 02h | Read |
| 04h | Write Uncorrectable |
| 05h | Compare |
| 08h | Write Zeroes |
| 09h | Dataset Management |

8.2 S.M.A.R.T.

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

Table 8-4 SMART (02h)

| Byte | Length | Description |
|---------|--------|---|
| 0 | 1 | Critical Warning |
| 1-2 | 2 | Composite Temperature |
| 3 | 1 | Available Spare |
| 4 | 1 | Available Spare Threshold |
| 5 | 1 | Percentage Used (Average Erase Count / P/E Cycle Count) |
| 6-31 | 26 | Reserved |
| 32-47 | 16 | Data Units Read |
| 48-63 | 16 | Data Units Written |
| 64-79 | 16 | Host Read Commands |
| 80-95 | 16 | Host Write Commands |
| 96-111 | 16 | Controller Busy Time |
| 112-127 | 16 | Power Cycles |
| 128-143 | 16 | Power On Hours |
| 144-159 | 16 | Unsafe Shutdowns |
| 160-175 | 16 | Media and Data Integrity Errors |
| 176-191 | 16 | Number of Error Information Log Entries |
| 192-195 | 4 | Warning Composite Temperature Time |
| 196-199 | 4 | Critical Composite Temperature Time |
| 200-201 | 2 | Temperature Sensor 1: Controller Temperature |
| 202-203 | 2 | Temperature Sensor 2: PCB Temperature |
| 204-205 | 2 | Temperature Sensor 3: NAND Flash Temperature |
| 206-207 | 2 | Temperature Sensor 4 |
| 208-209 | 2 | Temperature Sensor 5 |
| 210-211 | 2 | Temperature Sensor 6 |
| 212-213 | 2 | Temperature Sensor 7 |
| 214-215 | 2 | Temperature Sensor 8 |
| 216-511 | 296 | Reserved |

Note: Temperature display of the Temperature Sensor from 1 to 8 (corresponding bytes from 200 to 215) is not supported if the return value is 0h.

Table 8-5 SMART (C0h)

| Byte | Length | Description |
|---------|--------|-----------------------------|
| 0-255 | 256 | Reserved |
| 256-257 | 2 | SSD Protect Mode |
| 258-261 | 4 | Host Read UNC Count |
| 262-265 | 4 | Reserved |
| 266-269 | 4 | CRC Error Count |
| 270-273 | 4 | Total Early Bad Block Count |
| 274-277 | 4 | Total Later Bad Block Count |
| 278-281 | 4 | Max Erase Count |
| 282-285 | 4 | Average Erase Count |
| 286-289 | 4 | Program Fail Count |
| 290-293 | 4 | Erase Fail Count |
| 294-301 | 8 | Flash Write Sector |
| 302-305 | 4 | Total Spare Block |
| 306-309 | 4 | Current Spare Block |
| 310-313 | 4 | Read Retry Count |
| 314-511 | 210 | Reserved |

9. Electrical Specifications

9.1 Operating Voltage

Table 9-1 lists the supply voltage for PV250-M280.

Table 9-1 Operating Range

| Item | Range |
|----------------|-----------|
| Supply Voltage | 3.3V ± 5% |

9.2 Power Consumption

Table 9-2 lists the power consumption for PV250-M280.

Table 9-2 Power Consumption

| Capacity | | Unit | 240 GB | 480 GB | 960 GB | 1920 GB | 3840 GB |
|---------------|----|------|--------|--------|--------|---------|---------|
| Mode | | | | | | | |
| Active (Max.) | mA | | 985 | 1,190 | 1,220 | 1,260 | 1,595 |
| Idle | | | 240 | 240 | 240 | 240 | 230 |

Notes:

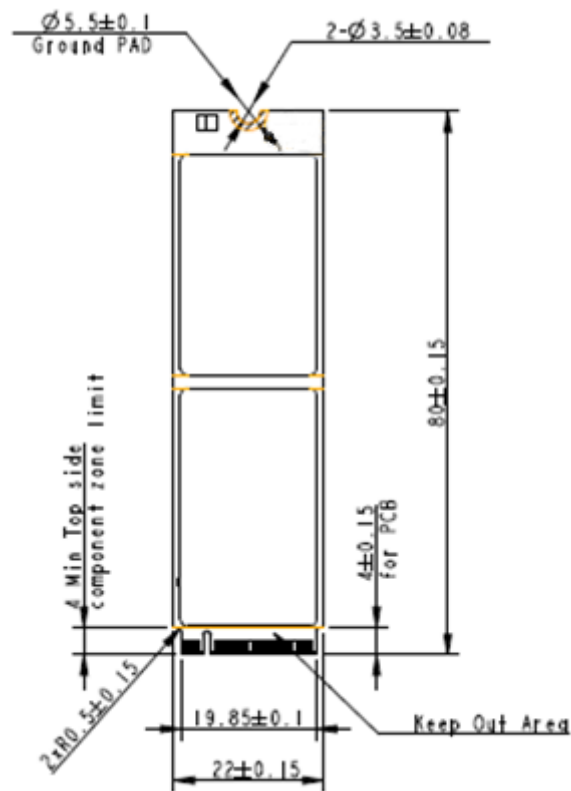
- All values are typical and may vary depending on flash configurations or host system settings.
- Power consumption is measured using CrystalDiskMark 8.0.4 with file size 1,000MB.

10. Mechanical Specifications

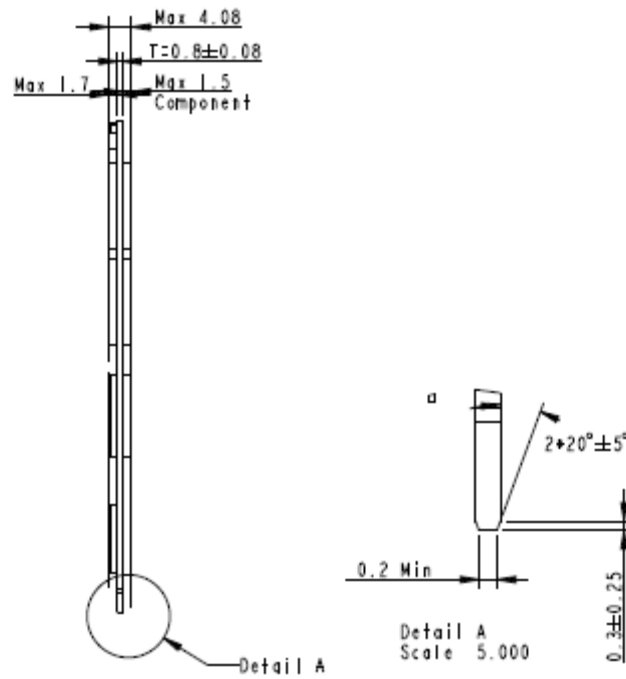
Table 10-1 Physical Information

| Parameter | Unit | 240 GB | 480 GB | 960 GB | 1920 GB | 3840 GB |
|---------------|--------|--------------|--------|--------|---------|---------|
| Length | mm | 80.00 ± 0.15 | | | | |
| Width | | 22.00 ± 0.15 | | | | |
| Height (Max.) | | 4.08 | | | | |
| Weight | g ± 5% | 6.29 | 7.13 | 7.19 | 7.8 | 7.33 |

Top View



Side View



Bottom side

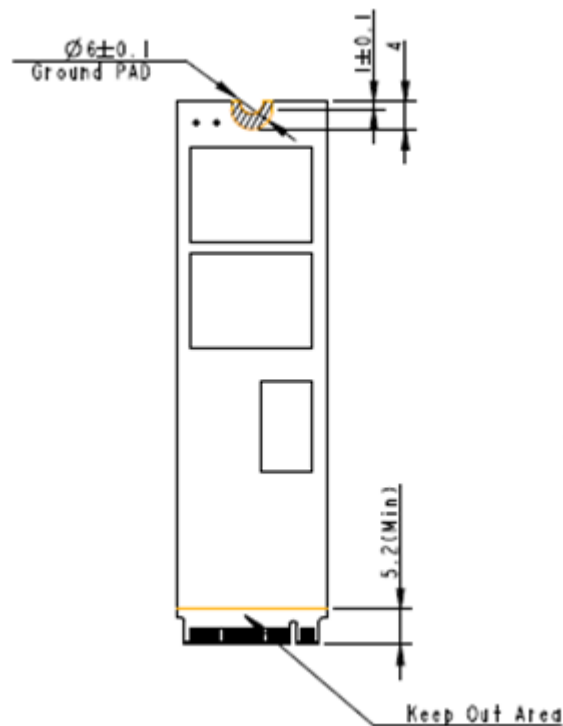


Figure 10-1 Physical Dimensions

11. Product Ordering Information

11.1 Product Code Designations

Apacer's PV250-M280 SSD is available in different configurations and densities. See the chart below for a comprehensive list of options for the PV250-M280 series devices.

| Code | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|
| | B | 9 | 2 | . | X | X | 5 | X | X | U | . | 0 | 0 | 1 | X | X |

| | |
|--|---|
| Code 1-3 (Product Line & Form Factor) | PCIe M.2 2280 |
| Code 5-6 (Model/Solution) | 25: PV250 A7: PV250 with TCG Opal |
| Code 7-8 (Product Capacity) | 5J: 240GB 5K: 480GB 5L: 960GB 5M: 1920GB 5N: 3840GB |
| Code 9 (Flash Type & Product Temp) | G: 3D TLC Standard Temperature H: 3D TLC Wide Temperature |
| Code 10 (Product Spec) | Double-sided M key with graphene |
| Code 12-14 (Version Number) | Random numbers generated by system |
| Code 15-16 (Firmware Version) | 02/03: Thermal Sensor OP |

11.2 Valid Combinations

The following tables list the available models of the PV250-M280 series which are in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

11.2.1 Without TCG Opal

| Capacity | Standard Temperature | Wide Temperature |
|----------|----------------------|------------------|
| 240GB | B92.255JGU.00121 | B92.255JHU.00121 |
| 480GB | B92.255KGU.00121 | B92.255KHU.00121 |
| 960GB | B92.255LGU.00121 | B92.255LHU.00121 |
| 1920GB | B92.255MGU.00121 | B92.255MHU.00121 |
| 3840GB | B92.255NGU.00102 | N/A |

11.2.2 With TCG Opal (optional)

| Capacity | Standard Temperature | Wide Temperature |
|----------|----------------------|------------------|
| 240GB | B92.A75JGU.00120 | B92.A75JHU.00120 |
| 480GB | B92.A75KGU.00120 | B92.A75KHU.00120 |
| 960GB | B92.A75LGU.00120 | B92.A75LHU.00120 |
| 1920GB | B92.A75MGU.00120 | B92.A75MHU.00120 |

Revision History

| Revision | Description | Date |
|----------|--|------------|
| 0.1 | Preliminary release | 12/23/2022 |
| 1.0 | - Updated Performance, Endurance and Power Consumption on Specifications Overview page - Updated Table 4-2, 4-4 and 9-2 | 3/16/2023 |
| 1.1 | Removed Power Failure Management from and added DataDefender to Flash Management | 4/7/2023 |
| 1.2 | - Removed product photo without graphene sheet from the cover page - Removed without-graphene-sheet dimensions from 10. Mechanical Specifications | 4/27/2023 |
| 1.3 | - Updated product photo on the cover page and 4.7 LED Indicator Behavior - Removed LED B from 4.7 LED Indicator Behavior | 4/28/2023 |
| 1.4 | - Added 1920GB support - Added NVMe Secure Erase and End-to-End Data Protection support | 6/1/2023 |
| 1.5 | Added CoreGlacier support | 8/4/2023 |
| 1.6 | Added rear view of the product to the cover page | 9/27/2023 |
| 1.7 | Updated rear view of the product to the cover page | 10/31/2023 |
| 1.8 | Added UL to 4.5 Certification and Compliance | 11/28/2023 |
| 1.9 | Added 3840GB support | 12/28/2023 |
| 2.0 | - Added TCG Opal support (optional) - Updated Performance on Specifications Overview page and Table 4-2 - Updated endurance for 1920GB on Specifications Overview page and Table 4-4 - Updated power consumption for 240GB-1920GB at Table 9-2 - Updated 11. Product Ordering Information by changing firmware code (code 15-16) for 240GB-1920GB and adding 11.2.2 With TCG Opal (optional) | 2/21/2024 |

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