RoHS Compliant

PCI Express Flash Drive

PM110-25 2.5” Product Specifications

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Version 1.4

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Features:

- **PCIe Interface**
  - Compliant with NVMe 1.2
  - Compatible with PCIe I/II/III x 4 interface
- **Capacity**
  - 128, 256, 512 GB
  - 1 TB
- **Performance***
  - Burst read/write: 4 GB/sec
  - Sequential read: up to 2,815 MB/sec
  - Sequential write: up to 1,475 MB/sec
  - Random read (4K): up to 296,000 IOPS
  - Random write (4K): up to 238,000 IOPS
- **Flash Management**
  - Built-in hardware ECC
  - Global Wear Leveling
  - Flash bad block management
  - S.M.A.R.T.
  - Power Failure Management
  - TRIM
- **NAND Flash Type:** MLC
- **MTBF (hours):** >1,000,000
- **Endurance (Est.)**
  - 128 GB: 157 TBW
  - 256 GB: 314 TBW
  - 512 GB: 628 TBW
  - 1 TB: 1,256 TBW
- **Temperature Range**
  - Operating: 0°C to 70°C
  - Storage: -40°C to 85°C
- **Supply Voltage**
  - 5 V ± 5%
- **Power Consumption***
  - Active mode: 540 mA
  - Idle mode: 105 mA
- **Form Factor**
  - 2.5 inch (100.00 x 69.85 x 9.50, unit: mm)
- **Connector**
  - U.2 (SFF-8639)
- **Shock & Vibration****
  - Shock: 1,500 G
  - Vibration: 15 G
- **DDR3 Cache for Enhanced Random Performance**
- **Thermal Sensor**
- **Thermal Management Technique**
- **End-to-End Data Protection**
- **RoHS Compliant**

*Varies from capacities. The values presented for Performances and Power Consumption are typical and may vary depending on different configurations and platforms.
**Non-operating

Table of Contents

1. Product Description

1.1 Introduction

Apacer PM110-25 (2.5 inch) Embedded Solid State Drive is a speedy and reliable companion for industrial PC and laptops. Designed in PCIe Gen3 x4 interface, the drive can deliver outstanding performance up to 2,815 MB/s sustained transfer rate, highly suitable to serve as operating system boot drive or storage media of important data. With its compliance with the latest PCIe specification, this cutting edge device supports power management, which greatly saves in power consumption, making it more environmental and economical than traditional hard disk drives.

Regarding data reliability, the controller unit of PM110-25 is built with a powerful ECC engine in the device correcting up to 120 bit per 2KB data. For better I/O performance, the controller unit comes with an external DDR3 cache to strengthen the IOPS (Input Output Per Second) of the device, proving to be the ideal companion for PC and laptop users.

1.2 Capacity Specifications

Table 1-1 Capacity Specifications

Capacity	Total Bytes*	Cylinders	Heads	Sectors	Max LBA**
128 GB	128,035,676,160	16,383	16	63	250,069,680
256 GB	256,060,514,304	16,383	16	63	500,118,192
512 GB	512,110,190,592	16,383	16	63	1,000,215,216
1 TB	1,024,209,543,168	16,383	16	63	2,000,409,264

*Display of total bytes varies from file systems.
**Cylinders, heads or sectors are not applicable for these capacities. Only LBA addressing applies.
***Notes: 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.
LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

1.3 Performance

Table 1-2 Performance Specifications

Performance \ Capacity	128 GB	256 GB	512 GB	1 TB
Sequential Read* (MB/s)	2,395	2,775	2,815	2,795
Sequential Write* (MB/s)	735	1,390	1,475	1,470
Random Read IOPS (4K)**	126,000	279,000	296,000	274,000
Random Write IOPS (4K)**	100,000	157,000	238,000	236,000

Note:
Results may differ from various flash configurations or host system setting.
*Sequential performance is based on CrystalDiskMark 5.2.1 with file size 1,000MB.
**Random performance measured using IOMeter with Queue Depth 32.

1.4 Pin Assignments

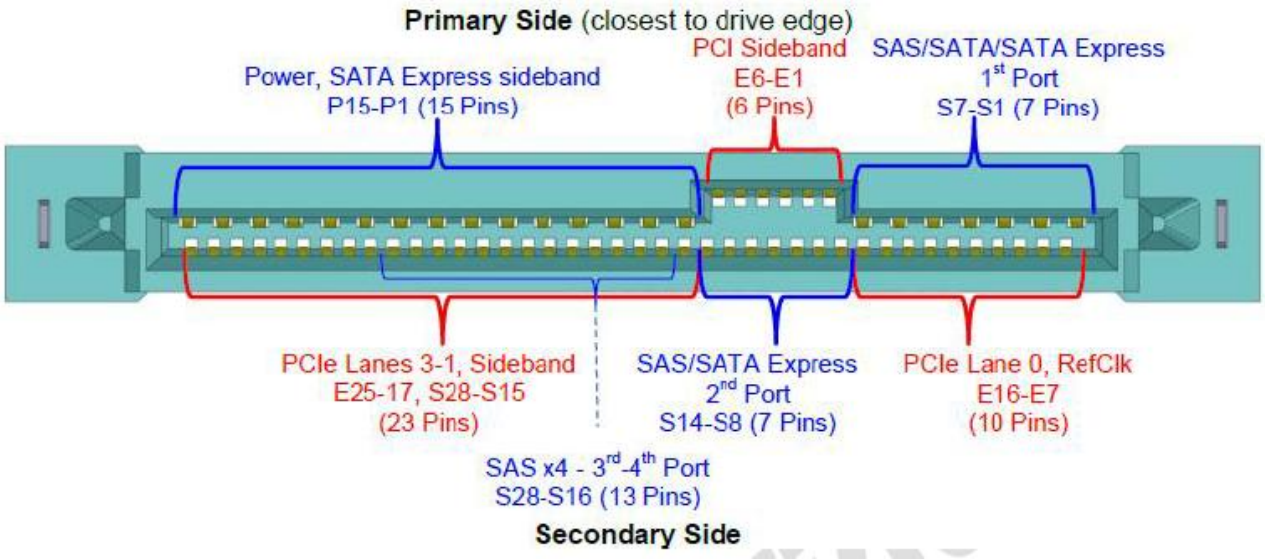


Figure 1-1 PCIe SSD Pin Locations

Table 1-3 Pin Assignments

Pin Number	Name	Type	Description
P1	WAKE#	Input	Signal for Link reactivation
P2	-	-	Outside scope of this specification
P3	CLKREQ#	Bi-Dir	Clock request
P4	IfDet#	Input	Interface Type Detect
P5	Ground	Ground	Ground
P6	Ground	Ground	Ground
P7	-	-	Outside scope of this specification
P8	-	-	Outside scope of this specification
P9	-	-	Outside scope of this specification
P10	PRSNT#	Input	Presence detect
P11	Activity	Input	-
P12	Ground	Ground	Ground
P13	+12V Precharge	Power	+12V Precharge power for SFF-8639 module
P14	+12V	Power	+12V power for SFF-8639 module
P15	+12V	Power	+12V power for SFF-8639 module
S1	Ground	Ground	Ground
S2	-	-	Outside scope of this specification
S3	-	-	Outside scope of this specification
S4	Ground	Ground	Ground
S5	-	-	Outside scope of this specification
S6	-	-	Outside scope of this specification

Pin Number	Name	Type	Description
S7	Ground	Ground	Ground
S8	Ground	Ground	Ground
S9	-	-	Outside scope of this specification
S10	-	-	Outside scope of this specification
S11	Ground	Ground	Ground
S12	-	-	Outside scope of this specification
S13	-	-	Outside scope of this specification
S14	Ground	Ground	Ground
S15	Reserved	-	Reserved
S16	Ground	Ground	Ground
S17	PETp1	Diff-Pair	Transmitter differential pair, Lane 1
S18	PETn1	Diff-Pair	Transmitter differential pair, Lane 1
S19	Ground	Ground	Ground
S20	PERn1	Diff-Pair	Receiver differential pair, Lane 1
S21	PERp1	Diff-Pair	Receiver differential pair, Lane 1
S22	Ground	Ground	Ground
S23	PETp2	Diff-Pair	Transmitter differential pair, Lane 2
S24	PETn2	Diff-Pair	Transmitter differential pair, Lane 2
S25	Ground	Ground	Ground
S26	PERn2	Diff-Pair	Receiver differential pair, Lane 2
S27	PERp2	Diff-Pair	Receiver differential pair, Lane 2
S28	Ground	Ground	Ground
E1	REFCLKB+	Diff-Pair	Reference clock (differential pair) for second X2 port
E2	REFCLKB-	Diff-Pair	Reference clock (differential pair) for second X2 port
E3	+3.3 Vaux	Power	3.3 V auxiliary power
E4	PERSTB#	Output	Fundamental reset for second X2 port
E5	PERST#	Output	Fundamental reset (if dual-port enabled, first X2 port)
E6	Reserved	-	Reserved
E7	REFCLK+	Diff-Pair	Reference clock (if dual-port enabled, first X2 port)
E8	REFCLK-	Diff-Pair	Reference clock (if dual-port enabled, first X2 port)
E9	Ground	Ground	Ground
E10	PETp0	Diff-Pair	Transmitter differential pair, Lane 0
E11	PETn0	Diff-Pair	Transmitter differential pair, Lane 0
E12	Ground	Ground	Ground
E13	PERn0	Diff-Pair	Receiver differential pair, Lane 0
E14	PERp0	Diff-Pair	Receiver differential pair, Lane 0
E15	Ground	Ground	Ground
E16	Reserved	-	Reserved
E17	PETp3	Diff-Pair	Transmitter differential pair, Lane 3
E18	PETn3	Diff-Pair	Transmitter differential pair, Lane 3

Pin Number	Name	Type	Description
E19	Ground	Ground	Ground
E20	PERn3	Diff-Pair	Receiver differential pair, Lane 3
E21	PERp3	Diff-Pair	Receiver differential pair, Lane 3
E22	Ground	Ground	Ground
E23	SMCLK	Bi-Dir	SMBus (System Management Bus) clock
E24	SMDAT	Bi-Dir	SMBus (System Management Bus) data
E25	DualPortEn#	Output	Dual-port Enable

2. Software Interface

2.1 Command Set

Table 2-1 Admin Commands

Opcode	Command Description
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Features
0Ah	Get Features
0Ch	Asynchronous Event Request
10h	Firmware Activate
11h	Firmware Image Download

Table 2-2 Admin Commands – NVM Command Set Specific

Opcode	Command Description
80h	Format NVM
81h	Security Send
82h	Security Receive

Table 2-3 NVM Commands

Opcode	Command Description
00h	Flush
01h	Write
02h	Read
04h	Write Uncorrectable
05h	Compare
08h	Write Zeroes
09h	Dataset Management

2.2 S.M.A.R.T.

S.M.A.R.T. is an acronym for Self-Monitoring, Analysis and Reporting Technology, an open standard allowing disk drives to automatically monitor their own health and report potential problems. It protects the user from unscheduled downtime by monitoring and storing critical drive performance and calibration parameters. Ideally, this should allow taking proactive actions to prevent impending drive failure.

3. Flash Management

3.1 Error Correction/Detection

This device implements hardware ECC scheme based on the BCH algorithm which can detect and correct up to 120 bits error in 2K Bytes.

3.2 Flash Block Management

Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. When host performs program/erase command on a block, bad block may appear in Status Register. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, block mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

3.3 Global Wear Leveling

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Global wear leveling is an important mechanism that level out the wearing of all blocks so that the wearing-down of all blocks can be almost evenly distributed. This will increase the lifespan of SSDs.

3.4 Power Failure Management

Power Failure Management plays a crucial role when experiencing unstable power supply. Power disruption may occur when users are storing data into the SSD. In this urgent situation, the controller would run multiple write-to-flash cycles to store the metadata for later block rebuilding. This urgent operation requires about several milliseconds to get it done. At the next power up, the firmware will perform a status tracking to retrieve the mapping table and resume previously programmed NAND blocks to check if there is any incompleteness of transmission.

Note: The controller unit of this product model is designed with a DRAM as a write cache for improved performance and data efficiency. Though unlikely to happen in most cases, the data cached in the volatile DRAM might be potentially affected if a sudden power loss takes place before the cached data is flushed into non-volatile NAND flash memory.

3.5 TRIM

TRIM is a SATA command that helps improve the read/write performance and efficiency of solid-state drives (SSD). The command enables the host operating system to inform SSD controller which blocks contain invalid data, mostly because of the erase commands from host. The invalid will be discarded permanently and the SSD will retain more space for itself.

3.6 Thermal Sensor

Apacer Thermal Sensor is a digital temperature sensor with serial interface. By using designated pins for transmission, storage device owners are able to read temperature data.

3.7 Thermal Management Technique

Thermal management technique can monitor the temperature of the SSD equipped with a built-in thermal sensor via S.M.A.R.T. commands. This method can ensure the temperature of the device stays within temperature limits by drive throttling, i.e. reducing the speed of the drive when the device temperature reaches the threshold level, so as to prevent overheating, guarantee data reliability, and prolong product lifespan. When the temperature exceeds the maximum threshold level, thermal throttling will be triggered to reduce performance step by step to prevent hardware components from being damaged. Performance is only permitted to drop to the extent necessary for recovering a stable temperature to cool down the device's temperature. Once the temperature decreases to the minimum threshold value, transfer speeds will rise back to its optimum performance level.

3.8 End-to-End Data Protection

End-to-End Data Protection provides full error detection covering the whole data pass between the host computer system and the internal storage media. It ensures data integrity by protecting against possible data corruption in the NAND, SRAM, and DRAM memory. Protected information is attached to the data or may be LBA-rooted. In the SSD concept, it stays in the data, travelling from the host, through the SSD flash controller, and then to the NAND flash media. When the user reads the data later, the same protected information travels the same route back and eventually returns to the host computer system. This measure is implemented to ensure data correctness everywhere in the read/write route.

With End-To-End Protection, errors, especially soft errors, can be located and isolated at any point during the data read/write route. Once an error is detected, an immediate attempt will be made to correct it, and any uncorrectable error will be reported to the host. It is two-way security rather than one-way, which offers a more comprehensive detection and prevents ECC failure.

4. Reliability Specifications

4.1 Environments

Table 4-1 Environmental Specifications

Environment		Specifications
Temperature	Operating	0°C to 70°C
	Storage	-40°C to 85°C
Vibration		Non-operating: Sine wave, 15(G), 10~2000(Hz), Operating: Random, 7.69 (Grms), 20~2000(Hz)
Shock		Non-operating: Acceleration, 1,500 G, 0.5 ms Operating: Peak acceleration, 50 G, 11 ms

Note: Shock and Vibration specifications are subject to change without notice.

4.2 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in SFD drive. The prediction result for PM110-25 is more than 1,000,000 hours.

Note: The MTBF is predicated and calculated based on “Telcordia Technologies Special Report, SR-332, Issue 2” method.

4.3 Certification and Compliance

PM110-25 complies with the following standards:

- FCC: CISPR22
- CE: EN55022
- BSMI 13438
- RoHS
- PCI Express Base 3.0
- UNH-IOL NVM Express Logo

4.4 Endurance (Est.)

The endurance of a storage device is predicted by Tera Bytes Written based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

Capacity	Tera Bytes Written
128 GB	157
256 GB	314
512 GB	628
1 TB	1,256

Note:

- Samples are built using Toshiba 15nm Toggle MLC NAND flash.
- The measurement assumes the data written to the SSD for test is under a typical and constant rate.
- The measurement follows the standard metric: 1 TB (Terabyte) = 1,000 GB.
- The measurement follows JEDEC JESD-219 standard to test WAF.
- This estimation complies with JEDEC JESD-219, enterprise endurance workload of random data with payload size distribution.
- The endurance of SSD could be estimated based on user behavior, NAND endurance cycles, and write amplification factor. It is not guaranteed by flash vendor.

5. Electrical Characteristics

5.1 Operating Voltage

Table 5-1 lists the supply voltage for PM110-25.

Table 5-1 Operating Voltage

Parameter	Conditions
Supply Voltage	5V ± 5%

5.2 Power Consumption

Table 5-2 lists the power consumption PM110-25.

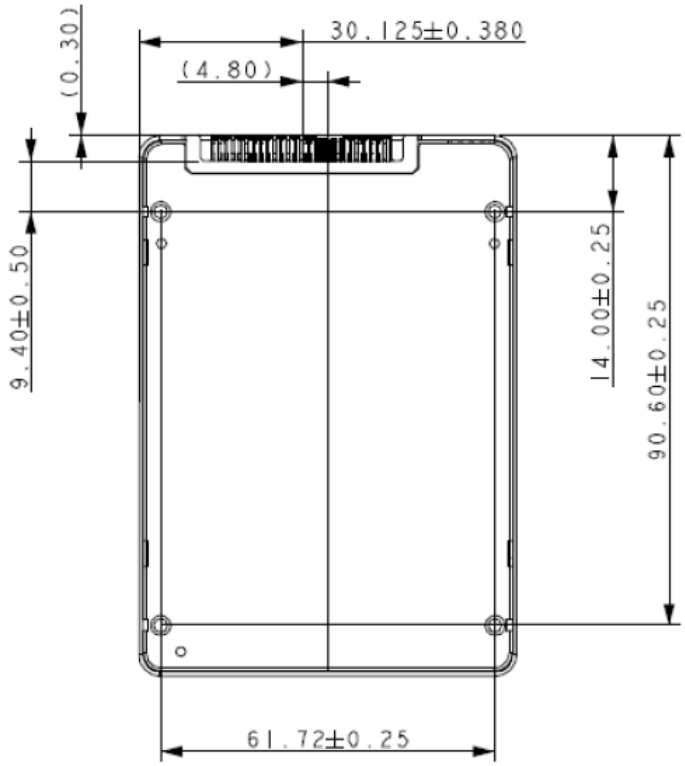
Table 5-2 Power Consumption

Capacity / Mode	128 GB	256 GB	512 GB	1 TB
Active (mA)	390	430	520	540
Idle (mA)	100	105	105	100

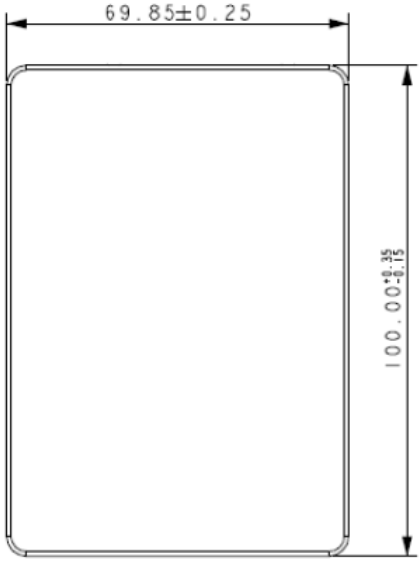
Note:
*All values are typical and may vary depending on flash configurations or host system settings.
**Active power is an average power measurement performed using CrystalDiskMark with 128KB sequential read/write transfers.

6. Mechanical Specifications

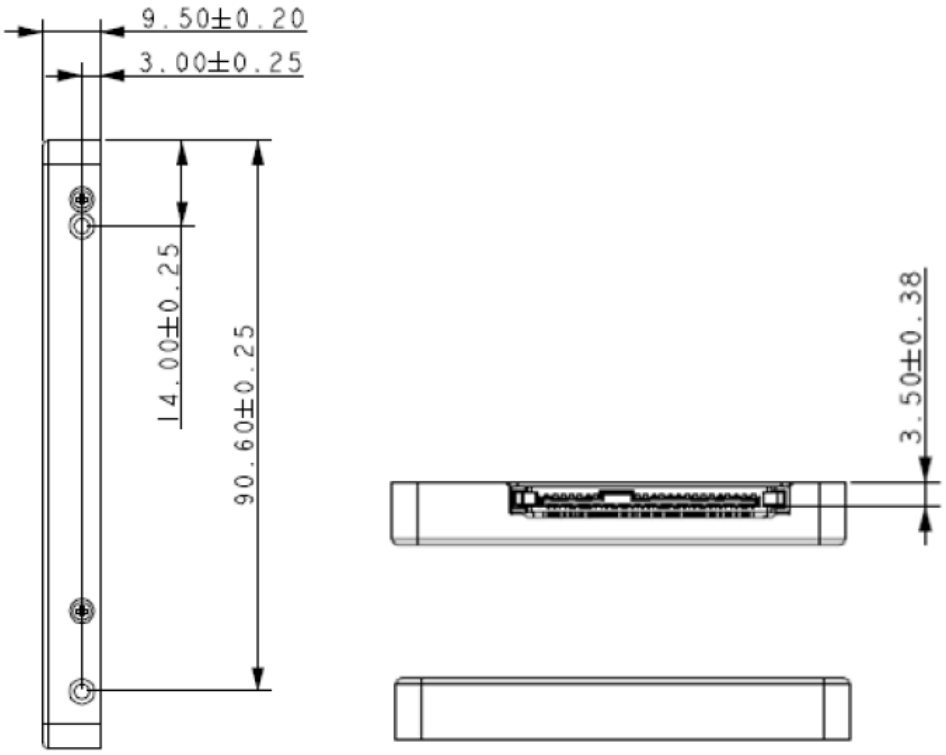
Bottom View



Top View



Side View



Unit: mm
Tolerance: ±0.2

7. Product Ordering Information

7.1 Product Code Designation

AP P xxxX 3 AH - 01 T T

Operating Temperature Range
T: 0°C to 70°C

Flash Type

Version Control

U.2

Capacity
128G = 128GB
256G = 256GB
512G = 512GB
001T = 1TB

PCIe

Apacer Product Code

7.2 Valid Combinations

Capacity	Part Number
128GB	APP128G3AH-01TT
256GB	APP256G3AH-01TT
512GB	APP512G3AH-01TT
1TB	APP001T3AH-01TT

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Revision History

Revision	Description	Date
0.1	Preliminary release.	7/22/2016
0.2	- Revised capacity range to 128GB-1TB - Updated performance and power consumption values - Updated product ordering information	12/2/2016
1.0	- Added product photo to Features page - Updated endurance ratings	12/26/2016
1.1	Added “Thermal Sensor/Thermal Throttling FW” and “End-to-End Data Protection” to Features page	1/5/2017
1.2	- Separated Thermal Throttling from Thermal Sensor on Features page - Revised ECC to 120 bits/2KB - Removed 3.6 Over Provision	1/11/2017
1.3	Added 3.7 Thermal Management Technique and 3.8 End-to-End Data Protection	4/13/2017
1.4	Updated capacity at 7.1 Product Code Designations	6/22/2017

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