

RoHS Compliant

PCI Express BGA Solid State Drive

Industrial PV180- μ SSD Product Specifications

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Specifications Overview:

- **PCIe Interface**
 - Compliant with PCI Express 4.0
 - Compliant with NVMe 1.4
 - Compatible with PCIe Gen4 x4 interface
- **Capacity**
 - 240, 480, 960 GB
- **Performance¹**
 - Interface burst read/write: 2 GB/sec
 - Sequential read: up to 3,745 MB/sec
 - Sequential write: up to 3,015 MB/sec
 - Random read (4K): up to 392,000 IOPS
 - Random write (4K): up to 710,000 IOPS
- **Flash Management**
 - Low-Density Parity-Check (LDPC) Code
 - Global Wear Leveling
 - Flash bad-block management
 - Flash Translation Layer: Page Mapping
 - Power Failure Management
 - S.M.A.R.T.
 - TRIM
 - Hyper Cache Technology
 - Over-provisioning
 - DataRAID™
 - NVMe Secure Erase
- **NAND Flash Type: 3D TLC (BiCS5)**
- **MTBF: >1,500,000 hours**
- **Endurance (in drive writes per day: DWPD)**
 - 240 GB: 0.34 DWPD
 - 480 GB: 0.45 DWPD
 - 960 GB: 0.59 DWPD
- **Temperature Range**
 - Operating: -40°C to 85°C
 - Storage: -40°C to 85°C
- **Supply Voltage**
 - 3.3V ± 5% or 2.5V ± 5%
 - 1.2V ± 5%
 - 0.85V ± 5%
- **Power Consumption¹**
 - Active mode (Max.): 1,255 mA
 - Idle mode: 240 mA
- **Security**
 - AES 256-bit hardware encryption
 - Write Protect² (optional)
- **Reliability**
 - Thermal Sensor
 - Thermal Throttling
 - End-to-End Data Protection
- **Form Factor**
 - PCIe BGA SSD (291 Ball)
 - Dimensions (unit: mm):
 - 240 GB: 20.00 x 16.00 x 1.15
 - 480 GB: 20.00 x 16.00 x 1.35
 - 960 GB: 20.00 x 16.00 x 1.65
- **RoHS Compliant**

Notes:

1. Varies from capacities. The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings.
2. Triggered via a hardware pin

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1. General Description

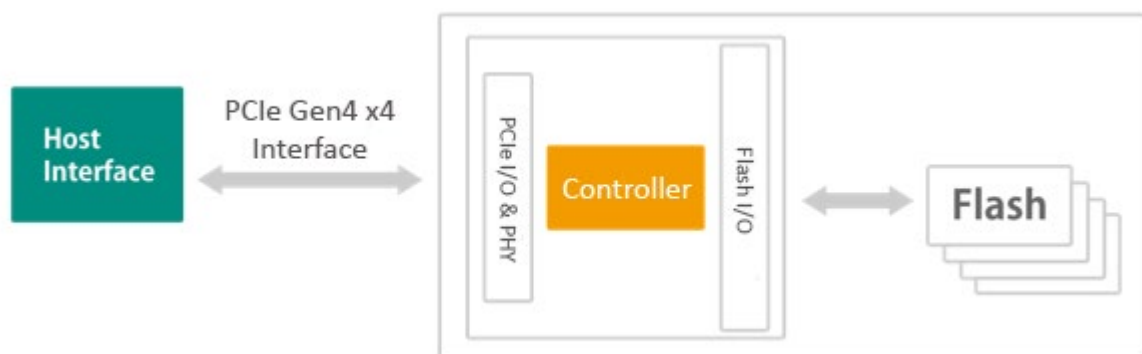
Apacer PCIe BGA SSD PV180- μ SSD presents a revolutionary breakthrough of NAND flash storage technology. This micro sized SSD delivers all the technological benefits in NAND based storage solution with ultra speed PCIe Gen4 x4 interface in an embedded BGA form factor, compatible with JEDEC PCIe M.2 1620. Formed in a size of an IC chip, the performance level can reach up to 3,745 MB/s for read and 3,015 MB/s for write.

PV180- μ SSD is built with a powerful PCIe controller that supports on-the-module ECC as well as efficient wear leveling scheme, and implemented with LDPC (Low Density Parity Check) ECC engine to extend SSD endurance and increase data reliability. Furthermore, PV180- μ SSD is equipped with a built-in thermal sensor to monitor the temperature of the SSD via S.M.A.R.T commands and configured with thermal throttling to dynamically adjust frequency scaling to enhance data reliability and provide sustained performance while overheating. For highly-intensive applications, End-to-End Data Protection ensures that data integrity can be assured at multiple points in the path to enable reliable delivery of data transfers.

Security-wise, Advanced Encryption Standard (AES) ensures data security and provides users with peace of mind knowing their data is safeguarded against unauthorized use at all times. PV180- μ SSD also adopts the latest page mapping file translation layer and comes with various implementations including power saving modes, flash block management, power failure management, TRIM, Hyper Cache technology, over-provisioning, DataRAID and NVMe secure erase.

Apacer PV180- μ SSD boasts micro size, high-speed performance, low power consumption, shock resistance, high stability and reliability. PV180- μ SSD will be adopted by many high-end industrial and 5G high-speed applications, including the Industrial IoT, cloud computing, servers and networking, defense, gaming, and high-performance computing

2. Functional Block



Note: The actual number of NAND flash used on Apacer PV180- μ SSD varies from capacities. The illustration is for reference only.

Figure 2-1 Functional Block Diagram

3. Pin Assignments

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU	A
B	DNU	DNU		DNU		DNU		TVB_REG			DNU		DNU		DNU		DNU	DNU	B
C	GND	GND	GND	GND	GND	DNU	DNU	DNU	DNU	FLASH_RZQ	DNU	DNU	DNU	DNU	GND	DNU	DNU	DNU	C
D				REFCLKP	REFCLKN	GND	PERSTN	CLKREQB	PWR_1	PWR_1	GND	XEXTRSTB	GPIO1	DNU	DNU				D
E	GND	GND	GND	GND	GND	GND	GND	DNU	PWR_1	PWR_1	GND	DNU	GPIO8	GND	GND	DNU	DNU	DNU	E
F				PERP0	PERN0	GND								DNU	GND				F
G	GND	GND	GND	GND	GND		PWR_3	PWR_3	GND	GND	PWR_3	PWR_3		GND	GND	DNU	DNU	DNU	G
H				PETP0	PETN0		PWR_3	PWR_3	GND	GND	PWR_3	PWR_3		GND	PLN				H
J	GND	GND	GND	GND	GND		PWR_3	PWR_3	GND	GND	PWR_3	PWR_3		GND	GND	DNU	DNU	DNU	J
K				PERP1	PERN1		GND	GND	GND	GND	GND	GND		DNU	PLA				K
L	GND	GND	GND	GND	GND		DNU	DNU	DNU	DNU	DNU	DNU		GND	GND	DNU	DNU	DNU	L
M				PETP1	PETN1		DNU	DNU	GND	GND	DNU	DNU		DNU	DNU				M
N	GND	GND	GND	GND	GND		DNU	DNU	DNU	DNU	DNU	DNU		GND	GND	DNU	JTAG_TCK	JTAG_TMS	N
P				PERP2	PERN2		GND	GND	GND	GND	GND	GND		DNU	DNU				P
R	GND	GND	GND	GND	GND		PWR_2	PWR_2	GND	GND	PWR_2	PWR_2		GND	GND	DNU	XGPIO0	DNU	R
T				PETP2	PETN2		PWR_2	PWR_2	GND	GND	PWR_2	PWR_2		DNU	DNU				T
U	GND	GND	GND	GND	GND		PWR_2	PWR_2	GND	GND	PWR_2	PWR_2		GND	GND	DNU	SMB_CLK	SMB_DATA	U
V				PERP3	PERN3									DNU	DNU				V
W	GND	GND	GND	GND	GND	GND	LEDVAB	DNU	PWR_1	PWR_1	GND	DNU	DNU	GND	GND	DNU	DNU	DNU	W
Y				PETP3	PETN3	GND	DNU	DNU	PWR_1	PWR_1	GND	DNU	GND	DNU	DNU				Y
AA	GND	GND	GND	GND	GND	DNU	DNU	DNU	DNU	CTL_RZQ	DNU	DNU	DNU	GND	GND	DNU	DNU	DNU	AA
AB	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU	AB
AC	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU	AC

Table 3-1 Pin Layout

Table 3-1 Pin Assignments

Pin Name	BGA 291	Pin Type	Description	IO Voltage
UART/GPIO				
XGPIO0	R17	I	Debug only	1.8V
GPIO1	D13	I	Debug only	1.8V
GPIO3	E13	O	Debug only	1.8V
SMB_CLK	U17	I/O	Debug only	1.8V
SMB_DATA	U18	I/O	Debug only	1.8V
JTAG_TCK	N17	I/O	Debug only	1.8V
JTAG_TMS	N18	I/O	Debug only	1.8V
XEXTRSTB	D12	-	Debug only	1.8V
1V8_REG	B8	-	Debug only	1.8V
GPIO6_WP (DNU)	AB6	I	Do not connect to any other signal or cap or resistor, left test pad only. Or refer to Section 3.10 of Design Guide if the WP function is used.	1.8V
PCIe Interface Signals				
PERP0	F4	I/O	PCIe TX/RX Differential signals defined by the PCI Express Card Electromechanical Specification.	--
PERN0	F5			
PERP1	K4			
PERN1	K5			
PERP2	P4			
PERN2	P5			
PERP3	V4			
PERN3	V5			
PETP0	H4			
PETN0	H5			
PETP1	M4			
PETN1	M5			
PETP2	T4			
PETN2	T5			
PETP3	Y4			
PETN3	Y5			
REFCLKP	D4	I	PCIe Reference Clock signals (100 MHz) defined by the PCI Express Card Electromechanical Specification.	--
REFCLKN	D5	I		--
PERST#	D7	I	PCIe Reset is a functional reset to the card as defined by the PCI Express Mini Card Electromechanical Specification.	1.8V

Pin Name	BGA 291	Pin Type	Description	IO Voltage
CLKREQ#	D8	I/O	Clock Request is a reference clock request signal as defined by the PCI Express Mini Card Electromechanical Specification; Also used by L1 PM Substates.	1.8V
Optional Signals				
FLASH_RZQ	C10	I	Flash Calibration REF RESISTENCE	-
CTL_RZQ	AA10	I	Control Calibration REF RESISTENCE	-
PLA_S3#	K15	O	Power Loss Acknowledge	1.8V
PLN#	H15	I	Power Loss Notification	1.8V
SSD Specific Signals				
LED_1#	W7	O	Open drain, active low signal. This signal is used to allow the Adapter to provide status indication via LED device that will be provided by the system.	3.3V
Power Supply Signals				
PWR_1	D9	I	+3.3V or +2.5V source	3.3V 2.5V
	D10			
	E9			
	E10			
	W9			
	W10			
	Y9			
	Y10			
PWR_2	R7	I	+1.2V source	1.2V
	R8			
	R11			
	R12			
	T7			
	T8			
	T11			
	T12			
	U7			
	U8			
	U11			
	U12			
PWR_3	G7	I	+0.85V source	0.85V
	G8			
	G11			
	G12			

Pin Name	BGA 291	Pin Type	Description	IO Voltage
	H7			
	H8			
	H11			
	H12			
	J7			
	J8			
	J11			
	J12			

Pin Name	BGA 291	Description
	C1	
	C2	
	C3	
	C4	
	C5	
	C15	
	D6	
	D11	
	E1	
	E2	
	E3	
	E4	
	E5	
GND	E6	GND
	E7	
	E11	
	E14	
	E15	
	F6	
	F15*	
	G1	
	G2	
	G3	
	G4	
	G5	
	G9	

Pin Name	BGA 291	Description
	G10	
	G14	
	G15	
	H9	
	H10	
	H14*	
	J1	
	J2	
	J3	
	J4	
	J5	
	J9	
	J10	
	J14	
	J15	
	K7	
	K8	
	K9	
	K10	
GND	K11	GND
	K12	
	L1	
	L2	
	L3	
	L4	
	L5	
	L14	
	L15	
	M9	
	M10	
	N1	
	N2	
	N3	
	N4	
	N5	

Pin Name	BGA 291	Description
	N14	
	N15	
	P7	
	P8	
	P9	
	P10	
	P11	
	P12	
	R1	
	R2	
	R3	
	R4	
	R5	
	R9	
	R10	
	R14	
	R15	
	T9	
	T10	
GND	U1	GND
	U2	
	U3	
	U4	
	U5	
	U9	
	U10	
	U14	
	U15	
	W1	
	W2	
	W3	
	W4	
	W5	
	W6	
	W11	

Pin Name	BGA 291	Description
	W14	
	W15	
	Y6	
GND	Y11	GND
	Y13	
	AA1	
	AA2	
	AA3	
	AA4	
	AA5	
	AA14	
	AA15	
DNU	A1	Do not use. Manufacturing purpose only.
	A2	
	A4	
	A6	
	A8	
	A11	
	A13	
	A15	
	A17	
	A18	
	B1	
	B2	
	B4	
	B6	
	B11	
	B13	
	B15	
	B17	
	B18	
	C6	
	C7	
C8		
C9		

Pin Name	BGA 291	Description
	C11	
	C12	
	C13*	
	C14*	
	C16	
	C17	
	C18	
	D14	
	D15*	
	E8	
	E12	
	E16	
	E17	
	E18	
	F14	
	G16	
	G17	
	G18	
	J16	
DNU	J17	Do not use. Manufacturing purpose only.
	J18	
	K14	
	L7	
	L8	
	L9	
	L10	
	L11	
	L12	
	L16	
	L17	
	L18	
	M7	
	M8	
	M11	
	M12	

Pin Name	BGA 291	Description
	M14	
	M15	
	N7	
	N8	
	N9	
	N10	
	N11	
	N12	
	N16	
	P14	
	P15	
	R16	
	R18	
	T14	
	T15	
	U16	
	V14	
	V15	
	W8	
DNU	W12	Do not use. Manufacturing purpose only.
	W13	
	W16	
	W17	
	W18	
	Y7	
	Y8	
	Y12	
	Y14	
	Y15	
	AA6	
	AA7	
	AA8	
	AA9	
	AA11	
	AA12	

Pin Name	BGA 291	Description
	AA13	
	AA16	
	AA17	
	AA18	
	AB1	
	AB2	
	AB4	
	AB8	
	AB11	
	AB13	
	AB15	
	AB17	
	AB18	
DNU	AC1	Do not use. Manufacturing purpose only.
	AC2	
	AC4	
	AC6	
	AC8	
	AC11	
	AC13	
	AC15	
	AC17	
	AC18	

*Note: For F15/H14/C13/C14/D15 balls, please refer to the design guide once "Power ID design" is adopted.

4. Product Specifications

4.1 Capacity

Capacity specifications of PV180-μSSD are available as shown in Table 4-1.

Table 4-1 Capacity Specifications

Capacity	Total bytes	Total LBA
240 GB	240,057,409,536	468,862,128
480 GB	480,103,981,056	937,703,088
960 GB	960,197,124,096	1,875,385,008

Notes:

- Display of total bytes varies from operating systems.
- 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.
- LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

4.2 Performance

Performance of PV180-μSSD is listed below in Table 4-2.

Table 4-2 Performance Specifications

Capacity	240 GB	480 GB	960 GB
Performance			
Sequential Read (MB/s)	3,220	3,745	3,725
Sequential Write (MB/s)	1,135	2,045	3,015
4K Random Read (IOPS)	116,000	229,000	392,000
4K Random Write (IOPS)	263,000	475,000	710,000

Notes:

- Measured with OS version: Win10 (64bit), version 1803 with HMB (Host Memory Buffer), performance may differ from various flash configurations or host system settings.
- Sequential performance is based on CrystalDiskMark 8.0.4 with file size 1,000MB.
- Random performance measured using IOMeter with Queue Depth 32.

4.3 Environmental Specifications

Environmental specifications of PV180-μSSD are shown in Table 4-3.

Table 4-3 Environmental Specifications

Item	Specifications
Operating temp.	-40°C to 85°C
Non-operating temp.	-40°C to 85°C
Operating humidity	20~95%
Non-operating humidity	20~95%

Note: This Environmental Specification table indicates the conditions for testing the device. Real world usages may affect the results.

4.4 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in PV180-μSSD. The prediction result for PV180-μSSD is more than 1,500,000 hours.

Note: The MTBF is predicated and calculated based on “Telcordia Technologies Special Report, SR-332, Issue 3” method.

4.5 Certification and Compliance

PV180-μSSD complies with the following standard:

- RoHS

4.6 Endurance

The endurance of a storage device is predicted by Drive Writes Per Day based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

Table 4-4 Endurance Specifications

Capacity	Drive Writes Per Day
240 GB	0.34
480 GB	0.45
960 GB	0.59

Notes:

- This estimation complies with JEDEC random client workload.
- Flash vendor guaranteed 3D NAND TLC P/E cycle: 3K
- WAF may vary from capacity, flash configurations and writing behavior on each platform.
- 1 Terabyte = 1,024GB
- DWPD (Drive Writes Per Day) is calculated based on the number of times that user overwrites the entire capacity of an SSD per day of its lifetime during the warranty period. (3D NAND TLC warranty: 3 years)

5. Flash Management

5.1 Error Correction/Detection

PV180- μ SSD implements a hardware ECC scheme, based on the Low Density Parity Check (LDPC). LDPC is a class of linear block error correcting code which has apparent coding gain over BCH code because LDPC code includes both hard decoding and soft decoding algorithms. With the error rate decreasing, LDPC can extend SSD endurance and increase data reliability while reading raw data inside a flash chip.

5.2 Bad Block Management

Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, page mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

5.3 Global Wear Leveling

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Global wear leveling is an important mechanism that levels out the wearing of all blocks so that the wearing-down of all blocks can be almost evenly distributed. This will increase the lifespan of SSDs.

5.4 Flash Translation Layer – Page Mapping

Page mapping is an advanced flash management technology whose essence lies in the ability to gather data, distribute the data into flash pages automatically, and then schedule the data to be evenly written. Page-level mapping uses one page as the unit of mapping. The most important characteristic is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different sizes of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. Thus, page mapping is adopted to increase random access speed and improve SSD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

5.5 Hyper Cache Technology

Apacer proprietary Hyper Cache technology uses a portion of the available capacity as SLC (1bit-per-cell) NAND flash memory, called Hyper cache mode. When data is written to SSD, the firmware will direct the data to Hyper Cache mode, providing excellent performance to handle various scenarios in industrial use.

5.6 Power Failure Management

Power Failure Management plays a crucial role when power supply becomes unstable. Power disruption may occur when users are storing data into the SSD, leading to instability in the drive. However, with Power Failure Management, a firmware protection mechanism will be activated to scan pages and blocks once power is resumed. Valid data will be transferred to new blocks for merging and the mapping table will be rebuilt. Therefore, data reliability can be reinforced, preventing damage to data stored in the NAND Flash.

5.7 TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks all the time.

5.8 Over-provisioning

Over-provisioning (OP) is a certain portion of the SSD capacity exclusively for increasing Garbage Collection (GC) efficiency, especially when the SSD is filled to full capacity or performs a heavy mixed-random workload. OP has the advantages of providing extended life expectancy, reliable data integrity, and high sustained write performance.

5.9 DataRAID™

Apacer's DataRAID algorithm applies an additional level of protection and error-checking. Using this algorithm, a certain amount of space is given over to aggregating and resaving the existing parity data used for error checking. So, in the event that data becomes corrupted, the parity data can be compared to the existing uncorrupted data and the content of the corrupted data can be rebuilt.

5.10 NVMe Secure Erase

NVMe Secure Erase is an NVMe drive sanitize command currently embedded in most of the storage drives. Defined in NVMe specifications, NVMe Secure Erase is part of Format NVM command that allows storage drives to erase all user data areas. The erase process usually runs on the firmware level as most of the NVMe-based storage media currently in the market are built-in with this command. NVMe Secure Erase can securely wipe out the user data in the drive and protects it from malicious attack.

6. Security and Reliability Features

6.1 Advanced Encryption Standard

Advanced Encryption Standard (AES) is a specification for the encryption of electronic data. AES has been adopted by the U.S. government since 2001 to protect classified information and is now widely implemented in embedded computing applications. The AES algorithm used in software and hardware is symmetric so that encrypting/decrypting requires the same encryption key. Without the key, the encrypted data is inaccessible to ensure information security.

Notably in flash memory applications, AES 256-bit hardware encryption is the mainstream to protect sensitive or confidential data. The hardware encryption provides better performance, reliability, and security than software encryption. It uses a dedicated processor, which is built inside the controller, to process the encryption and decryption. This enormously shortens the processing time and makes it efficient.

6.2 Write Protect (optional)

Apacer implements the Virtual Write scheme that allows write commands to go through the flash controller and data temporarily stored, but no data has been actually written into the flash. Once the system is reset and rebooted, the temporarily stored data will be lost and nowhere to be found in the system. Since the Virtual Write scheme runs at device level, it requires no software or driver installation and is independent from the host OS.

6.3 Thermal Sensor

Apacer Thermal Sensor is a digital temperature sensor with serial interface. By using designated pins for transmission, storage device owners are able to read temperature data.

6.4 Thermal Throttling

Thermal throttling can monitor the temperature of the SSD equipped with a built-in thermal sensor. This method can ensure the temperature of the device stays within temperature limits by drive throttling, i.e. reducing the speed of the drive when the device temperature reaches the threshold level, so as to prevent overheating, guarantee data reliability, and prolong product lifespan. When the temperature exceeds the maximum threshold level, thermal throttling will be triggered to reduce performance step by step to prevent hardware components from being damaged. Performance is only permitted to drop to the extent necessary for recovering a stable temperature to cool down the device's temperature. Once the temperature decreases to the minimum threshold value, transfer speeds will rise back to its optimum performance level.

6.5 End-to-End Data Protection

End-to-End Data Protection is a feature implemented in Apacer SSD products that extends error control to cover the entire path from the host computer to the drive and back, and that ensures data integrity at multiple points in the path to enable reliable delivery of data transfers. Unlike ECC which does not exhibit the ability to determine the occurrence of errors throughout the process of data transmission, End-to-End Data Protection allows SSD controller to identify an error created anywhere in the path and report the error to the host computer before it is written to the drive. This error-checking and error-reporting mechanism therefore guarantees the trustworthiness and reliability of the SSD.

7. Software Interface

7.1 Command Set

Table 7-1 summarizes the commands supported by PV180-μSSD.

Table 7-1 Admin Commands

Opcode	Command Description
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Features
0Ah	Get Features
0Ch	Asynchronous Event Request
10h	Firmware Activate
11h	Firmware Image Download
14h	Device Self-test

Table 7-2 Admin Commands – NVM Command Set Specific

Opcode	Command Description
80h	Format NVM
81h	Security Send
82h	Security Receive
84h	Sanitize

Table 7-3 NVM Commands

Opcode	Command Description
00h	Flush
01h	Write
02h	Read
04h	Write Uncorrectable
05h	Compare
08h	Write Zeroes
09h	Dataset Management

7.2 S.M.A.R.T.

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

Table 7-4 SMART (02h)

Byte	Length	Description
0	1	Critical Warning
1-2	2	Composite Temperature (NAND Flash Temperature)
3	1	Available Spare
4	1	Available Spare Threshold
5	1	Percentage Used (Average Erase Count / P/E Cycle Count)
6-31	26	Reserved
32-47	16	Data Units Read
48-63	16	Data Units Written
64-79	16	Host Read Commands
80-95	16	Host Write Commands
96-111	16	Controller Busy Time
112-127	16	Power Cycles
128-143	16	Power On Hours
144-159	16	Unsafe Shutdowns
160-175	16	Media and Data Integrity Errors
176-191	16	Number of Error Information Log Entries
192-195	4	Warning Composite Temperature Time
196-199	4	Critical Composite Temperature Time
200-201	2	Temperature Sensor 1: Composite NAND Flash Temperature
202-203	2	Temperature Sensor 2: Controller Temperature
204-205	2	Temperature Sensor 3
206-207	2	Temperature Sensor 4
208-209	2	Temperature Sensor 5
210-211	2	Temperature Sensor 6
212-213	2	Temperature Sensor 7
214-215	2	Temperature Sensor 8: Flash Temperature
216-511	296	Reserved

Note: Temperature display of the Temperature Sensor from 1 to 8 (corresponding bytes from 200 to 215) is not supported if the return value is 0h.

8. Electrical Specifications

8.1 Supply Voltage

Table 8-1 lists the supply voltage for PV180- μ SSD.

Table 8-1 Supply Range

Parameter	Rating			
	Specification	Min.	Nom.	Max.
Operating Voltage	Flash Core	+2.45V +3.135V	+2.5V +3.3V	+2.625V +3.465V
	Flash IO Supply	+1.16V	+1.2V	+1.26V
	Controller Core	+0.80V	+0.85V	+0.88V

8.2 Power Consumption

Table 8-2 lists the power consumption for PV180- μ SSD.

Table 8-2 Power Consumption

Mode	Capacity	Unit	240 GB	480 GB	960 GB
Active (Max.)		mA	1,035	1,225	1,255
Idle			230	240	235

Notes:

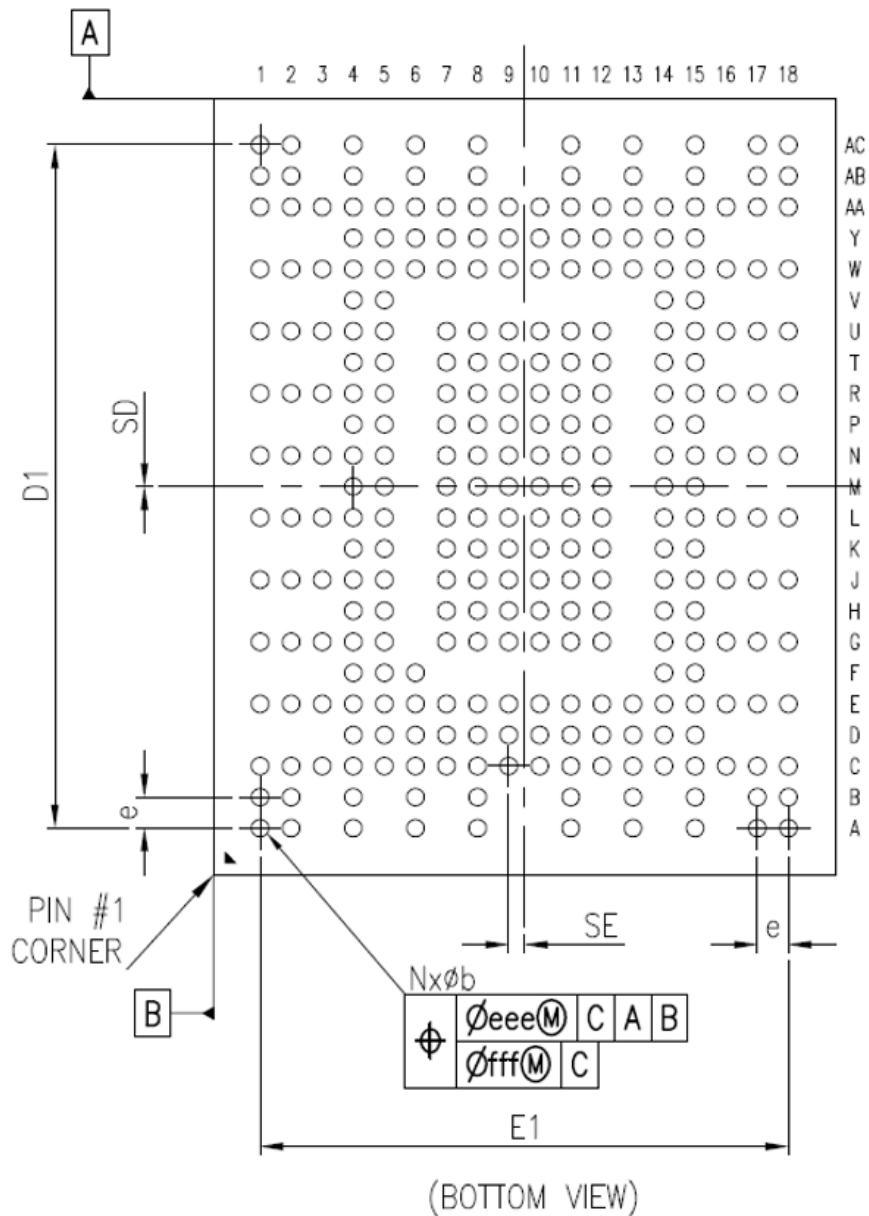
- Power consumption is measured using CrystalDiskMark 8.0.4 with file size 1,000MB.
- All values represent the total voltage measured based on an evaluation board.

9. Mechanical Specifications

Package: 16mm (x-axis) x 20mm (y-axis) / 0.8mm (Ball Pitch)

Table 9-1 Physical Dimensions

Parameter	Unit	240GB	480GB	960GB
Length	mm	20		
Width		16		
Height		1.15	1.35	1.65



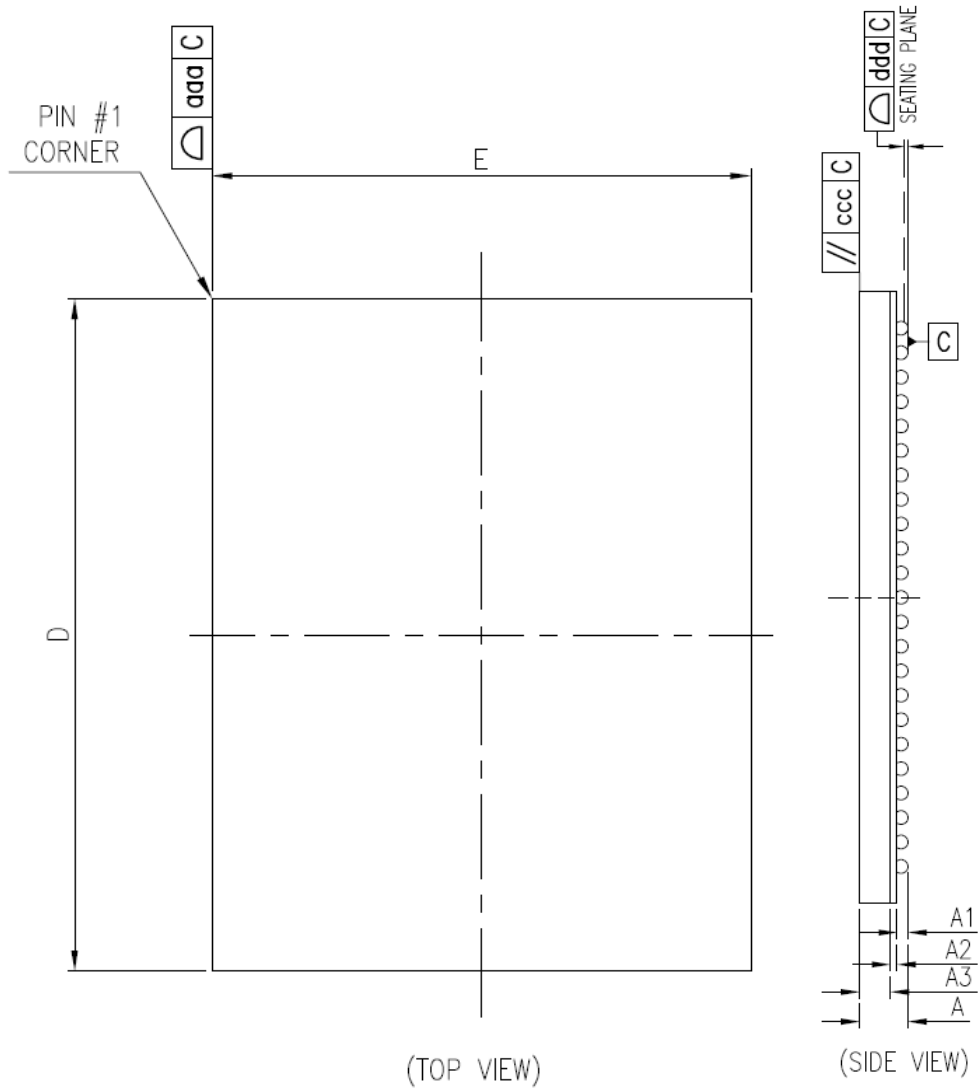


Figure 9-1 Physical Dimensions

Table 9-2 Package Specification (240GB)

	SYMBOL	DIMENSION IN MM		
		MIN.	NOM.	MAX.
TOTAL THICKNESS	A	0.95	1.07	1.15
STAND OFF	A1	0.30	0.35	0.40
SUBSTRATE THICKNESS	A2	0.22		
MOLD THICKNESS	A3	0.50		
BODY SIZE	D	20		
	E	16		
BALL DIAMETER		0.45		
BALL OPENING		0.40		
BALL WIDTH	b	0.40	0.45	0.50
BALL PITCH	e	0.80		
BALL COUNT	N	291		
EDGE BALL CENTER TO CENTER	D1	17.60 BSC.		
	E1	13.60 BSC.		
BODY CENTER TO CONTACT BALL	SD	0.00 BSC.		
	SE	0.40 BSC.		
JEDEC(REF)		MO-216(REF.)		
PACKAGE EDGE TOLERANCE	aaa	0.15		
MOLD FLATNESS	ccc	0.20		
COPLANARITY	ddd	0.20		
BALL OFFSET(PACKAGE)	eee	0.15		
BALL OFFSET(BALL)	fff	0.08		

Table 9-3 Package Specification (480GB)

	SYMBOL	DIMENSION IN MM		
		MIN.	NOM.	MAX.
TOTAL THICKNESS	A	1.15	1.27	1.35
STAND OFF	A1	0.30	0.35	0.40
SUBSTRATE THICKNESS	A2	0.22		
MOLD THICKNESS	A3	0.70		
BODY SIZE	D	20		
	E	16		
BALL DIAMETER		0.45		
BALL OPENING		0.40		
BALL WIDTH	b	0.40	0.45	0.50
BALL PITCH	e	0.80		
BALL COUNT	N	291		
EDGE BALL CENTER TO CENTER	D1	17.60 BSC.		
	E1	13.60 BSC.		
BODY CENTER TO CONTACT BALL	SD	0.00 BSC.		
	SE	0.40 BSC.		
JEDEC(REF)		MO-216(REF.)		
PACKAGE EDGE TOLERANCE	aaa	0.15		
MOLD FLATNESS	ccc	0.20		
COPLANARITY	ddd	0.20		
BALL OFFSET(PACKAGE)	eee	0.15		
BALL OFFSET(BALL)	fff	0.08		

Table 9-4 Package Specification (960GB)

	SYMBOL	DIMENSION IN MM		
		MIN.	NOM.	MAX.
TOTAL THICKNESS	A	1.45	1.57	1.65
STAND OFF	A1	0.30	0.35	0.40
SUBSTRATE THICKNESS	A2	0.22		
MOLD THICKNESS	A3	1.00		
BODY SIZE	D	20		
	E	16		
BALL DIAMETER		0.45		
BALL OPENING		0.40		
BALL WIDTH	b	0.40	0.45	0.50
BALL PITCH	e	0.80		
BALL COUNT	N	291		
EDGE BALL CENTER TO CENTER	D1	17.60 BSC.		
	E1	13.60 BSC.		
BODY CENTER TO CONTACT BALL	SD	0.00 BSC.		
	SE	0.40 BSC.		
JEDEC(REF)		MO-216(REF.)		
PACKAGE EDGE TOLERANCE	aaa	0.15		
MOLD FLATNESS	ccc	0.20		
COPLANARITY	ddd	0.20		
BALL OFFSET(PACKAGE)	eee	0.15		
BALL OFFSET(BALL)	fff	0.08		

10. Product Ordering Information

10.1 Product Code Designations

Apacer's PV180-μSSD is available in different configurations and densities. See the chart below for a comprehensive list of options for the PV180-μSSD series devices.

Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	B	H	6	.	1	8	5	X	H	A	.	X	X	X	X	X

Code 1-3 (Product Line & Form Factor)	PV180-μSSD
Code 5-6 (Model/Solution)	PV180
Code 7-8 (Product Capacity)	5J: 240GB 5K: 480GB 5L: 960GB
Code 9 (Flash Type & Product Temp)	3D TLC Wide Temperature
Code 10 (Product Spec)	PCIe BGA SSD
Code 12-14 (Version Number)	Random numbers generated by system
Code 15-16 (Firmware Version)	02: Thermal Throttling OP 05: Thermal Throttling Write Protect OP

10.2 Valid Combinations

The following tables list the available models of the PV180- μ SSD series which are in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

10.2.1 With Thermal Throttling + OP

Capacity	Valid Combination	Top Side Marking
240GB	BH6.185JHA.00102	PHD240BE44D
480GB	BH6.185KHA.00102	PHD480BE48D
960GB	BH6.185LHA.00102	PHD960BE4HD

10.2.2 With Thermal Throttling + Write Protect + OP

Capacity	Valid Combination	Top Side Marking
240GB	BH6.185JHA.00205	PHD240BE44D
480GB	BH6.185KHA.00205	PHD480BE48D
960GB	BH6.185LHA.00205	PHD960BE4HD

Revision History

Revision	Description	Date
0.1	Preliminary release	4/7/2023
1.0	Updated endurance rating on Specifications Overview page and Table 4-4	4/18/2023
1.1	- Modified Supply Voltage on Specifications Overview page - Updated Table 9-1 by adding 3.3V to operating voltage	5/2/2023
1.2	- Added Write Protect to the Security section on Specifications Overview page - Added GPIO6_WP (DNU) pin to Table 3-1 - Added 7.2 Write Protect - Updated 11. Product Ordering Information by adding write protect support	5/5/2023
1.3	Added +3.3V to the Power Supply Signals of Table 3-1 and a note to F15/H14/C13/C14/D15 balls	5/19/2023
1.4	- Updated pin type of GPIO6_WP (DNU) PIN to I at Table 3-1 - Updated pin name of BGA W7 to LED_1# at Table 3-1 - Removed rise/fall time and min. off time from Table 9-1	6/6/2023
1.5	Updated pin name of balls D7, D8, H15, and K15 at Table 3-1	8/23/2023
1.6	Updated top side marking at 11.2 Valid Combinations	9/8/2023
1.7	Removed AB6 ball from BGA 291 for pin name DNU	9/11/2023
1.8	Removed HMB support	10/3/2023
1.9	Removed APST and ASPM L1.2 support	11/29/2023

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