Apacer

RoHS Compliant

PCI Express BGA Solid State Drive

Industrial PH150-µSSD BiCS5 Product Specifications

May 21, 2024

Version 1.3

Apacer Technology Inc.
1F, No.32, Zhongcheng Rd., Tucheng Dist., New Taipei City, Taiwan, R.O.C
Tel: +886-2-2267-8000 Fax: +886-2-2267-2261
www.apacer.com

Specifications Overview:

- **PCIe Interface**
  - Compliant with PCI Express 3.1
  - Compliant with NVMe 1.3
  - Compatible with PCIe Gen3 x4 interface
- **Capacity**
  - 40, 80, 160 GB
- **Performance**[1]
  - Interface burst read/write: 2 GB/sec
  - Sequential read: up to 2,260 MB/sec
  - Sequential write: up to 1,530 MB/sec
  - Random read (4K): up to 186,000 IOPS
  - Random write (4K): up to 343,000 IOPS
- **Flash Management**
  - Low-Density Parity-Check (LDPC) Code
  - Global Wear Leveling
  - Flash bad-block management
  - Flash Translation Layer: Page Mapping
  - Power Failure Management
  - S.M.A.R.T.
  - TRIM
  - Hyper Cache Technology
  - SLC-liteX
  - DataRAID™
  - NVMe Secure Erase
- **NVMe Features**[2]
  - Supports HMB (Host Memory Buffer)
- **NAND Flash Type:** 3D TLC (BiCS5)
- **MTBF:** >2,000,000 hours
- **Endurance (in drive writes per day: DWPD)**
  - 40 GB: 14.37 DWPD
  - 80 GB: 46.02 DWPD
  - 160 GB: 13.81 DWPD
- **Temperature Range**
  - Operating (Tc): -40°C to 85°C
  - Storage (Ta): -40°C to 85°C
- **Supply Voltage**
  - 3.3V ± 5% or 2.5V ± 5%
  - 1.2V ± 5%
  - 0.9V ± 5%
- **Power Consumption**[1]
  - Active mode (Max.): 795 mA
  - Idle mode: 260 mA
- **Security**
  - AES 256-bit hardware encryption
  - Write Protect (optional)
- **Reliability**
  - Thermal Sensor
  - Thermal Throttling
  - End-to-End Data Protection
- **Physical Characteristics**
  - Form factor: PCIe BGA SSD (M.2 1620-S1)
  - Dimensions: 16.00 x 20.00 x 1.15, unit: mm
  - 291 balls
- **RoHS Compliant**

Notes:
1. Varies from capacities. The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings.
2. Windows 10 (version 1703) onwards supports the HMB (Host Memory Buffer) function.

© 2024 Apacer Technology Inc.

Table of Contents

1. General Description 4

2. Functional Block 4

3. Pin Assignments 5

4. Product Specifications 15

4.1 Capacity 15
4.2 Performance 15
4.3 Environmental Specifications 16
4.4 Mean Time Between Failures (MTBF) 16
4.5 Certification and Compliance 16
4.6 Endurance 16

5. Flash Management 17

5.1 Error Correction/Detection 17
5.2 Bad Block Management 17
5.3 Global Wear Leveling 17
5.4 Flash Translation Layer – Page Mapping 17
5.5 Power Failure Management 18
5.6 Hyper Cache Technology 18
5.7 SLC-liteX 18
5.8 DataRAID™ 18
5.9 NVMe Secure Erase 18

6. NVMe Support Features 19

6.1 Host Memory Buffer 19

7. Security and Reliability Features 20

7.1 Advanced Encryption Standard 20
7.2 Write Protect (optional) 20
7.3 Thermal Sensor 20
7.4 Thermal Throttling 20
7.5 End-to-End Data Protection 21

8. Software Interface 22

8.1 Command Set 22

© 2024 Apacer Technology Inc.

8.2 S.M.A.R.T. 23

9. Electrical Specifications 25

9.1 Supply Voltage 25

9.2 Power Consumption 25

10. Mechanical Specifications 26

11. Product Ordering Information 28

11.1 Product Code Designations 28

11.2 Valid Combinations 29

© 2024 Apacer Technology Inc.

1. General Description

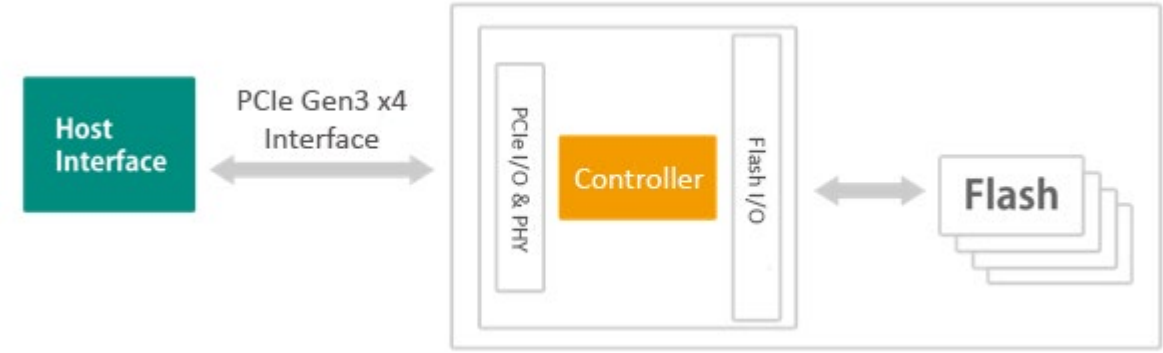
Apacer PCIe BGA SSD PH150-µSSD (M.2 1620) presents a revolutionary breakthrough of NAND flash storage technology. This micro sized SSD delivers all the technological benefits in NAND based storage solution with ultra speed PCIe Gen3 x4 interface in an embedded BGA form factor, compatible with JEDEC PCIe M.2 1620. Formed in a size of an IC chip, the performance level can reach up to 2,260 MB/s for read and 1,530 MB/s for write.

PH150-µSSD is equipped with a powerful PCIe controller that supports on-the-module ECC, along with an efficient wear-leveling scheme. Additionally, it incorporates LDPC (Low Density Parity Check) ECC engine and Apacer's SLC-liteX technology, supporting P/E cycles of up to 30,000 times to extend SSD endurance and enhance data reliability. Furthermore, PH150-µSSD features a built-in thermal sensor to monitor the SSD temperature via S.M.A.R.T commands. It is configured with thermal throttling to dynamically adjust frequency scaling, ensuring sustained performance while preventing overheating. For highly-intensive applications, End-to-End Data Protection ensures data integrity at multiple points in the path, enabling reliable delivery of data transfers.

Security-wise, Advanced Encryption Standard (AES) and Write Protect ensure data security and provide users with peace of mind knowing their data is safeguarded against unauthorized use at all times. PH150-µSSD also adopts the latest page mapping file translation layer and comes with various implementations including flash block management, power failure management, Hyper Cache technology, DataRAID, and NVMe secure erase.

Apacer PH150-µSSD boasts micro size, high-speed performance, low power consumption, shock resistance, high stability and reliability. PH150-µSSD is the ideal choice for high-end industrial and 5G high-speed applications, including industrial IoT, cloud computing, servers and networking, defense, gaming, and high-performance computing.

2. Functional Block



Note: The actual number of NAND flash used on Apacer PH150-µSSD varies from capacities. The illustration is for reference only.

Figure 2-1 Functional Block Diagram

© 2024 Apacer Technology Inc.

3. Pin Assignments

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU	A
B	DNU	DNU		DNU		NC		DNU			DNU		DNU		DNU		DNU	DNU	B
C	GND	GND	GND	GND	GND	DNU	NC	NC	DNU	FLASH_RZQ	DNU	DNU	PWR_ID4	PWR_ID3	GND	DNU	DNU	DNU	C
D				REFCLKP	REFCLKN	GND	PERST#	CLKREQ#	PWR_1	PWR_1	GND	DNU	DIAG1	NC	PWR_ID0				D
E	GND	GND	GND	GND	GND	GND	GND	NC	PWR_1	PWR_1	GND	NC	DIAG0	GND	GND	DNU	DNU	DNU	E
F				PERP0	PERN0	GND								NC	PWR_ID1				F
G	GND	GND	GND	GND	GND		PWR_3	PWR_3	GND	GND	PWR_3	PWR_3		GND	GND	DNU	DNU	DNU	G
H				PETP0	PETN0		PWR_3	PWR_3	GND	GND	PWR_3	PWR_3		PWR_ID2	PLN				H
J	GND	GND	GND	GND	GND		PWR_3	PWR_3	GND	GND	PWR_3	PWR_3		GND	GND	DNU	DNU	DNU	J
K				PERP1	PERN1		GND	GND	GND	GND	GND	GND		RFU	PLA				K
L	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	DNU	NC	L
M				PETP1	PETN1		RFU	RFU	GND	GND	RFU	RFU		RFU	RFU				M
N	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	JTAG_TCK	JTAG_TMS	N
P				PERP2	PERN2		GND	GND	GND	GND	GND	GND		RFU	RFU				P
R	GND	GND	GND	GND	GND		PWR_2	PWR_2	GND	GND	PWR_2	PWR_2		GND	GND	DNU	XGPIO0	NC	R
T				PETP2	PETN2		PWR_2	PWR_2	GND	GND	PWR_2	PWR_2		RFU	RFU				T
U	GND	GND	GND	GND	GND		PWR_2	PWR_2	GND	GND	PWR_2	PWR_2		GND	GND	DNU	SMB_CLK	SMB_DATA	U
V				PERP3	PERN3									RFU	RFU				V
W	GND	GND	GND	GND	GND	GND	LED	RFU	PWR_1	PWR_1	GND	RFU	RFU	GND	GND	DNU	DNU	ALERT#	W
Y				PETP3	PETN3	GND	DNU	DNU	PWR_1	PWR_1	GND	DNU	GND	DNU	DNU				Y
AA	GND	GND	GND	GND	GND	DNU	DNU	DNU	DNU	CTL_RZQ	DNU	DNU	DNU	GND	GND	DNU	DNU	DNU	AA
AB	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU	AB
AC	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU	AC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

Table 3-1 Pin Layout

Table 3-1 Pin Assignments

Pin Name	BGA 345	Pin Type	Description	IO Voltage
UART/GPIO				
XGPIO0	R17	I	Debug only	1.8V
DIAG0	E13	O	Debug only	1.8V
DIAG1	D13	I	Debug only	1.8V
SMB_CLK	U17	I/O	Debug only	1.8V
SMB_DATA	U18	I/O	Debug only	1.8V
JTAG_TCK	N17	I/O	Debug only	1.8V
JTAG_TMS	N18	I/O	Debug only	1.8V

© 2024 Apacer Technology Inc.

Pin Name	BGA 345	Pin Type	Description	IO Voltage
PCIe Interface Signals				
PERP0	F4	I/O	PCIe TX/RX Differential signals defined by the PCI Express Card Electromechanical Specification.	--
PERN0	F5			
PERP1	K4			
PERN1	K5			
PERP2	P4			
PERN2	P5			
PERP3	V4			
PERN3	V5			
PETP0	H4			
PETN0	H5			
PETP1	M4			
PETN1	M5			
PETP2	T4			
PETN2	T5			
PETP3	Y4			
PETN3	Y5			
REFCLKP	D4	I	PCIe Reference Clock signals (100 MHz) defined by the PCI Express Card Electromechanical Specification.	--
REFCLKN	D5	I		--
PERST#	D7	I	PE-Reset is a functional reset to the card as defined by the PCI Express Mini Card Electromechanical Specification.	1.8V
CLKREQ#	D8	I/O	--	1.8V
Optional Signals				
FLASH_RZQ	C10	--	Flash Calibration REF RESISTENCE	1.2V
CTL_RZQ	AA10	--	Control Calibration REF RESISTENCE	1.2V
PLA	K15	O	--	1.8V
PLN	H15	I	Power Loss Notification	1.8V
ALERT	W18			
SSD Specific Signals				
LED	W7	O	Open drain, active low signal. This signal is used to allow the Adapter to provide status indication via LED device that will be provided by the system.	3.3V

© 2024 Apacer Technology Inc.

Pin Name	BGA 345	Description
Power ID	D15	Power ID defined by PCIe spec
	F15	
	H14	
	C14	
	C13	
PWR_1	D9	+2.5V source (Option 3.3V)
	D10	
	E9	
	E10	
	W9	
	W10	
	Y9	
	Y10	
PWR_2	R7	+1.2V source
	R8	
	R11	
	R12	
	T7	
	T8	
	T11	
	T12	
	U7	
	U8	
	U11	
	U12	
PWR_3	G7	+0.9V source
	G8	
	G11	
	G12	
	H7	
	H8	
	H11	
	H12	
	J7	
	J8	

© 2024 Apacer Technology Inc.

Pin Name	BGA 345	Description
	J11	
	J12	
DNU	A1	Do Not Use
	A11	
	A13	
	A15	
	A17	
	A18	
	A2	
	A4	
	A6	
	A8	
	AA11	
	AA12	
	AA13	
	AA16	
	AA17	
	AA18	
	AA6	
	AA7	
	AA8	
	AA9	
	AB1	
	AB11	
	AB13	
	AB15	
	AB17	
	AB18	
	AB2	
	AB4	
	AB6	
	AB8	
	AC1	
	AC11	
	AC13	

© 2024 Apacer Technology Inc.

Pin Name	BGA 345	Description
	AC15	
	AC17	
	AC18	
	AC2	
	AC4	
	AC6	
	AC8	
	B1	
	B11	
	B13	
	B15	
	B17	
	B18	
	B2	
	B4	
	B8	
	C11	
	C12	
	C16	
	C17	
	C18	
	C6	
	C9	
	D12	
	E16	
	E17	
	E18	
	G16	
	G17	
	G18	
	J16	
	J17	
	J18	
	L16	
	L17	

© 2024 Apacer Technology Inc.

Pin Name	BGA 345	Description
	N16	
	R16	
	U16	
	W16	
	W17	
	Y12	
	Y14	
	Y15	
	Y7	
	Y8	
GND	AA1	Return current path
	AA14	
	AA15	
	AA2	
	AA3	
	AA4	
	AA5	
	C1	
	C15	
	C2	
	C3	
	C4	
	C5	
	D11	
	D6	
	E1	
	E11	
	E14	
	E15	
	E2	
	E3	
	E4	
	E5	
	E6	
	E7	

© 2024 Apacer Technology Inc.

Pin Name	BGA 345	Description
	F6	
	G1	
	G10	
	G14	
	G15	
	G2	
	G3	
	G4	
	G5	
	G9	
	H10	
	H9	
	J1	
	J10	
	J14	
	J15	
	J2	
	J3	
	J4	
	J5	
	J9	
	K10	
	K11	
	K12	
	K7	
	K8	
	K9	
	L1	
	L14	
	L15	
	L2	
	L3	
	L4	
	L5	
	M10	

© 2024 Apacer Technology Inc.

Pin Name	BGA 345	Description
	M9	
	N1	
	N14	
	N15	
	N2	
	N3	
	N4	
	N5	
	P10	
	P11	
	P12	
	P7	
	P8	
	P9	
	R1	
	R10	
	R14	
	R15	
	R2	
	R3	
	R4	
	R5	
	R9	
	T10	
	T9	
	U1	
	U10	
	U14	
	U15	
	U2	
	U3	
	U4	
	U5	
	U9	
	W1	

© 2024 Apacer Technology Inc.

Pin Name	BGA 345	Description
	W11	
	W14	
	W15	
	W2	
	W3	
	W4	
	W5	
	W6	
	Y11	
	Y13	
	Y6	
NC	B6	Not Connect
	C7	
	C8	
	D14	
	E12	
	E8	
	F14	
	L18	
	R18	
RFU	K14	Reserved for future use
	L10	
	L11	
	L12	
	L7	
	L8	
	L9	
	M11	
	M12	
	M14	
	M15	
	M7	
	M8	
	N10	
	N11	

© 2024 Apacer Technology Inc.

Pin Name	BGA 345	Description
	N12	
	N7	
	N8	
	N9	
	P14	
	P15	
	T14	
	T15	
	V14	
	V15	
	W12	
	W13	
	W8	

© 2024 Apacer Technology Inc.

4. Product Specifications

4.1 Capacity

Capacity specifications of PH150-µSSD are available as shown in Table 4-1.

Table 4-1 Capacity Specifications

Capacity	Total bytes	Total LBA
40 GB	40,018,529,936	78,161,328
80 GB	80,026,361,856	156,301,488
160 GB	160,041,885,696	312,581,808

Notes:
- Display of total bytes varies from operating systems.
- 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.
- LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

4.2 Performance

Performance of PH150-µSSD is listed below in Table 4-2.

Table 4-2 Performance Specifications

Capacity / Performance	40 GB	80 GB	160GB
Sequential Read (MB/s)	1,145	2,260	2,110
Sequential Write (MB/s)	560	1,105	1,530
4K Random Read (IOPS)	55,000	106,000	186,000
4K Random Write (IOPS)	124,000	247,000	343,000

Notes:
- Measured with OS version: Win10 (64bit), version 1803 with HMB (Host Memory Buffer), performance may differ from various flash configurations or host system settings.
- Sequential performance is based on CrystalDiskMark 8.0.4 with file size 1,000MB.
- Random performance measured using IOMeter with Queue Depth 32.

© 2024 Apacer Technology Inc.

4.3 Environmental Specifications

Environmental specifications of PH150-µSSD are shown in Table 4-3.

Table 4-3 Environmental Specifications

Item	Specifications
Operating temp. (Tc)	-40°C to 85°C
Non-operating temp. (Ta)	-40°C to 85°C
Operating humidity	20~95%
Non-operating humidity	20~95%

Notes:
- This Environmental Specification table indicates the conditions for testing the device. Real world usages may affect the results.
- Tc: case temperature; Ta: ambient temperature. The operating temperature is determined by the case temperature. Adequate airflow is advisable as it enables the device to maintain optimal temperatures, especially in environments with heavy workloads.

4.4 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in PH150-µSSD. The prediction result for PH150-µSSD is more than 2,000,000 hours.

Note: The MTBF is predicated and calculated based on “Telcordia Technologies Special Report, SR-332, Issue 3” method.

4.5 Certification and Compliance

PH150-µSSD complies with the following standards:

- RoHS

4.6 Endurance

The endurance of a storage device is predicted by Drive Writes Per Day based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

Table 4-4 Endurance Specifications

Capacity	Drive Writes Per Day
40 GB	14.37
800 GB	46.02
160 GB	13.81

Notes:
- This estimation complies with JEDEC random client workload.
- Flash vendor guaranteed SLC-liteX P/E cycle: 30K
- WAF may vary from capacity, flash configurations and writing behavior on each platform.
- 1 Terabyte = 1,024GB
- DWPD (Drive Writes Per Day) is calculated based on the number of times that user overwrites the entire capacity of an SSD per day of its lifetime during the warranty period. (3D SLC-liteX warranty: 5 years)

© 2024 Apacer Technology Inc.

5. Flash Management

5.1 Error Correction/Detection

PH150-µSSD implements a hardware ECC scheme, based on the Low Density Parity Check (LDPC). LDPC is a class of linear block error correcting code which has apparent coding gain over BCH code because LDPC code includes both hard decoding and soft decoding algorithms. With the error rate decreasing, LDPC can extend SSD endurance and increase data reliability while reading raw data inside a flash chip.

5.2 Bad Block Management

Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, page mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

5.3 Global Wear Leveling

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Global wear leveling is an important mechanism that levels out the wearing of all blocks so that the wearing-down of all blocks can be almost evenly distributed. This will increase the lifespan of SSDs.

5.4 Flash Translation Layer – Page Mapping

Page mapping is an advanced flash management technology whose essence lies in the ability to gather data, distribute the data into flash pages automatically, and then schedule the data to be evenly written. Page-level mapping uses one page as the unit of mapping. The most important characteristic is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different sizes of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. Thus, page mapping is adopted to increase random access speed and improve SSD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

© 2024 Apacer Technology Inc.

5.5 Power Failure Management

Power Failure Management plays a crucial role when power supply becomes unstable. Power disruption may occur when users are storing data into the SSD, leading to instability in the drive. However, with Power Failure Management, a firmware protection mechanism will be activated to scan pages and blocks once power is resumed. Valid data will be transferred to new blocks for merging and the mapping table will be rebuilt. Therefore, data reliability can be reinforced, preventing damage to data stored in the NAND Flash.

5.6 Hyper Cache Technology

Apacer proprietary Hyper Cache technology uses a portion of the available capacity as SLC (1bit-per-cell) NAND flash memory, called Hyper cache mode. When data is written to SSD, the firmware will direct the data to Hyper Cache mode, providing excellent performance to handle various scenarios in industrial use.

5.7 SLC-liteX

Apacer's SLC-liteX is based on 3D NAND technology. The firmware is carefully tweaked by our engineering team so as to offer the greatest number of P/E cycles in this format – 30,000, which is 10 times more than MLC or industrial 3D TLC. The longest lifespans are therefore available at reasonable cost.

5.8 DataRAID™

Apacer's DataRAID algorithm applies an additional level of protection and error-checking. Using this algorithm, a certain amount of space is given over to aggregating and resaving the existing parity data used for error checking. So, in the event that data becomes corrupted, the parity data can be compared to the existing uncorrupted data and the content of the corrupted data can be rebuilt.

5.9 NVMe Secure Erase

NVMe Secure Erase is an NVMe drive sanitize command currently embedded in most of the storage drives. Defined in NVMe specifications, NVMe Secure Erase is part of Format NVM command that allows storage drives to erase all user data areas. The erase process usually runs on the firmware level as most of the NVMe-based storage media currently in the market are built-in with this command. NVMe Secure Erase can securely wipe out the user data in the drive and protects it from malicious attack.

© 2024 Apacer Technology Inc.

6. NVMe Support Features

6.1 Host Memory Buffer

Host Memory Buffer (HMB) allows HOST to allocate system memory for SSD's exclusive use in order to provide better performance and endurance, especially for DRAMless solutions.

© 2024 Apacer Technology Inc.

7. Security and Reliability Features

7.1 Advanced Encryption Standard

Advanced Encryption Standard (AES) is a specification for the encryption of electronic data. AES has been adopted by the U.S. government since 2001 to protect classified information and is now widely implemented in embedded computing applications. The AES algorithm used in software and hardware is symmetric so that encrypting/decrypting requires the same encryption key. Without the key, the encrypted data is inaccessible to ensure information security.

Notably in flash memory applications, AES 256-bit hardware encryption is the mainstream to protect sensitive or confidential data. The hardware encryption provides better performance, reliability, and security than software encryption. It uses a dedicated processor, which is built inside the controller, to process the encryption and decryption. This enormously shortens the processing time and makes it efficient.

7.2 Write Protect (optional)

Apacer implements the Virtual Write scheme that allows write commands to go through the flash controller and data temporarily stored, but no data has been actually written into the flash. Once the system is reset and rebooted, the temporarily stored data will be lost and nowhere to be found in the system. Since the Virtual Write scheme runs at device level, it requires no software or driver installation and is independent from the host OS.

7.3 Thermal Sensor

Apacer Thermal Sensor is a digital temperature sensor with serial interface. By using designated pins for transmission, storage device owners are able to read temperature data.

7.4 Thermal Throttling

Thermal throttling can monitor the temperature of the SSD equipped with a built-in thermal sensor. This method can ensure the temperature of the device stays within temperature limits by drive throttling, i.e. reducing the speed of the drive when the device temperature reaches the threshold level, so as to prevent overheating, guarantee data reliability, and prolong product lifespan. When the temperature exceeds the maximum threshold level, thermal throttling will be triggered to reduce performance step by step to prevent hardware components from being damaged. Performance is only permitted to drop to the extent necessary for recovering a stable temperature to cool down the device's temperature. Once the temperature decreases to the minimum threshold value, transfer speeds will rise back to its optimum performance level.

© 2024 Apacer Technology Inc.

7.5 End-to-End Data Protection

End-to-End Data Protection is a feature implemented in Apacer SSD products that extends error control to cover the entire path from the host computer to the drive and back, and that ensures data integrity at multiple points in the path to enable reliable delivery of data transfers. Unlike ECC which does not exhibit the ability to determine the occurrence of errors throughout the process of data transmission, End-to-End Data Protection allows SSD controller to identify an error created anywhere in the path and report the error to the host computer before it is written to the drive. This error-checking and error-reporting mechanism therefore guarantees the trustworthiness and reliability of the SSD.

© 2024 Apacer Technology Inc.

8. Software Interface

8.1 Command Set

Table 8-1 summarizes the commands supported by PH150-µSSD.

Table 8-1 Admin Commands

Opcode	Command Description
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Features
0Ah	Get Features
0Ch	Asynchronous Event Request
10h	Firmware Activate
11h	Firmware Image Download
14h	Device Self-test
18h	Keep Alive

Table 8-2 Admin Commands – NVM Command Set Specific

Opcode	Command Description
80h	Format NVM

Table 8-3 NVM Commands

Opcode	Command Description
00h	Flush
01h	Write
02h	Read
04h	Write Uncorrectable
08h	Write Zeroes
09h	Dataset Management

© 2024 Apacer Technology Inc.

8.2 S.M.A.R.T.

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

Table 8-4 SMART (02h)

Byte	Length	Description
0	1	Critical Warning
1-2	2	Composite Temperature
3	1	Available Spare
4	1	Available Spare Threshold
5	1	Percentage Used
6-31	26	Reserved
32-47	16	Data Units Read
48-63	16	Data Units Written
64-79	16	Host Read Commands
80-95	16	Host Write Commands
96-111	16	Controller Busy Time
112-127	16	Power Cycles
128-143	16	Power On Hours
144-159	16	Unsafe Shutdowns
160-175	16	Media and Data Integrity Errors
176-191	16	Number of Error Information Log Entries
192-195	4	Warning Composite Temperature Time
196-199	4	Critical Composite Temperature Time
200-201	2	Temperature Sensor 1
202-203	2	Temperature Sensor 2
204-205	2	Temperature Sensor 3
206-207	2	Temperature Sensor 4
208-209	2	Temperature Sensor 5
210-211	2	Temperature Sensor 6
212-213	2	Temperature Sensor 7
214-215	2	Temperature Sensor 8
216-511	296	Reserved

Note: Temperature display of the Temperature Sensor from 1 to 8 (corresponding bytes from 200 to 215) is not supported if the return value is 0h.

© 2024 Apacer Technology Inc.

Table 8-5 SMART (C0h)

Byte	Length	Description
0-255	256	Reserved
256-257	2	SSD Protect Mode
258-261	4	Host Read UNC Count
262-265	4	PHY Error Count
266-269	4	Reserved
270-273	4	Total Early Bad Block Count
274-277	4	Total Later Bad Block Count
278-281	4	Max Erase Count
282-285	4	Average Erase count
286-289	4	Program Fail Count
290-293	4	Erase Fail Count
294-301	8	Flash Write Sector
302-305	4	Total Spare Block
306-309	4	Current Spare Block
310-313	4	Read Retry Count
314-511	210	Reserved

© 2024 Apacer Technology Inc.

9. Electrical Specifications

9.1 Supply Voltage

Table 9-1 lists the supply voltage for PH150-µSSD.

Table 9-1 Supply Range

Parameter	Rating			
Operating Voltage	Specification	Min.	Nom.	Max.
	Flash Core	+2.45V +3.135V	+2.5V +3.3V	+2.625V +3.465V
	Flash IO Supply	+1.18V	+1.2V	+1.26V
	Controller Core	+0.89V	+0.9V	+0.945V

9.2 Power Consumption

Table 9-2 lists the power consumption for PH150-µSSD.

Table 9-2 Power Consumption

Capacity / Mode	Unit	40 GB	80 GB	160 GB
Active (Max.)	mA	520	795	785
Idle		250	255	260

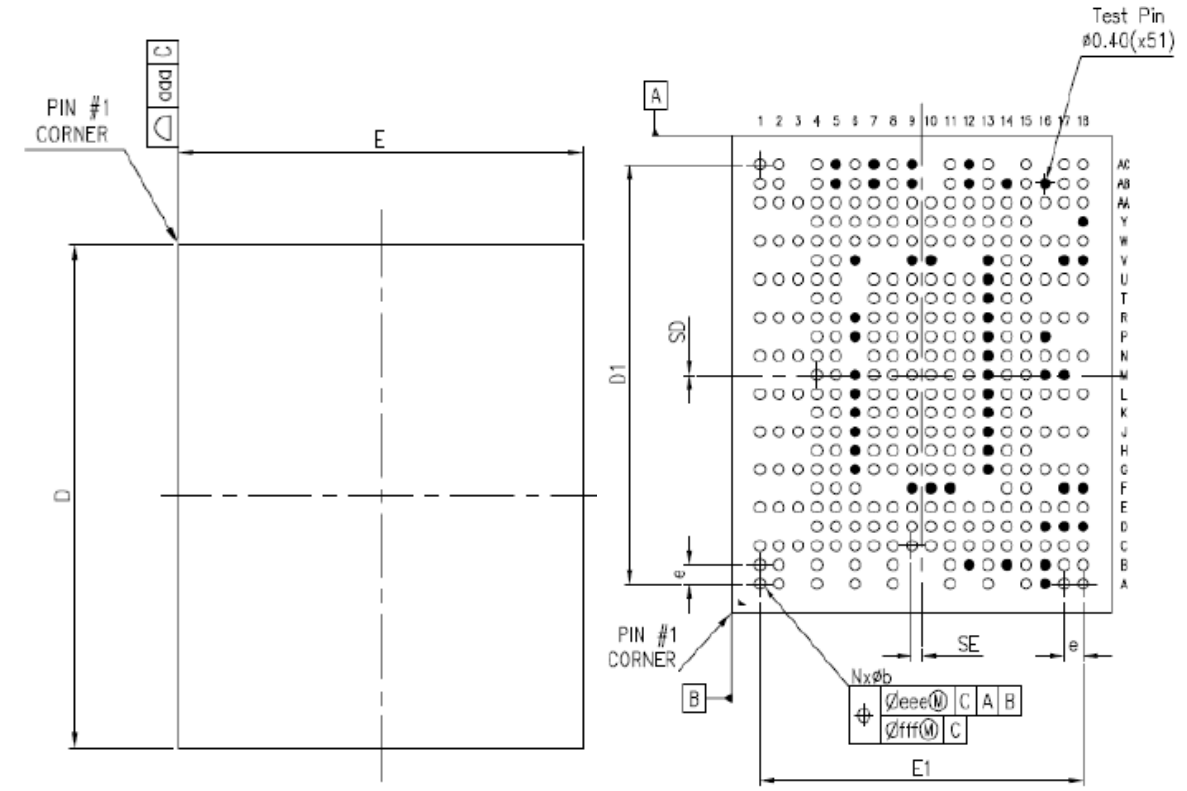
Notes:
- All values are typical and may vary depending on flash configurations or host system settings.
- Power consumption is measured using CrystalDiskMark 8.0.4 with file size 1,000MB.
- All values represent the total voltage measured based on an evaluation board.

© 2024 Apacer Technology Inc.

10. Mechanical Specifications

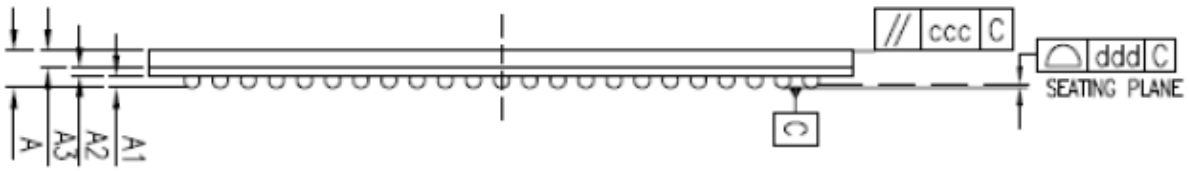
Table 10-1 Physical Dimensions

Parameter	Unit	40 GB	80 GB	160 GB
Length	mm	20.00		
Width		16.00		
Height (Max.)		1.15		



Top View

Bottom View



Side View

Figure 10-1 Physical Dimensions

© 2024 Apacer Technology Inc.

Table 10-2 Package Specification

	SYMBOL	DIMENSION IN MM		
		MIN.	NOM.	MAX.
TOTAL THICKNESS	A	0.95	1.07	1.15
STAND OFF	A1	0.30	0.35	0.40
SUBSTRATE THICKNESS	A2		0.22	
MOLD THICKNESS	A3		0.50	
BODY SIZE	D		20	
	E		16	
BALL DIAMETER			0.45	
BALL OPENING			0.40	
BALL WIDTH	b	0.40	0.45	0.50
BALL PITCH	e		0.80	
BALL COUNT	N		291	
EDGE BALL CENTER TO CENTER	D1		17.60 BSC.	
	E1		13.60 BSC.	
BODY CENTER TO CONTACT BALL	SD		0.00 BSC.	
	SE		0.40 BSC.	
JEDEC(REF)			MO-216(REF.)	
PACKAGE EDGE TOLERANCE	aaa		0.15	
MOLD FLATNESS	ccc		0.20	
COPLANARITY	ddd		0.20	
BALL OFFSET(PACKAGE)	eee		0.15	
BALL OFFSET(BALL)	fff		0.08	

© 2024 Apacer Technology Inc.

11. Product Ordering Information

11.1 Product Code Designations

Apacer's PH150-µSSD is available in different configurations and densities. See the chart below for a comprehensive list of options for the PH150-µSSD series devices.

Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	B	H	6	.	C	B	9	X	T	A	.	X	X	X	X	X

Code 1-3 (Product Line & Form Factor)	PH150-µSSD
Code 5-6 (Model/Solution)	PH150
Code 7-8 (Product Capacity)	9H: 40GB 9J: 80GB 9K: 160GB
Code 9 (Flash Type & Product Temp)	3D SLC-liteX Wide Temperature
Code 10 (Product Spec)	PCIe BGA SSD
Code 12-14 (Version Number)	Random numbers generated by system
Code 15-16 (Firmware Version)	05: Thermal Throttling SLC-liteX 09: Thermal Throttling SLC-liteX WP

© 2024 Apacer Technology Inc.

11.2 Valid Combinations

The following table lists the available models of the PH150-µSSD series which are in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

11.2.1 Without Write Protect

Capacity	Valid Combination	Top Side Marking
40GB	BH6.CB9HTA.00105	PHB-40GBE22E
80GB	BH6.CB9JTA.00105	PHB-80GBE44E
160GB	BH6.CB9KTA.00105	PHB-160BE48E

11.2.2 With Write Protect (optional)

Capacity	Valid Combination	Top Side Marking
40GB	BH6.CB9HTA.00209	PHB-40GBE22E
80GB	BH6.CB9JTA.00209	PHB-80GBE44E
160GB	BH6.CB9KTA.00209	PHB-160BE48E

© 2024 Apacer Technology Inc.

Revision History

Revision	Description	Date
1.0	Initial release	9/26/2023
1.1	Removed APST and ASPM L1.2 support	11/29/2023
1.2	Added a note regarding temperature at Table 4-3	3/29/2024
1.3	Added top side marking to 11.2 Valid Combinations	5/21/2024

© 2024 Apacer Technology Inc.

Global Presence

Taiwan (Headquarters)
Apacer Technology Inc.
1F., No.32, Zhongcheng Rd., Tucheng Dist.,
New Taipei City 236, Taiwan R.O.C.
Tel: 886-2-2267-8000
Fax: 886-2-2267-2261
amtsales@apacer.com

U.S.A.
Apacer Memory America, Inc.
46732 Lakeview Blvd., Fremont, CA 94538
Tel: 1-408-518-8699
Fax: 1-510-249-9551
sa@apacerus.com

Japan
Apacer Technology Corp.
6F, Daiyontamachi Bldg., 2-17-12, Shibaura, Minato-Ku,
Tokyo, 108-0023, Japan
Tel: 81-3-5419-2668
Fax: 81-3-5419-0018
jpservices@apacer.com

Europe
Apacer Technology B.V.
Science Park Eindhoven 5051 5692 EB Son,
The Netherlands
Tel: 31-40-267-0000
Fax: 31-40-290-0686
sales@apacer.nl

China
Apacer Electronic (Shanghai) Co., Ltd
Room D, 22/FL, No.2, Lane 600, JieyunPlaza,
Tianshan RD, Shanghai, 200051, China
Tel: 86-21-6228-9939
Fax: 86-21-6228-9936
sales@apacer.com.cn

India
Apacer Technologies Pvt Ltd,
1874, South End C Cross, 9th Block Jayanagar,
Bangalore-560069, India
Tel: 91-80-4152-9061/62
Fax: 91-80-4170-0215
sales_india@apacer.com

© 2024 Apacer Technology Inc.