Apacer

RoHS Compliant

PCI Express BGA Solid State Drive

PV920-µSSD Product Specifications

May 23, 2022

Version 1.3

Apacer Technology Inc.
1F, No.32, Zhongcheng Rd., Tucheng Dist., New Taipei City, Taiwan, R.O.C
Tel: +886-2-2267-8000 Fax: +886-2-2267-2261
www.apacer.com

Apacer

Specifications Overview:

- **PCIe Interface**
  - Compliant with NVMe 1.4
  - Compatible with PCIe Gen3 x4 interface
- **Capacity**
  - 120, 240, 480, 960 GB
- **Performance**[1]
  - Interface burst read/write: 2 GB/sec
  - Sequential read: up to 3,220 MB/sec
  - Sequential write: up to 2,705 MB/sec
  - Random read (4K): up to 311,000 IOPS
  - Random write (4K): up to 277,000 IOPS
- **Flash Management**
  - Low-Density Parity-Check (LDPC) Code
  - Global Wear Leveling
  - Flash bad-block management
  - Flash Translation Layer: Page Mapping
  - Power Failure Management
  - S.M.A.R.T.
  - TRIM
  - Hyper Cache Technology
  - Over-Provisioning
  - SMART Read Refresh™
  - NVMe Secure Erase
  - Write Protect
- **NAND Flash Type:** 3D TLC (B27)
- **MTBF:** >3,000,000 hours
- **Endurance (in drive writes per day: DWPD)**
  - 120 GB: 1.23 DWPD
  - 240 GB: 1.25 DWPD
  - 480 GB: 1.25 DWPD
  - 960 GB: 1.22 DWPD
- **Temperature Range**
  - Operating:
    Standard: 0°C to 70°C
    Wide: -40°C to 85°C
  - Storage: -40°C to 85°C
- **Supply Voltage**
  - 3.3 V ± 5%
  - 1.8 V ± 5%
  - 1.2 V ± 5%
- **Power Consumption**[1]
  - Active mode: 1,260 mA
  - Idle mode: 320 mA
- **Form Factor**
  - PCIe BGA SSD (M.2 1620)
  - Dimensions: 16.00 x 20.00 x 1.78[2], unit: mm
  - 291 balls
- **Security**
  - AES 256-bit hardware encryption
- **Reliability**
  - Thermal Sensor
  - Thermal Throttling
  - End-to-End Data Protection
- **Power Management**
  - Supports APST
  - Supports ASPM L1.2
- **NVMe Features**[3]
  - Supports HMB (Host Memory Buffer)
- **RoHS Compliant**

Notes:
1. Varies from capacities. The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings.
2. Height/Thickness: 1.78mm (960GB) / 1.28mm (120-480GB)
3. Windows 10 (version 1703) onwards supports the HMB (Host Memory Buffer) function.

Table of Contents

1. General Description

Apacer PCIe BGA SSD PV920-µSSD (M.2 1620) presents a revolutionary breakthrough of NAND flash storage technology. This micro sized SSD delivers all the technological benefits in NAND based storage solution with ultra speed PCIe Gen3 x4 interface in an embedded BGA form factor, compatible with JEDEC PCIe M.2 1620. Formed in a size of an IC chip, the performance level can reach up to 3,220 MB/s for read and 2,705 MB/s for write.

Regarding reliability, PV920-µSSD is built with a powerful PCIe controller that supports on-the-module ECC as well as efficient wear leveling scheme, and implemented with LDPC (Low Density Parity Check) ECC engine to extend SSD endurance and increase data reliability. Furthermore, PV920-µSSD is equipped with a built-in thermal sensor to monitor the temperature of the SSD via S.M.A.R.T commands and configured with thermal throttling to dynamically adjust frequency scaling to enhance data reliability and provide sustained performance while overheating. For highly-intensive applications, End-to-End Data Protection ensures that data integrity can be assured at multiple points in the path to enable reliable delivery of data transfers.

Security-wise, Advanced Encryption Standard (AES) ensures data security and provides users with a peace of mind knowing their data is safeguarded at all times. PV920-µSSD also adopts the latest page mapping file translation layer and comes with various implementations including power saving modes, flash block management, S.M.A.R.T., TRIM, Write Protect and SMART Read Refresh™.

Apacer PV920-µSSD boasts micro size, high-speed performance, low power consumption, shock resistance, high stability and reliability. PV920-µSSD will be adopted by many high-end industrial and 5G high-speed applications, including the Industrial IoT, cloud computing, servers and networking, defense, gaming, and high-performance computing

2. Functional Block

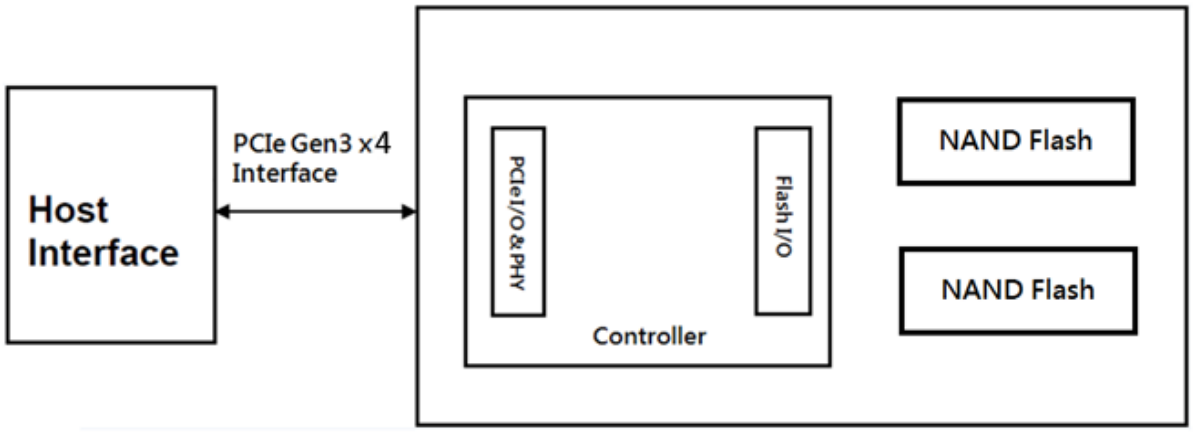


Figure 2-1 Functional Block Diagram

3. Pin Assignments

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU	A
B	DNU	DNU		DNU		NC		DNU			DNU		DNU		DNU		DNU	DNU	B
C	GND	GND	GND	GND	GND	DNU	XTAL_OUT	XTAL_IN	DNU	RZQ_1	GPG	DNU	RFU	RFU	GND	GP9/SW	DNU	DNU	C
D				PCIE_REFCLKP	PCIE_REFCLKN	GND	PRESET#	PCLKREQ#	VCC	VCC	GND	GPS	URX/UA1	NC	RFU				D
E	GND	GND	GND	GND	GND	GND	GND	NC	VCC	VCC	GND	NC	UTX/UA0	GND	GND	DNU	DNU	DNU	E
F				PRXP0	PRXN0	GND								NC	RFU				F
G	GND	GND	GND	GND	GND		VDDI	VDDI	GND	GND	VDDI	VDDI		GND	GND	DNU	DNU	DNU	G
H				PTXP0	PTXN0		VDDI	VDDI	GND	GND	VDDI	VDDI		RFU	GP7/PLN#				H
J	GND	GND	GND	GND	GND		VDDI	VDDI	GND	GND	VDDI	VDDI		GND	GND	DNU	DNU	DNU	J
K				PRXP1	PRXN1		GND	GND	GND	GND	GND	GND		RFU	GP8/PLA#				K
L	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	DNU	JT_TRST#	L
M				PTXP1	PTXN1		RFU	RFU	GND	GND	RFU	RFU		RFU	RFU				M
N	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	JT_TCK	JT_TMS	N
P				PRXP2	PRXN2		GND	GND	GND	GND	GND	GND		RFU	RFU				P
R	GND	GND	GND	GND	GND		VCCQ	VCCQ	GND	GND	VCCQ	VCCQ		GND	GND	DNU	JT_TDI	JT_TDO	R
T				PTXP2	PTXN2		1V8	1V8	GND	GND	VCCQ	VCCQ		RFU	RFU				T
U	GND	GND	GND	GND	GND		1V8	1V8	GND	GND	VCCQ	VCCQ		GND	GND	DNU	SCL	SDA	U
V				PRXP3	PRXN3									RFU	RFU				V
W	GND	GND	GND	GND	GND	GND	LED_1#/GP4	RFU	VCC	VCC	GND	RFU	RFU	GND	GND	DNU	DNU	ALERT#/GP3	W
Y				PTXP3	PTXN3	GND	GP2	GP1	VCC	VCC	GND	RESET#	GND	DNU	DNU				Y
AA	GND	GND	GND	GND	GND	DNU	GP0	DNU	TP	RZQ_2	DNU	TMOD	DNU	GND	GND	DNU	DNU	DNU	AA
AB	VDD	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU	AB
AC	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU	AC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

Table 3-1 Pin Layout

Table 3-1 Pin Assignments

Signal Name	Ball Number (BGA 291)	Pin Type		Description
PCIE_REFCLKP	D4	I	PCIe interface	PCIe Reference Clock P
PCIE_REFCLKN	D5	I		PCIe Reference Clock N
PRXP0	F4	I		PCIe Lane 0 Receiver Differential Signal P
PRXN0	F5	I		PCIe Lane 0 Receiver Differential Signal N
PTXP0	H4	O		PCIe Lane 0 Transmitter Differential Signal P
PTXN0	H5	O		PCIe Lane 0 Transmitter Differential Signal N
PRXP1	K4	I		PCIe Lane 1 Receiver Differential Signal P
PRXN1	K5	I		PCIe Lane 1 Receiver Differential Signal N
PTXP1	M4	O		PCIe Lane 1 Transmitter Differential Signal P

Signal Name	Ball Number (BGA 291)	Pin Type		Description
PTXN1	M5	O	PCIe interface	PCIe Lane 1 Transmitter Differential Signal N
PRXP2	P4	I		PCIe Lane 2 Receiver Differential Signal P
PRXN2	P5	I		PCIe Lane 2 Receiver Differential Signal N
PTXP2	T4	O		PCIe Lane 2 Transmitter Differential Signal P
PTXN2	T5	O		PCIe Lane 2 Transmitter Differential Signal N
PRXP3	V4	I		PCIe Lane 3 Receiver Differential Signal P
PRXN3	V5	I		PCIe Lane 3 Receiver Differential Signal N
PTXP3	Y4	O		PCIe Lane 3 Transmitter Differential Signal P
PTXN3	Y5	O		PCIe Lane 3 Transmitter Differential Signal N
PCLKREQ#	D8	I/O		PCIe Clock Request, Active Low
PRESET#	D7	I		PCIe Interface Hardware Reset, Active Low
XTAL_OUT	C7	O	Crystal	Crystal Output
XTAL_IN	C8	I		Crystal Input
RZQ_1	C10	N/A	ZQ	Memory or NAND calibration resistor
RZQ_2	AA10	N/A		Memory or NAND calibration resistor
RESET#	Y12	I	Reset	Power-on Reset, Active Low
TMOD	AA12	I	Test	ATE Test Mode Select
TP	AA9	O		Analog Test Output
GP0	AA7	I/O	Debug GPIO (1.8V)	General Purpose Input and Output 0
GP1	Y8	I/O		General Purpose Input and Output 1
GP2	Y7	I/O		General Purpose Input and Output 2 / Write Protect – Low active
ALERT#/GP3	W18	I/O		Alert notification to master (Output, Active Low) / General Purpose Input and Output 3
LED_1#/GP4	W7	I/O		Signal output to drive an external transistor to provide status indication via LED device (Output, Active Low) / General Purpose Input and Output 4
GP5	D12	I/O		General Purpose Input and Output 5
GP6	C11	I/O		General Purpose Input and Output 6
GP7/PLN#	H15	I/O		General Purpose Input and Output 7 / Power Loss Notification (Input, Active low)
GP8/PLA#	K15	I/O		General Purpose Input and Output 8 / Power Loss Acknowledgement (Output, Active Low)
GP9/SW	C16	I/O		General Purpose Input and Output 9 / Security Wipe
SDA	U18	I/O	I2C/ SMBus (1.8V)	I2C Data / SMBus Data - Open Drain
SCL	U17	I/O		I2C Clock / SMBus Clock - Open Drain
UTX/UAO	E13	O	UART (1.8V)	UART Transmitter / UART Output
URX/UAI	D13	I		UART Receiver / UART Input
JT_TMS	N18	I	JTAG (1.8V)	JTAG Mode Select
JT_TDI	R17	I		JTAG Data Input
JT_TRST#	L18	I		JTAG Reset, Active Low
JT_TDO	R18	O		JTAG Data Output
JT_TCK	N17	I		JTAG Clock

Signal Name	Ball Number (BGA 291)	Pin Type	Description
VCC	D9, D10, E9, E10, W9, W10, Y9, Y10	Power (3.3V)	External Power Supply
VCCQ	R7, R8, R11, R12, T11, T12, U11, U12	Power (1.2V)	External Power Supply
VDDI	G7, G8, G11, G12, H7, H8, H11, H12, J7, J8, J11, J12	Power (1.2V)	Power Supply for LDO
VDD	AB1	Power (0.9V)	LDO Output - Core Power
1V8	T7, T8, U7, U8	Power (1.8V)	External Power Supply
GND	C1, C2, C3, C4, C5, C15, D6, D11, E1, E2, E3, E4, E5, E6, E7, E11, E14, E15, F6, G1, G2, G3, G4, G5, G9, G10, G14, G15, H9, H10, J1, J2, J3, J4, J5, J9, J10, J14, J15, K7, K8, K9, K10, K11, K12, L1, L2, L3, L4, L5, L14, L15, M9, M10, N1, N2, N3, N4, N5, N14, N15, P7, P8, P9, P10, P11, P12, R1, R2, R3, R4, R5, R9, R10, R14, R15, T9, T10, U1, U2, U3, U4, U5, U9, U10, U14, U15, W1, W2, W3, W4, W5, W6, W11, W14, W15, Y6, Y11, Y13, AA1, AA2, AA3, AA4, AA5, AA14, AA15	Ground	Ground
DNU	A1, A2, A4, A6, A8, A11, A13, A15, A17, A18, B1, B2, B4, B8, B11, B13, B15, B17, B18, C6, C9, C12, C17, C18, E16, E17, E18, G16, G17, G18, J16, J17, J18, L16, L17, N16, R16, U16, W16, W17, Y14, Y15, AA6, AA8, AA11, AA13, AA16, AA17, AA18, AB2, AB4, AB6, AB8, AB11, AB13, AB15, AB17, AB18, AC1, AC2, AC4, AC6, AC8, AC11, AC13, AC15, AC17, AC18	NC	Do Not Use
NC	B6, D14, E8, E12, F14	NC	Not Connect

Signal Name	Ball Number (BGA 291)	Pin Type	Description
RFU	C13, C14, D15, F15, H14, K14, L7, L8, L9, L10, L11, L12, M7, M8, M11, M12, M14, M15, N7, N8, N9, N10, N11, N12, P14, P15, T14, T15, V14, V15, W8, W12, W13	NC	Reserved for Future Use

Notes:
- Pin Type: I - Input Only, O - Output Only, I/O - Input and Output
- "P" and "N" in differential signals, e.g. RX0**P** and RX0**N**, mean positive-end signal and negative- end signal.
- In signal names with "#", e.g. PCLKREQ#, PRESET#, RESET# and JT_TRST#, the "#" means "active low".

4. Product Specifications

4.1 Capacity

Capacity specifications of PV920-µSSD are available as shown in Table 4-1. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

Table 4-1 Capacity Specifications

Capacity	Total bytes	Total LBA
120 GB	120,034,123,776	234,441,648
240 GB	240,057,409,536	468,862,128
480 GB	480,103,981,056	937,703,088
960 GB	960,197,124,096	1,875,385,008

Notes:
- Display of total bytes varies from operating systems.
- 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.
- LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

4.2 Performance

Performance of PV920-µSSD is listed below in Table 4-2.

Table 4-2 Performance Specifications

Performance \ Capacity	120 GB	240 GB	480 GB	960 GB
Sequential Read (MB/s)	1,440	3,030	3,220	3,160
Sequential Write (MB/s)	650	1,355	2,215	2,705
Random Read IOPS (4K)	50,000	100,000	191,000	311,000
Random Write IOPS (4K)	150,000	261,000	277,000	263,000

Notes:
- Measured with OS version: Win10 (64bit), version 1803 with HMB (Host Memory Buffer), performance may differ from various flash configurations or host system settings.
- Sequential performance is based on CrystalDiskMark 5.2.1 with file size 1,000MB.
- Random performance measured using IOMeter with Queue Depth 32.

4.3 Environmental Specifications

Environmental specifications of PV920-µSSD are shown in Table 4-3.

Table 4-3 Environmental Specifications

Item	Specifications
Operating temp.	0°C to 70°C (Standard); -40°C to 85°C (Wide)
Non-operating temp.	-40°C to 85°C
Operating humidity	20~95%
Non-operating humidity	20~95%

Note: This Environmental Specification table indicates the conditions for testing the device. Real world usages may affect the results.

4.4 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in PV920-µSSD. The prediction result for PV920-µSSD is more than 3,000,000 hours.

Note: The MTBF is predicated and calculated based on “Telcordia Technologies Special Report, SR-332, Issue 3” method.

4.5 Certification and Compliance

PV920-µSSD complies with the following standards:

- CE
- FCC
- RoHS
- BSMI

4.6 Endurance

The endurance of a storage device is predicted by Drive Writes Per Day based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

Table 4-4 Endurance Specifications

Capacity	Drive Writes Per Day
120 GB	1.23
240 GB	1.25
480 GB	1.25
960 GB	1.22

Notes:

- This estimation complies with JEDEC JESD-219, enterprise endurance workload of random data with payload size distribution.
- Flash vendor guaranteed 3D NAND TLC P/E cycle: 3K
- WAF may vary from capacity, flash configurations and writing behavior on each platform.
- 1 Terabyte = 1,024GB
- DWPD (Drive Writes Per Day) is calculated based on the number of times that user overwrites the entire capacity of an SSD per day of its lifetime during the warranty period. (3D NAND TLC warranty: 2 years)

5. Flash Management

5.1 Error Correction/Detection

PV920-µSSD implements a hardware ECC scheme, based on the Low Density Parity Check (LDPC). LDPC is a class of linear block error correcting code which has apparent coding gain over BCH code because LDPC code includes both hard decoding and soft decoding algorithms. With the error rate decreasing, LDPC can extend SSD endurance and increase data reliability while reading raw data inside a flash chip.

5.2 Bad Block Management

Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, page mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

5.3 Global Wear Leveling

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Global wear leveling is an important mechanism that levels out the wearing of all blocks so that the wearing-down of all blocks can be almost evenly distributed. This will increase the lifespan of SSDs.

5.4 Flash Translation Layer – Page Mapping

Page mapping is an advanced flash management technology whose essence lies in the ability to gather data, distribute the data into flash pages automatically, and then schedule the data to be evenly written. Page-level mapping uses one page as the unit of mapping. The most important characteristic is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different sizes of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. Thus, page mapping is adopted to increase random access speed and improve SSD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

5.5 Hyper Cache Technology

Apacer proprietary Hyper Cache technology uses a portion of the available capacity as SLC (1bit-per-cell) NAND flash memory, called Hyper cache mode. When data is written to SSD, the firmware will direct the data to Hyper Cache mode, providing excellent performance to handle various scenarios in industrial use.

5.6 Power Failure Management

Power Failure Management plays a crucial role when power supply becomes unstable. Power disruption may occur when users are storing data into the SSD, leading to instability in the drive. However, with Power Failure Management, a firmware protection mechanism will be activated to scan pages and blocks once power is resumed. Valid data will be transferred to new blocks for merging and the mapping table will be rebuilt. Therefore, data reliability can be reinforced, preventing damage to data stored in the NAND Flash.

5.7 TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks all the time.

5.8 Over-Provisioning

Over-Provisioning (OP) is a certain portion of the SSD capacity exclusively for increasing Garbage Collection (GC) efficiency, especially when the SSD is filled to full capacity or performs a heavy mixed-random workload. OP has the advantages of providing extended life expectancy, reliable data integrity, and high sustained write performance.

5.9 SMART Read Refresh™

Apacer's SMART Read Refresh plays a proactive role in avoiding read disturb errors from occurring to ensure health status of all blocks of NAND flash. Developed for read-intensive applications in particular, SMART Read Refresh is employed to make sure that during read operations, when the read operation threshold is reached, the data is refreshed by re-writing it to a different block for subsequent use.

5.10 NVMe Secure Erase

NVMe Secure Erase is an NVMe drive sanitize command currently embedded in most of the storage drives. Defined in NVMe specifications, NVMe Secure Erase is part of Format NVM command that allows storage drives to erase all user data areas. The erase process usually runs on the firmware level as most of the NVMe-based storage media currently in the market are built-in with this command. NVMe Secure Erase can securely wipe out the user data in the drive and protects it from malicious attack.

5.11 Write Protect

Apacer implements the Virtual Write scheme that allows write commands to go through the flash controller and data temporarily stored, but no data has been actually written into the flash. Once the system is reset and rebooted, the temporarily stored data will be lost and nowhere to be found in the system. Since the Virtual Write scheme runs at device level, it requires no software or driver installation and is independent from the host OS.

6. NVMe Support Features

6.1 Host Memory Buffer

Host Memory Buffer (HMB) allows HOST to allocate system memory for SSD’s exclusive use in order to provide better performance and endurance, especially for DRAMless solutions.

7. Security and Reliability Features

7.1 Thermal Sensor

Apacer Thermal Sensor is a digital temperature sensor with serial interface. By using designated pins for transmission, storage device owners are able to read temperature data.

7.2 Thermal Throttling

Thermal throttling can monitor the temperature of the SSD equipped with a built-in thermal sensor. This method can ensure the temperature of the device stays within temperature limits by drive throttling, i.e. reducing the speed of the drive when the device temperature reaches the threshold level, so as to prevent overheating, guarantee data reliability, and prolong product lifespan. When the temperature exceeds the maximum threshold level, thermal throttling will be triggered to reduce performance step by step to prevent hardware components from being damaged. Performance is only permitted to drop to the extent necessary for recovering a stable temperature to cool down the device's temperature. Once the temperature decreases to the minimum threshold value, transfer speeds will rise back to its optimum performance level.

7.3 Advanced Encryption Standard

Advanced Encryption Standard (AES) is a specification for the encryption of electronic data. AES has been adopted by the U.S. government since 2001 to protect classified information and is now widely implemented in embedded computing applications. The AES algorithm used in software and hardware is symmetric so that encrypting/decrypting requires the same encryption key. Without the key, the encrypted data is inaccessible to ensure information security.

Notably in flash memory applications, AES 256-bit hardware encryption is the mainstream to protect sensitive or confidential data. The hardware encryption provides better performance, reliability, and security than software encryption. It uses a dedicated processor, which is built inside the controller, to process the encryption and decryption. This enormously shortens the processing time and makes it efficient.

7.4 End-to-End Data Protection

End-to-End Data Protection is a feature implemented in Apacer SSD products that extends error control to cover the entire path from the host computer to the drive and back, and that ensures data integrity at multiple points in the path to enable reliable delivery of data transfers. Unlike ECC which does not exhibit the ability to determine the occurrence of errors throughout the process of data transmission, End-to-End Data Protection allows SSD controller to identify an error created anywhere in the path and report the error to the host computer before it is written to the drive. This error-checking and error-reporting mechanism therefore guarantees the trustworthiness and reliability of the SSD.

8. Software Interface

8.1 Command Set

Table 8-1 summarizes the commands supported by PV920-µSSD.

Table 8-1 Admin Commands

Opcode	Command Description
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Features
0Ah	Get Features
0Ch	Asynchronous Event Request
10h	Firmware Activate
11h	Firmware Image Download
14h	Device Self-test

Table 8-2 Admin Commands – NVM Command Set Specific

Opcode	Command Description
80h	Format NVM

Table 8-3 NVM Commands

Opcode	Command Description
00h	Flush
01h	Write
02h	Read
09h	Dataset Management

8.2 S.M.A.R.T.

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

Table 8-4 SMART (02h)

Byte	Length	Description
0	1	Critical Warning
1-2	2	Composite Temperature (NAND Flash)
3	1	Available Spare
4	1	Available Spare Threshold
5	1	Percentage Used (Average Erase Count / P/E Cycle Count)
6-31	26	Reserved
32-47	16	Data Units Read
48-63	16	Data Units Written
64-79	16	Host Read Commands
80-95	16	Host Write Commands
96-111	16	Controller Busy Time
112-127	16	Power Cycles
128-143	16	Power On Hours
144-159	16	Unsafe Shutdowns
160-175	16	Media and Data Integrity Errors
176-191	16	Number of Error Information Log Entries
192-195	4	Warning Composite Temperature Time
196-199	4	Critical Composite Temperature Time
200-201	2	Temperature Sensor 1: Controller Temperature
204-205	2	Temperature Sensor 3: NAND Flash Temperature
206-207	2	Temperature Sensor 4
208-209	2	Temperature Sensor 5
210-211	2	Temperature Sensor 6
212-213	2	Temperature Sensor 7
214-215	2	Temperature Sensor 8
216-511	296	Reserved

Table 8-5 SMART (C0h)

Byte	Length	Description
0-255	256	Reserved
256-257	2	SSD Protect Mode
258-261	4	Host Read UNC Count
262-265	4	PHY Error Count
266-269	4	CRC Error Count
270-273	4	Total Early Bad Block Count
274-277	4	Total Later Bad Block Count
278-281	4	Max Erase Count
282-285	4	Average Erase Count
286-289	4	Program Fail Count
290-293	4	Erase Fail Count
294-301	8	Flash Write Sector
302-305	4	Total Spare Block
306-309	4	Current Spare Block
310-313	4	Read Retry Count
314-511	210	Reserved

9. Electrical Specifications

9.1 Operating Voltage

Table 9-1 lists the supply voltage for PV920-µSSD.

Table 9-1 Operating Range

Parameter	Voltage	Range
VCC	3.3V	3.135V ~ 3.465V
1V8	1.8V	1.71V ~1.89V
VCCQ	1.2V	1.14V ~ 1.26V
VDDI	1.2V	1.14V ~ 1.26V

9.2 Power Consumption

Table 9-2 lists the power consumption for PV920-µSSD.

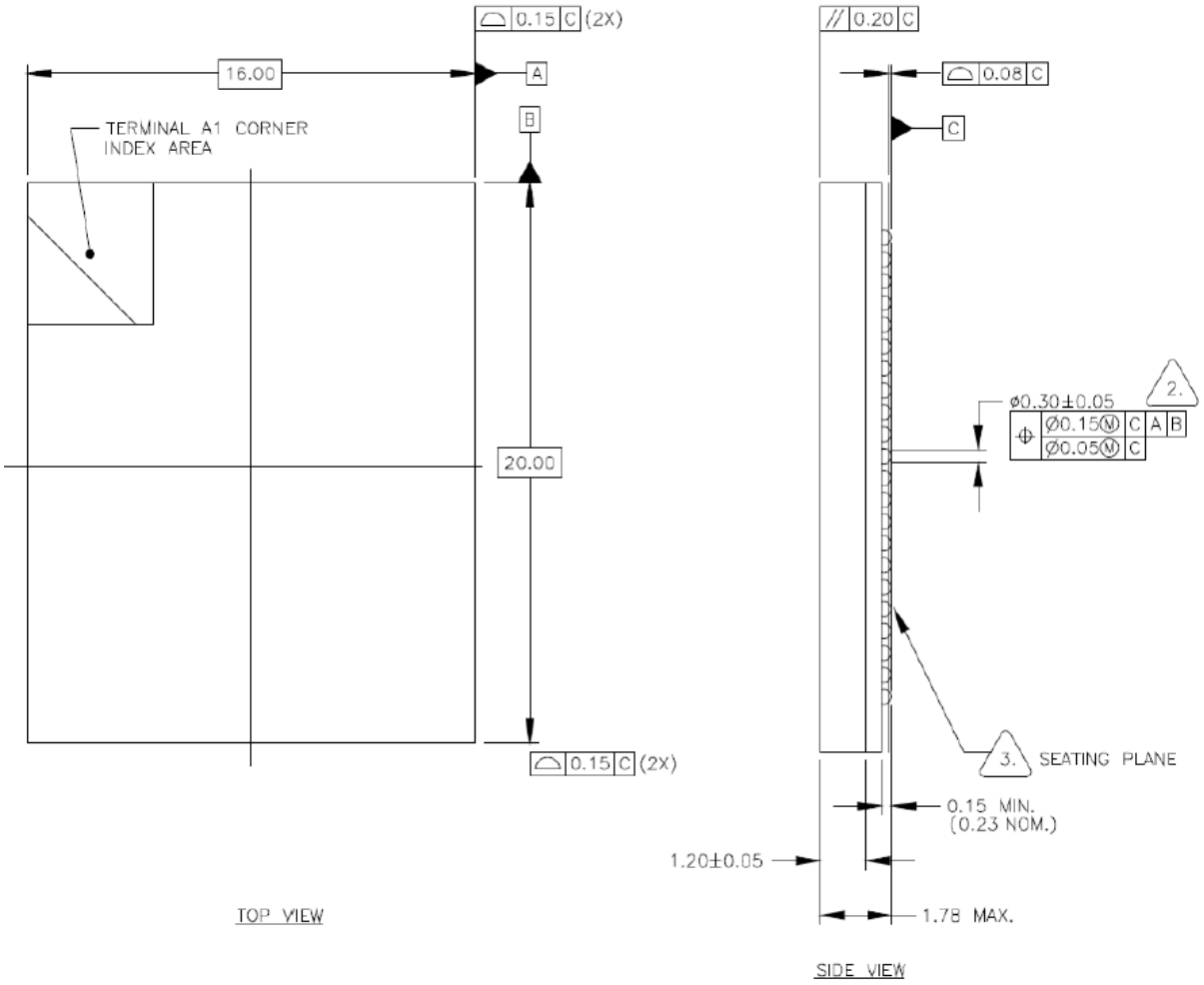
Table 9-2 Power Consumption

Capacity / Mode	120 GB	240 GB	480 GB	960 GB
Active (mA)	605	890	1,105	1,260
Idle (mA)	320	310	310	310

Notes:
- All values are typical and may vary depending on flash configurations or host system settings.
- Active power is an average power measurement performed using CrystalDiskMark with 128KB sequential read/write transfers.
- All values represent the total voltage measured based on an evaluation board.

10. Physical Characteristics

10.1 960GB



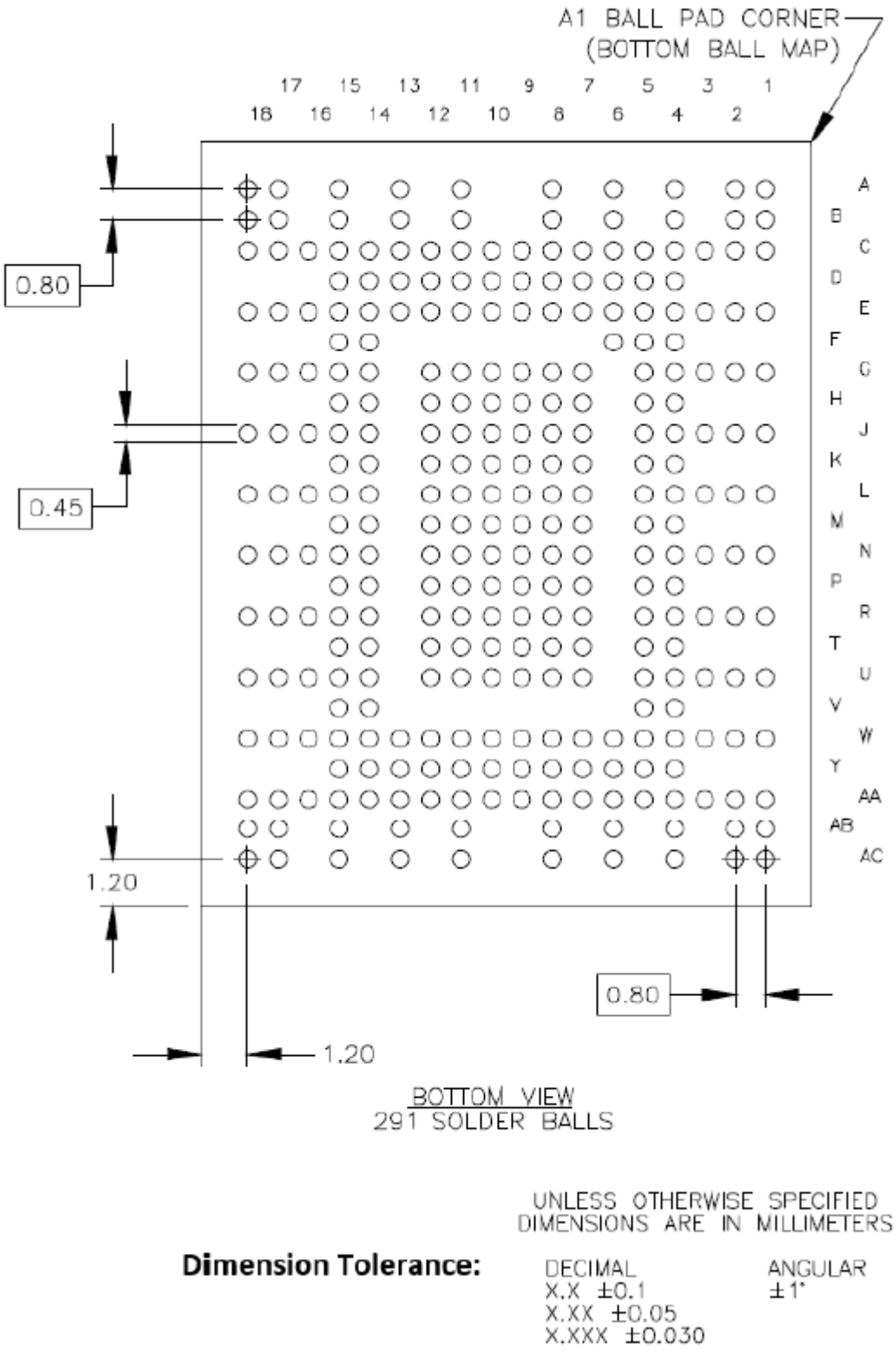
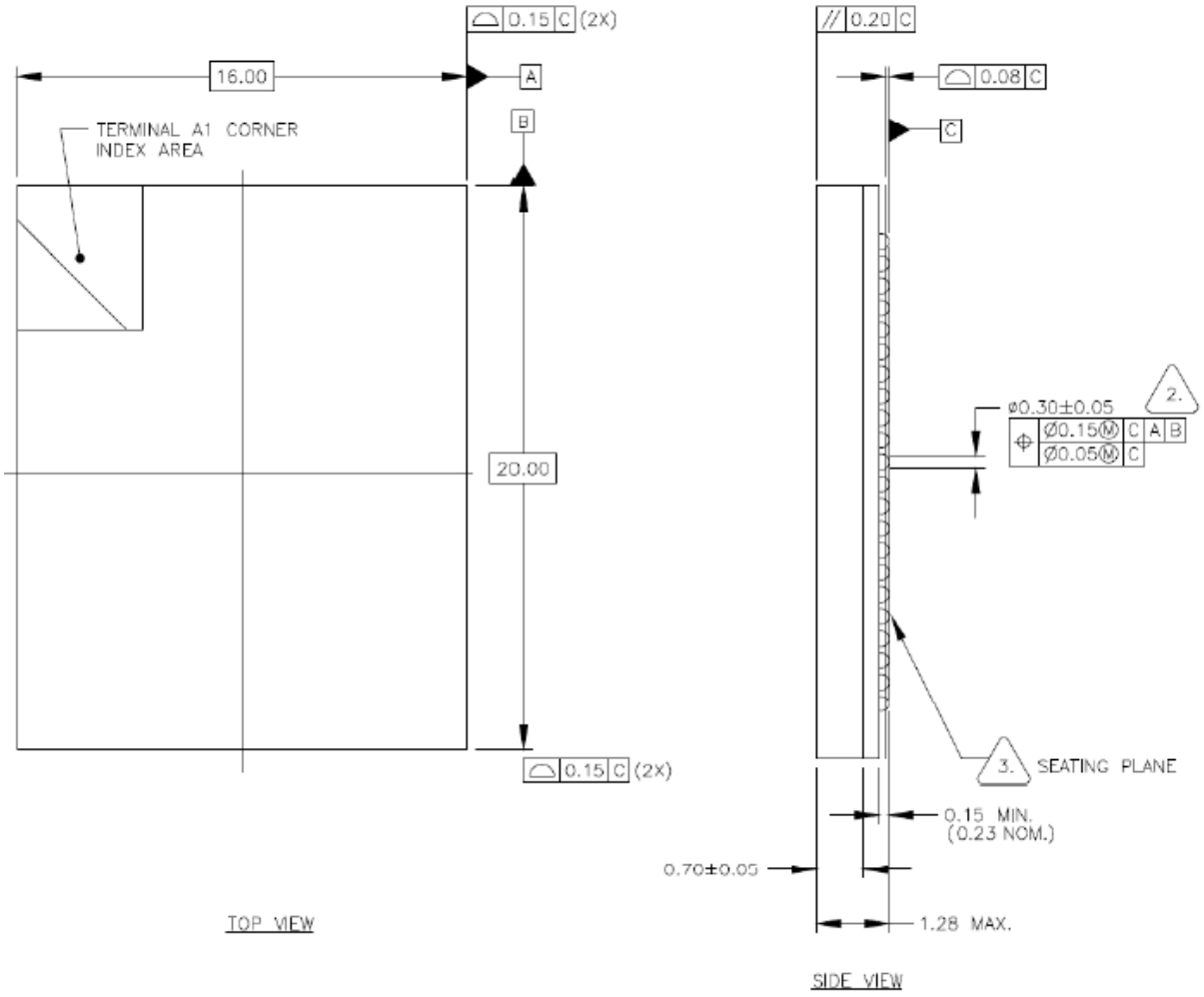


Figure 10-1 960GB Dimensions

10.2 120-480GB



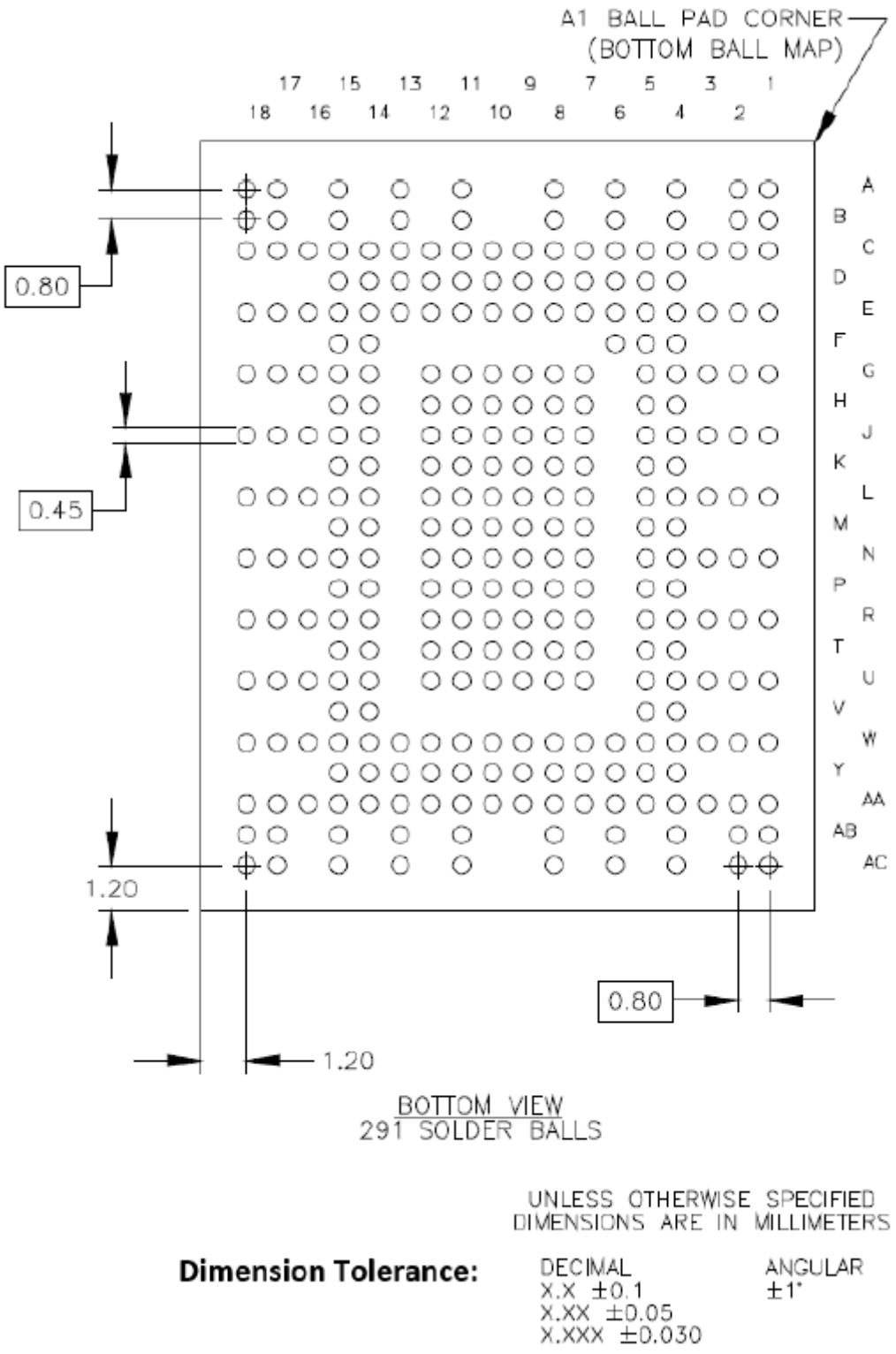


Figure 10-2 120-480GB Dimensions

11. Product Ordering Information

11.1 Product Code Designations

Apacer's PV920-µSSD is available in different configurations and densities. See the chart below for a comprehensive list of options for the PV920-µSSD series devices.

Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	B	H	6	.	9	2	5	X	X	A	.	0	0	1	0	2

Code 1-3 (Product Line & Form Factor)	PV920-µSSD
Code 5-6 (Model/Solution)	PV920
Code 7-8 (Product Capacity)	5H: 120GB 5J: 240GB 5K: 480GB 5L: 960GB
Code 9 (Flash Type & Product Temp)	G: 3D TLC Standard Temperature H: 3D TLC Wide Temperature
Code 10 (Product Spec)	PCIe BGA SSD
Code 12-14 (Version Number)	Random numbers generated by system
Code 15-16 (Firmware Version)	Thermal Throttling Write Protect + OP

11.2 Valid Combinations

The following tables list the available models of the PV920-µSSD series which are in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Capacity	Standard Temperature	Wide Temperature
120GB	BH6.925HGA.00102	BH6.925HHA.00102
240GB	BH6.925JGA.00102	BH6.925JHA.00102
480GB	BH6.925KGA.00102	BH6.925KHA.00102
960GB	BH6.925LGA.00102	BH6.925LHA.00102

Revision History

Revision	Description	Date
1.0	Initial release	7/21/2021
1.1	- Added ball number to Form Factor on Specifications Overview page - Updated Table 3-1 by adding “BGA 291” to the Ball Number header, removing 1.8V from pin type of signal VCCQ and revising the description of signal 1V8 - Updated Table 9-1 by adding parameter 1V8 and modifying voltage and range of parameter VCCQ - Added a note regarding measuring method to 9.2 Power Consumption	8/11/2021
1.2	Added standard temperature support	8/31/2021
1.3	Removed “optional” from the description for signal GP2 at Table 3-1	5/23/2022

Global Presence

Taiwan (Headquarters)
Apacer Technology Inc.
1F., No.32, Zhongcheng Rd., Tucheng Dist.,
New Taipei City 236, Taiwan R.O.C.
Tel: 886-2-2267-8000
Fax: 886-2-2267-2261
amtsales@apacer.com

U.S.A.
Apacer Memory America, Inc.
46732 Lakeview Blvd., Fremont, CA 94538
Tel: 1-408-518-8699
Fax: 1-510-249-9551
sa@apacerus.com

Japan
Apacer Technology Corp.
6F, Daiyontamachi Bldg., 2-17-12, Shibaura, Minato-Ku,
Tokyo, 108-0023, Japan
Tel: 81-3-5419-2668
Fax: 81-3-5419-0018
jpservices@apacer.com

Europe
Apacer Technology B.V.
Science Park Eindhoven 5051 5692 EB Son,
The Netherlands
Tel: 31-40-267-0000
Fax: 31-40-290-0686
sales@apacer.nl

China
Apacer Electronic (Shanghai) Co., Ltd
Room D, 22/FL, No.2, Lane 600, JieyunPlaza,
Tianshan RD, Shanghai, 200051, China
Tel: 86-21-6228-9939
Fax: 86-21-6228-9936
sales@apacer.com.cn

India
Apacer Technologies Pvt Ltd,
1874, South End C Cross, 9th Block Jayanagar,
Bangalore-560069, India
Tel: 91-80-4152-9061/62
Fax: 91-80-4170-0215
sales_india@apacer.com