Apacer

RoHS Compliant

PCI Express BGA Solid State Drive

PT910-µSSD Product Specifications

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Version 1.1

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Specifications Overview:

- **PCIe Interface**
  - Compliant with NVMe 1.3
  - Compatible with PCIe Gen3 x2 interface
- **Capacity**
  - 30, 60, 120, 240 GB
- **Performance***
  - Interface burst read/write: 2 GB/sec
  - Sequential read: up to 1,725 MB/sec
  - Sequential write: up to 1,230 MB/sec
  - Random read (4K): up to 168,000 IOPS
  - Random write (4K): up to 135,000 IOPS
- **Flash Management**
  - Low-Density Parity-Check (LDPC) Code
  - Global Wear Leveling
  - Flash bad-block management
  - Flash Translation Layer: Page Mapping
  - Power Failure Management
  - S.M.A.R.T.
  - TRIM
  - Hyper Cache Technology
  - Over-Provisioning
  - SMART Read Refresh™
  - NVMe Secure Erase
- **NAND Flash Type:** 3D TLC (BiCS4)
- **MTBF:** >3,000,000 hours
- **Endurance (in drive writes per day: DWPD)**
  - 30 GB: 2.77 DWPD
  - 60 GB: 3 DWPD
  - 120 GB: 2.96 DWPD
  - 240 GB: 2.94 DWPD
- **Temperature Range**
  - Operating: 0°C to 70°C
  - Storage: -40°C to 85°C
- **Supply Voltage**
  - 3.3 V ± 5%
  - 1.8 V ± 5%
  - 1.2 V ± 5%
- **Power Consumption***
  - Active mode: 570 mA
  - Idle mode: 145 mA
- **Form Factor**
  - PCIe BGA SSD (M.2 1113)
  - Dimensions: 11.5 x 13.0 x 1.4, unit: mm
  - 345 balls
- **Security**
  - AES 256-bit hardware encryption
- **Reliability**
  - Thermal Sensor
  - Thermal Throttling
  - End-to-End Data Protection
- **Power Management**
  - Supports APST
  - Supports ASPM L1.2
- **NVMe Features****
  - Supports HMB (Host Memory Buffer)
- **RoHS Compliant**

*Varies from capacities. The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings.
**Windows 10 (version 1703) onwards supports the HMB (Host Memory Buffer) function.

Table of Contents

1. General Descriptions

Apacer PCIe BGA SSD PT910-µSSD (M.2 1113) presents a revolutionary breakthrough of NAND flash storage technology. This micro sized SSD delivers all the technological benefits in NAND based storage solution with ultra speed PCIe Gen3x2 interface in an embedded BGA form factor, compatible with JEDEC PCIe M.2 1113. Formed in a size of an IC chip, the performance level can reach up to 670 MB/s for read and 585 MB/s for write. With its micro-size and ultra speed, PT910-µSSD is definitely the ideal storage solution for high performance demand mobile devices.

2. Functional Block

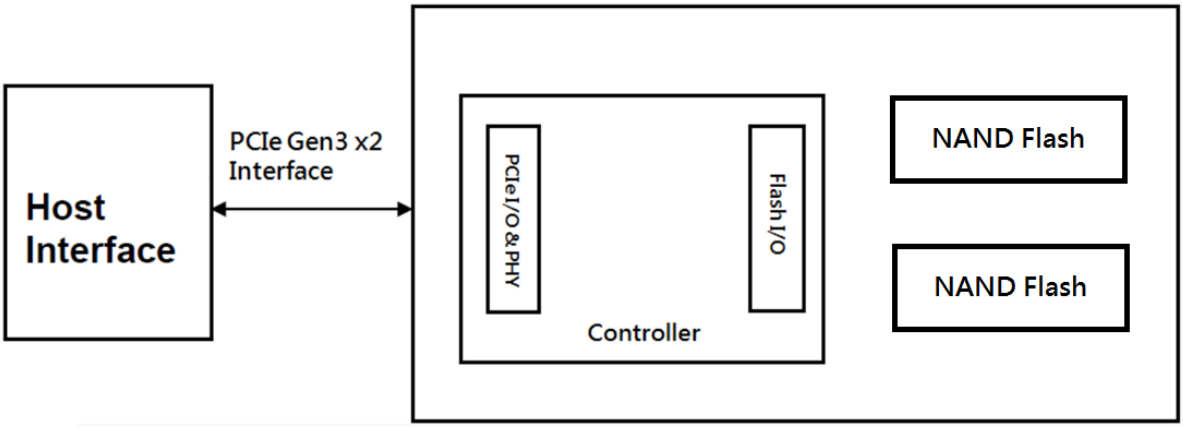

Figure 2-1 Functional Block Diagram

3. Pin Assignments

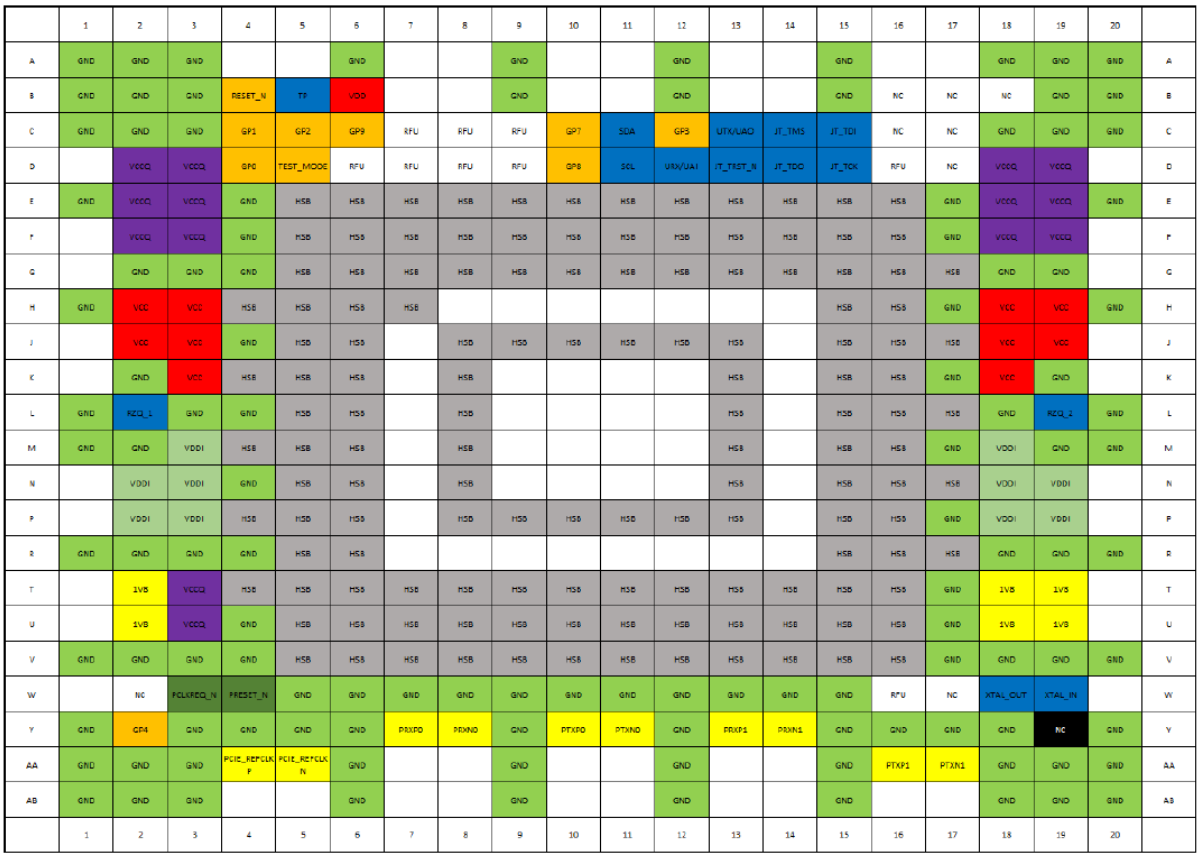

Table 3-1 Pin Layout

Table 3-1 Pin Assignments

Signal Name	Ball Number (BGA 345)	Pin Type*		Description
PCIE_REFCLKP	AA4	I	PCIe interface	PCIe Reference Clock P
PCIE_REFCLKN	AA5	I		PCIe Reference Clock N
PTXP1	AA16	O		PCIe Lane 1 Transmitter Differential Signal P
PTXN1	AA17	O		PCIe Lane 1 Transmitter Differential Signal N
PRXP1	Y13	I		PCIe Lane 1 Receiver Differential Signal P
PRXN1	Y14	I		PCIe Lane 1 Receiver Differential Signal N
PTXP0	Y10	O		PCIe Lane 0 Transmitter Differential Signal P
PTXN0	Y11	O		PCIe Lane 0 Transmitter Differential Signal N
PRXP0	Y7	I		PCIe Lane 0 Receiver Differential Signal P
PRXN0	Y8	I		PCIe Lane 0 Receiver Differential Signal N
PCLKREQ_N	W3	I/O		PCIe Clock Request

Note:
*Pin Type: I - Input Only, O - Output Only, I/O - Input and Output
***"P" and "N" in differential signals, e.g. PTXP1 and PTXN1, mean positive-end signal and negative-end signal.
***In signal names with "_N", e.g. PCLKREQ_N, PRESET_N, RESET_N and JT_TRST_N, the "_N" means "active low".

Signal Name	Ball Number (BGA 345)	Pin Type*		Description
PRESET_N	W4	I		PCIe Interface Hardware Reset
XTAL_OUT	W18	O	Crystal	Crystal Output
XTAL_IN	W19	I		Crystal Input
RZQ_1	L2	N/A	ZQ	Memory or NAND calibration resistor
RZQ_2	L19	N/A		Memory or NAND calibration resistor
RESET_N	B4	I	Reset	Power-on Reset
TEST_MODE	D5	I	Test	ATE Test Mode Select
TP	B5	O		Analog Test Output
GP0	D4	I/O	Debug	General Purpose Input and Output, for Vendor Test
GP1	C4	I/O		
GP2	C5	I/O		
GP3	C12	I/O		
GP4	Y2	I/O		
GP7	C10	I/O		
GP8	D10	I/O		
GP9	C6	I/O		
SDA	C11	I/O	I2C	I2C Data, Open Drain
SCL	D11	I/O		I2C Clock, Open Drain
UTX/UAO	C13	O	UART	UART Transmit / Output
URX/UAI	D12	I		UART Receive / Input
JT_TMS	C14	I	JTAG	JTAG Mode Select
JT_TDI	C15	I		JTAG Data Input
JT_TRST_N	D13	I		JTAG Reset
JT_TDO	D14	O		JTAG Data Output
JT_TCK	D15	I		JTAG Clock
VCC	H2, H3, H18, H19, J2, J3, J18, J19, K3, K18	Power	POWER	(3.3V) External Power Supply
VCCQ	D2, D3, D18, D19, E2, E3, E18, E19, F2, F3, F18, F19, T3, U3	Power		(1.2/1.8V) External Power Supply
VDDI	M3, M18, N2, N3, N18, N19, P2, P3, P18, P19	Power		(1.2V) Power Supply for LDO
VDD	B6	Power		LDO Output - Core Digital Signal
1V8	T2, T18, T19, U2, U18, U19	Power		1.8V Power for PCIe/PLL/Digital Input and Output, Power Supplier Used by ATE
GND	A1, A2, A3, A6, A9, A12, A15, A18, A19, A20, AA1, AA2, AA3, AA6, AA9, AA12, AA15, AA18, AA19, AA20, AB1, AB2, AB3, AB6, AB9, AB12, AB15, AB18, AB19, AB20, B1, B2, B3, B9, B12, B15, B19, B20, C1, C2, C3, C18, C19, C20, E1, E4, E17, E20, F4, F17, G2, G3, G4, G18, G19, H1, H17,	Ground	Ground	Ground

Signal Name	Ball Number (BGA 345)	Pin Type*		Description
	H20, J4, K2, K17, K19, L1, L3, L4, L18, L20, M1, M2, M17, M19, M20, N4, P17, R1, R2, R3, R4, R18, R19, R20, T17, U4, U17, V1, V2, V3, V4, V17, V18, V19, V20, W5, W6, W7, W8, W9, W10, W11, W12, W13, W14, W15, Y1, Y3, Y4, Y5, Y6, Y9, Y12, Y15, Y16, Y17, Y18, Y20			
HSB	E5, E6, E7, E8, E9, E10, E11, E12, E13, E14, E15, E16, F5, F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, F16, G5, G6, G7, G8, G9, G10, G11, G12, G13, G14, G15, G16, G17, H4, H5, H6, H7, H15, H16, J5, J6, J8, J9, J10, J11, J12, J13, J15, J16, J17, K4, K5, K6, K8, K13, K15, K16, L5, L6, L8, L13, L15, L16, L17, M4, M5, M6, M8, M13, M15, M16, N5, N6, N8, N13, N15, N16, N17, P4, P5, P6, P8, P9, P10, P11, P12, P13, P15, P16, R5, R6, R15, R16, R17, T4, T5, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, U5, U6, U7, U8, U9, U10, U11, U12, U13, U14, U15, U16, V5, V6, V7, V8, V9, V10, V11, V12, V13, V14, V15, V16		NC	Host specific balls
RFU	C7, C8, C9, D6, D7, D8, D9, D16, W16		NC	Reserved for future use
NC	B16, B17, B18, C16, C17, D17, W2, W17		NC	Not Connect

4. Product Specifications

4.1 Capacity

Capacity specifications of PT910-µSSD are available as shown in Table 4-1. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

Table 4-1 Capacity Specifications

Capacity	Total bytes*	Total LBA
30 GB	30,016,659,456	58,626,288
60 GB	60,022,480,896	117,231,408
120 GB	120,034,123,776	234,441,648
240 GB	240,057,409,536	468,862,128

*Display of total bytes varies from file systems, which means not all of the bytes can be used for storage.
**Notes: 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.
LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

4.2 Performance

Performance of PT910-µSSD is listed below in Table 4-2.

Table 4-2 Performance Specifications

Capacity / Performance	30 GB	60 GB	120 GB	240 GB
Sequential Read* (MB/s)	405	815	1,640	1,725
Sequential Write* (MB/s)	160	335	635	1,230
Random Read IOPS (4K)**	18,000	45,000	94,000	168,000
Random Write IOPS (4K)**	15,000	69,000	119,000	135,000

Note:
Measured with OS version: Win10 (64bit), version 1803 with HMB (Host Memory Buffer), performance may differ from various flash configurations or host system settings.
*Sequential performance is based on CrystalDiskMark 5.2.1 with file size 1,000MB.
**Random performance measured using IOMeter with Queue Depth 32.

4.3 Environmental Specifications

Environmental specifications of PT910-µSSD are shown in Table 4-3.

Table 4-3 Environmental Specifications

Item	Specifications
Operating temp.	0°C to 70°C
Non-operating temp.	-40°C to 85°C
Operating humidity	20~95%
Non-operating humidity	20~95%

4.4 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in PT910-µSSD. The prediction result for PT910-µSSD is more than 3,000,000 hours.

Note: The MTBF is predicated and calculated based on “Telcordia Technologies Special Report, SR-332, Issue 3” method.

4.5 Certification and Compliance

PT910-µSSD complies with the following standards:

- CE
- FCC
- RoHS
- BSMI

4.6 Endurance

The endurance of a storage device is predicted by Drive Writes Per Day based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

Table 4-4 Drive Writes Per Day

Capacity	Drive Writes Per Day
30 GB	2.77
60 GB	3
120 GB	2.96
240 GB	2.94

Note:

- This estimation complies with JEDEC random client workload.
- Flash vendor guaranteed 3D NAND TLC P/E cycle: 3K
- WAF may vary from capacity, flash configurations and writing behavior on each platform.
- 1 Terabyte = 1,024GB
- DWPD (Drive Writes Per Day) is calculated based on the number of times that user overwrites the entire capacity of an SSD per day of its lifetime during the warranty period. (3D NAND TLC warranty: 2 years)

5. Flash Management

5.1 Error Correction/Detection

PT910-µSSD implements a hardware ECC scheme, based on the Low Density Parity Check (LDPC). LDPC is a class of linear block error correcting code which has apparent coding gain over BCH code because LDPC code includes both hard decoding and soft decoding algorithms. With the error rate decreasing, LDPC can extend SSD endurance and increase data reliability while reading raw data inside a flash chip.

5.2 Bad Block Management

Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, page mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

5.3 Global Wear Leveling

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Global wear leveling is an important mechanism that levels out the wearing of all blocks so that the wearing-down of all blocks can be almost evenly distributed. This will increase the lifespan of SSDs.

5.4 Flash Translation Layer – Page Mapping

Page mapping is an advanced flash management technology whose essence lies in the ability to gather data, distribute the data into flash pages automatically, and then schedule the data to be evenly written. Page-level mapping uses one page as the unit of mapping. The most important characteristic is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different sizes of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. Thus, page mapping is adopted to increase random access speed and improve SSD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

5.5 Power Failure Management

Power Failure Management plays a crucial role when power supply becomes unstable. Power disruption may occur when users are storing data into the SSD, leading to instability in the drive. However, with Power Failure Management, a firmware protection mechanism will be activated to scan pages and blocks once power is resumed. Valid data will be transferred to new blocks for merging and the mapping table will be rebuilt. Therefore, data reliability can be reinforced, preventing damage to data stored in the NAND Flash.

5.6 TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks all the time.

5.7 Hyper Cache Technology

Apacer proprietary Hyper Cache technology uses a portion of the available capacity as SLC (1bit-per-cell) NAND flash memory, called Hyper cache mode. When data is written to SSD, the firmware will direct the data to Hyper Cache mode, providing excellent performance to handle various scenarios in industrial use.

5.8 Over-Provisioning

Over-Provisioning (OP) is a certain portion of the SSD capacity exclusively for increasing Garbage Collection (GC) efficiency, especially when the SSD is filled to full capacity or performs a heavy mixed-random workload. OP has the advantages of providing extended life expectancy, reliable data integrity, and high sustained write performance.

5.9 SMART Read Refresh™

Apacer's SMART Read Refresh plays a proactive role in avoiding read disturb errors from occurring to ensure health status of all blocks of NAND flash. Developed for read-intensive applications in particular, SMART Read Refresh is employed to make sure that during read operations, when the read operation threshold is reached, the data is refreshed by re-writing it to a different block for subsequent use.

5.10 NVMe Secure Erase

NVMe Secure Erase is an NVMe drive sanitize command currently embedded in most of the storage drives. Defined in NVMe specifications, NVMe Secure Erase is part of Format NVM command that allows storage drives to erase all user data areas. The erase process usually runs on the firmware level as most of the NVMe-based storage media currently in the market are built-in with this command. NVMe Secure Erase can securely wipe out the user data in the drive and protects it from malicious attack.

6. NVMe Support Features

6.1 Host Memory Buffer

Host Memory Buffer (HMB) allows HOST to allocate system memory for SSD's exclusive use in order to provide better performance and endurance, especially for DRAMless solutions.

7. Security & Reliability Features

7.1 Thermal Sensor

Apacer Thermal Sensor is a digital temperature sensor with serial interface. By using designated pins for transmission, storage device owners are able to read temperature data.

7.2 Thermal Throttling

Thermal throttling can monitor the temperature of the SSD equipped with a built-in thermal sensor. This method can ensure the temperature of the device stays within temperature limits by drive throttling, i.e. reducing the speed of the drive when the device temperature reaches the threshold level, so as to prevent overheating, guarantee data reliability, and prolong product lifespan. When the temperature exceeds the maximum threshold level, thermal throttling will be triggered to reduce performance step by step to prevent hardware components from being damaged. Performance is only permitted to drop to the extent necessary for recovering a stable temperature to cool down the device's temperature. Once the temperature decreases to the minimum threshold value, transfer speeds will rise back to its optimum performance level.

7.3 Advanced Encryption Standard

Advanced Encryption Standard (AES) is a specification for the encryption of electronic data. AES has been adopted by the U.S. government since 2001 to protect classified information and is now widely implemented in embedded computing applications. The AES algorithm used in software and hardware is symmetric so that encrypting/decrypting requires the same encryption key. Without the key, the encrypted data is inaccessible to ensure information security.

Notably in flash memory applications, AES 256-bit hardware encryption is the mainstream to protect sensitive or confidential data. The hardware encryption provides better performance, reliability, and security than software encryption. It uses a dedicated processor, which is built inside the controller, to process the encryption and decryption. This enormously shortens the processing time and makes it efficient.

7.4 End-to-End Data Protection

End-to-End Data Protection is a feature implemented in Apacer SSD products that extends error control to cover the entire path from the host computer to the drive and back, and that ensures data integrity at multiple points in the path to enable reliable delivery of data transfers. Unlike ECC which does not exhibit the ability to determine the occurrence of errors throughout the process of data transmission, End-to-End Data Protection allows SSD controller to identify an error created anywhere in the path and report the error to the host computer before it is written to the drive. This error-checking and error-reporting mechanism therefore guarantees the trustworthiness and reliability of the SSD.

8. Software Interface

8.1 Command Set

Table 8-1 summarizes the commands supported by PT910-µSSD.

Table 8-1 Admin Commands

Opcode	Command Description
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Features
0Ah	Get Features
0Ch	Asynchronous Event Request
10h	Firmware Activate
11h	Firmware Image Download

Table 8-2 Admin Commands – NVM Command Set Specific

Opcode	Command Description
80h	Format NVM

Table 8-3 NVM Commands

Opcode	Command Description
00h	Flush
01h	Write
02h	Read
09h	Dataset Management

8.2 S.M.A.R.T.

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

Table 8-4 SMART (02h)

Byte	Length	Description
0	1	Critical Warning
1-2	2	Composite Temperature (NAND Flash)
3	1	Available Spare
4	1	Available Spare Threshold
5	1	Percentage Used (Average Erase Count / P/E Cycle Count)
6-31	26	Reserved
32-47	16	Data Units Read
48-63	16	Data Units Written
64-79	16	Host Read Commands
80-95	16	Host Write Commands
96-111	16	Controller Busy Time
112-127	16	Power Cycles
128-143	16	Power On Hours
144-159	16	Unsafe Shutdowns
160-175	16	Media and Data Integrity Errors
176-191	16	Number of Error Information Log Entries
192-195	4	Warning Composite Temperature Time
196-199	4	Critical Composite Temperature Time
200-201	2	Temperature Sensor 1: Controller Temperature
204-205	2	Temperature Sensor 3: NAND Flash Temperature
206-207	2	Temperature Sensor 4
208-209	2	Temperature Sensor 5
210-211	2	Temperature Sensor 6
212-213	2	Temperature Sensor 7
214-215	2	Temperature Sensor 8
216-511	296	Reserved

Table 8-5 SMART (C0h)

Byte	Length	Description
0-255	256	Reserved
256-257	2	SSD Protect Mode
258-261	4	Host Read UNC Count
262-265	4	PHY Error Count
266-269	4	CRC Error Count
270-273	4	Total Early Bad Block Count
274-277	4	Total Later Bad Block Count
278-281	4	Max Erase Count
282-285	4	Average Erase Count
286-289	4	Program Fail Count
290-293	4	Erase Fail Count
294-301	8	Flash Write Sector
302-305	4	Total Spare Block
306-309	4	Current Spare Block
310-313	4	Read Retry Count
314-511	210	Reserved

9. Electrical Specifications

9.1 Operating Voltage

Table 9-1 lists the supply voltage for PT910-µSSD.

Table 9-1 Operating Range

Parameter	Voltage	Range
VCC	3.3V	3.135V ~ 3.465V
VCCQ	1.8V	1.71V ~ 1.89V
VDDI	1.2V	1.14V ~ 1.26V

9.2 Power Consumption

Table 9-2 lists the power consumption for PT910-µSSD.

Table 9-2 Power Consumption

Capacity / Mode	30 GB	60 GB	120 GB	480 GB
Active (mA)	240	325	510	570
Idle (mA)	140	140	145	145

Note:
*All values are typical and may vary depending on flash configurations or host system settings.
**Active power is an average power measurement performed using CrystalDiskMark with 128KB sequential read/write transfers.
***All values represent the total voltage measured using an evaluation board.

10. Physical Characteristics

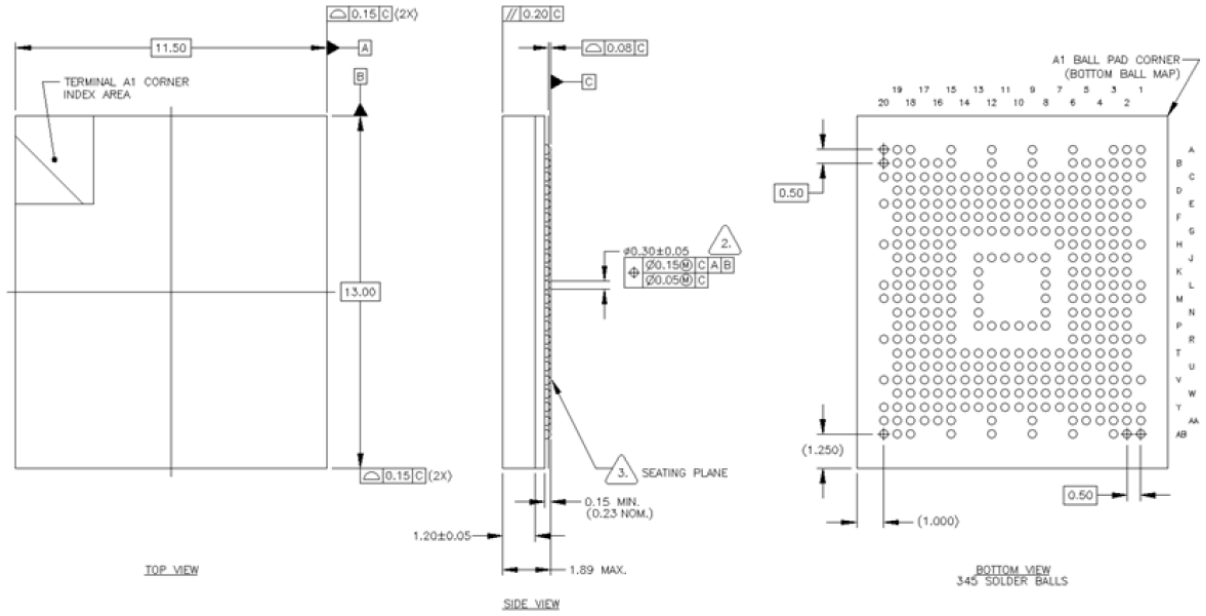

Figure 10-1 Dimensions

11. Product Ordering Information

11.1 Product Code Designations

Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	B	H	6	.	9	1	5	X	G	A	.	0	0	1	0	3

Code 1-3 (Product Line & Form Factor)	PT910-µSSD
Code 5-6 (Model/Solution)	PT910
Code 7-8 (Product Capacity)	5F: 30GB 5G: 60GB 5H: 120GB 5J: 240GB
Code 9 (Flash Type & Product Temp)	3D TLC Standard Temperature
Code 10 (Product Spec)	PCIe BGA SSD
Code 12-14 (Version Number)	Random numbers generated by system
Code 15-16 (Firmware Version)	Thermal Throttling + OP

11.2 Valid Combinations

Capacity	Part Number
30GB	BH6.915FGA.00103
60GB	BH6.915GGA.00103
120GB	BH6.915HGA.00103
240GB	BH6.915JGA.00103

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Revision History

Revision	Description	Date
1.0	Initial release	11/11/2020
1.1	- Added ball number to Form Factor on Specifications Overview page - Added “BGA 345” to the Ball Number header at Table 3-1 - Added a note regarding measuring method to 9.2 Power Consumption	8/3/2021

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