

RoHS Compliant PCI Express Flash Drive

PV130-CFX Product Specifications



December 20, 2018

Version 1.0



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Specifications Overview:

- **PCIe Interface**
 - Compliant with NVMe 1.3
 - Compatible with PCIe Gen3 x2 interface
- **Capacity**
 - 120, 240, 480 GB
- **Performance***
 - Interface burst read/write: 2 GB/sec
 - Sequential read: up to 1,655 MB/sec
 - Sequential write: up to 1,025 MB/sec
 - Random read (4K): up to 187,000 IOPS
 - Random write (4K): up to 170,000 IOPS
- **Flash Management**
 - Low-Density Parity-Check (LDPC) Code
 - Global Wear Leveling
 - Flash bad-block management
 - Flash Translation Layer: Page Mapping
 - S.M.A.R.T.
 - DataDefender
 - TRIM
 - Over-Provisioning
 - Hyper Cache Technology
- **NVMe Support Features**
 - HMB (Host Memory Buffer)**
- **Security**
 - End-to-End Data Protection
- **Reliability**
 - Thermal Management Technique
- **NAND Flash Type: 3D TLC**
- **Temperature Range**
 - Operating: 0°C to 70°C
 - Storage: -40°C to 100°C
- **Supply Voltage**
 - 3.3 V ± 5%
- **Power Consumption***
 - Active mode: 970 mA
 - Idle mode: 135 mA
- **Power Management**
 - Supports APST
 - Supports ASPM L1.2
- **Form Factor**
 - CFexpress Type B Card
 - Dimensions: 38.50 x 29.60 x 3.80, unit: mm
 - Net Weight: 8.5 g
- **Shock & Vibration*****
 - Shock: 1,500 G
 - Vibration: 15 G
- **RoHS Compliant**

*The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings.

**Windows 10 (version 1703) onwards supports the HMB (Host Memory Buffer) function.

***Non-operating

Table of Contents

1. General Descriptions	4
2. Functional Block	4
3. Pin Assignments.....	5
4. Product Specifications.....	7
4.1 Capacity.....	7
4.2 Performance	7
4.3 Environmental Specifications	7
4.4 Certification and Compliance.....	8
5. Flash Management	9
5.1 Error Correction/Detection.....	9
5.2 Bad Block Management	9
5.3 Global Wear Leveling	9
5.4 Flash Translation Layer – Page Mapping.....	9
5.5 DataDefender™	9
5.6 TRIM.....	10
5.7 Over-Provisioning	10
5.8 Hyper Cache Technology	10
6. NVMe Support Features	11
6.1 Host Memory Buffer.....	11
7. Security & Reliability Features	12
7.1 Thermal Management Technique	12
7.2 End-to-End Data Protection.....	12
8. Software Interface	13
8.1 Command Set.....	13
8.2 S.M.A.R.T.	14
9. Electrical Specifications	16
9.1 Operating Voltage.....	16
9.2 Power Consumption	16
10. Physical Characteristics.....	17

10.1 Dimensions	17
10.2 Net Weight	17

11. Product Ordering Information..... 18

11.1 Product Code Designations	18
11.2 Valid Combinations	19

1. General Descriptions

Apacer Industrial CFexpress PV130-CFX is the next generation Solid State Drive (SSD) with compact and removable storage to support larger, faster hosts deployed in a wide range of applications that require outstanding performance.

PV130-CFX provides full compliance with the latest PCIe Gen3 x2 (two-lanes) and NVMe Express interface specifications which allows the SSD to deliver exceptionally low latency and high performance, up to 1,655 MB/s read and 1,025 MB/s write. This new standard is designed for a variety of applications ranging from industrial, imaging, computing to enterprise markets.

2. Functional Block

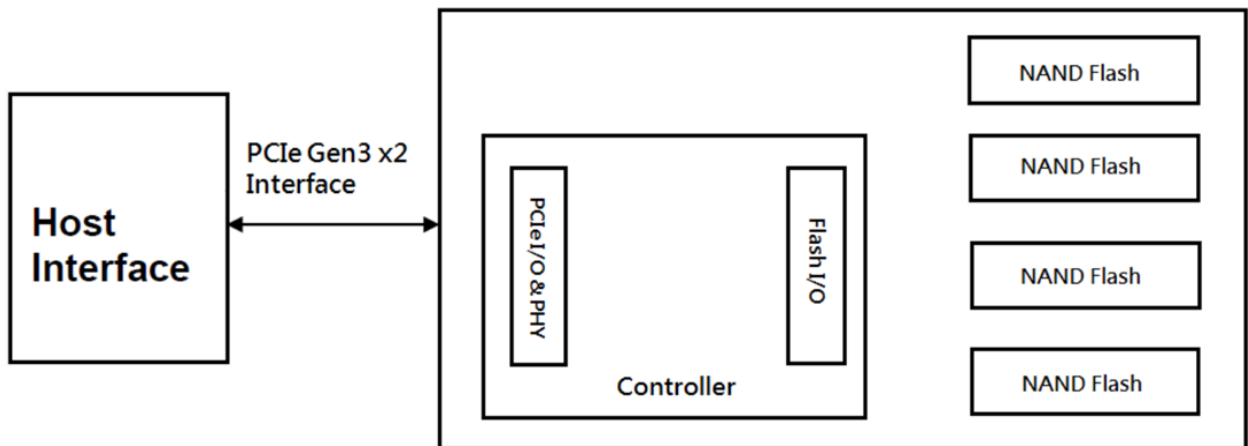


Figure 2-1 Functional Block Diagram

3. Pin Assignments

Table 3-1 lists the pin assignment of the media. The I/O column indicates the signal direction viewed from the media: “I” indicates the signal input to the media and “O” indicates the signal output from the media. In the Connection column, “R” indicates the signal is required, “Opt” indicates the signal is optional, and “NC” indicates the signal shall not be connected.

Table 3-1 Pin Assignments and Description

Pin No.	Signal	I/O	Media	Host	Notes
21	GND		R	R	
20	PETp0	I	R	R	
19	PETn0	I	R	R	
18	GND		R	R	
17	PERp0	O	R	R	
16	PERn0	O	R	R	
15	GND		R	R	
14	REFCLK+	I	R	R	
13	REFCLK-	I	R	R	
12	INS#	O	R	R	1
11	CLKREQ#	O	R	Opt	2
10	+3.3V		R	R	
9	PERST#	I	R	R	
8	Reserved		NC	NC	
7	Reserved		NC	NC	4
6	PETp1	I	Opt	Opt	
5	PETn1	I	Opt	Opt	
4	GND		R	Opt	3
3	PERp1	O	Opt	Opt	
2	PERn1	O	Opt	Opt	
1	GND		R	R	

1. A host pull-up resistor in the range of 100kΩ-200kΩ is required on this pin.

2. A host pull-up resistor (≥5kΩ) is required on this pin.

3. If the PCI Express Transmitter differential pair Lane 1 and Receiver differential pair Lane 1 are implemented, this pin shall be connected to ground.

4. Note that this pin is assigned to USBEN in XQD specification.

Table 3-2 Signal and Pin Assignments

Category	Signal Name	Description
PCI Express	PETp0	PCI Express 8 GT/s two Lane. 2 transmitter differential pairs and 2 receiver differential pairs.
	PETn0	
	PERp0	
	PERn0	
	PETp1	
	PETn1	
	PERp1	
	PERn1	
Auxiliary	REFCLK+	PCI Express differential (and spread-spectrum) reference clock.
	REFCLK-	
	PERST#	PCI Express functional reset.
	INS#	This signal is used for media detection and power control.
	CLKREQ#	This signal is used to indicate when REFCLK is needed for the PCI Express interface.
Power Source	+3.3V	3.3V power
Ground	GND	Round

4. Product Specifications

4.1 Capacity

Capacity specifications of PV130-CFX are available as shown in Table 4-1. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

Table 4-1 Capacity Specifications

Capacity	Total bytes*	Cylinders	Heads	Sectors	Max LBA
120 GB	120,033,640,448	16,383	16	63	234,441,648
240 GB	240,056,795,136	16,383	16	63	468,862,128
480 GB	480,103,104,512	16,383	16	63	937,703,088

*Display of total bytes varies from file systems, which means not all of the bytes can be used for storage.

**Notes: 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.

LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

4.2 Performance

Performance of PV130-CFX is listed below in Table 4-2.

Table 4-2 Performance Specifications

Performance	Capacity	120 GB	240 GB	480 GB
	Sequential Read* (MB/s)		1,470	1,600
Sequential Write* (MB/s)		500	945	1,025
Random Read IOPS** (4K)		89,000	152,000	187,000
Random Write IOPS** (4K)		102,000	160,000	170,000

Note:

Results may differ from various flash configurations or host system setting.

*Sequential performance is based on CrystalDiskMark 5.2.1 with file size 1,000MB.

**Random performance measured using IOMeter with Queue Depth 64.

4.3 Environmental Specifications

Environmental specifications of PV130-CFX are shown in Table 4-3.

Table 4-3 Environmental Specifications

Item	Specifications
Operating temp.	0°C to 70°C
Non-operating temp.	-40°C to 100°C
Operating vibration	7.69 GRMS, 20~2000 Hz/random (compliant with MIL-STD-810G)
Non-operating vibration	4.02 GRMS, 15~2000 Hz/random (compliant with MIL-STD-810G)
Operating shock	50(G), 11(ms), half-sine wave
Non-operating shock	1,500(G), 0.5(ms), half-sine wave

Note: Shock and Vibration specifications are subject to change without notice.

4.4 Certification and Compliance

PV130-CFX complies with the following standards:

- CE
- FCC
- RoHS

5. Flash Management

5.1 Error Correction/Detection

PV130-CFX implements a hardware ECC scheme, based on the Low Density Parity Check (LDPC). LDPC is a class of linear block error correcting code which has apparent coding gain over BCH code because LDPC code includes both hard decoding and soft decoding algorithms. With the error rate decreasing, LDPC can extend SSD endurance and increase data reliability while reading raw data inside a flash chip.

5.2 Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. Apacer implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

5.3 Global Wear Leveling

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Global wear leveling is an important mechanism that levels out the wearing of all blocks so that the wearing-down of all blocks can be almost evenly distributed. This will increase the lifespan of SSDs.

5.4 Flash Translation Layer – Page Mapping

Page mapping is an advanced flash management technology whose essence lies in the ability to gather data, distribute the data into flash pages automatically, and then schedule the data to be evenly written. Page-level mapping uses one page as the unit of mapping. The most important characteristic is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different sizes of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. Thus, page mapping is adopted to increase random access speed and improve SSD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

5.5 DataDefender™

Apacer DataDefender combines both firmware and hardware mechanisms to ensure data integrity. When power disruption occurs, the hardware mechanism will notice and trigger the controller to run multiple write-to-flash cycles to store data. Then the firmware will check that the data was correctly written to the NAND flash after the power disruption, preventing data loss.

5.6 TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks all the time.

5.7 Over-Provisioning

Over-Provisioning (OP) is a certain portion of the SSD capacity exclusively for increasing Garbage Collection (GC) efficiency, especially when the SSD is filled to full capacity or performs a heavy mixed-random workload. OP has the advantages of providing extended life expectancy, reliable data integrity, and high sustained write performance.

5.8 Hyper Cache Technology

Apacer proprietary Hyper Cache technology uses a portion of the available capacity as SLC (1bit-per-cell) NAND flash memory, called Hyper cache mode. When data is written to SSD, the firmware will direct the data to Hyper Cache mode, providing excellent performance to handle various scenarios in industrial use.

6. NVMe Support Features

6.1 Host Memory Buffer

Host Memory Buffer (HMB) allows HOST to allocate system memory for SSD's exclusive use in order to provide better performance and endurance, especially for DRAMless solutions.

7. Security & Reliability Features

7.1 Thermal Management Technique

Thermal management technique can monitor the temperature of the SSD equipped with a built-in thermal sensor via S.M.A.R.T. commands. This method can ensure the temperature of the device stays within temperature limits by drive throttling, i.e. reducing the speed of the drive when the device temperature reaches the threshold level, so as to prevent overheating, guarantee data reliability, and prolong product lifespan. When the temperature exceeds the maximum threshold level, thermal throttling will be triggered to reduce performance step by step to prevent hardware components from being damaged. Performance is only permitted to drop to the extent necessary for recovering a stable temperature to cool down the device's temperature. Once the temperature decreases to the minimum threshold value, transfer speeds will rise back to its optimum performance level.

7.2 End-to-End Data Protection

End-to-End Data Protection is a feature implemented in Apacer SSD products that extends error control to cover the entire path from the host computer to the drive and back, and that ensures data integrity at multiple points in the path to enable reliable delivery of data transfers. Unlike ECC which does not exhibit the ability to determine the occurrence of errors throughout the process of data transmission, End-to-End Data Protection allows SSD controller to identify an error created anywhere in the path and report the error to the host computer before it is written to the drive. This error-checking and error-reporting mechanism therefore guarantees the trustworthiness and reliability of the SSD.

8. Software Interface

8.1 Command Set

Table 8-1 summarizes the commands supported by PV130-CFX.

Table 8-1 Admin Commands

Opcode	Command Description
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Features
0Ah	Get Features
0Ch	Asynchronous Event Request
10h	Firmware Activate
11h	Firmware Image Download

Table 8-2 Admin Commands – NVM Command Set Specific

Opcode	Command Description
80h	Format NVM
81h	Security Send
82h	Security Receive

Table 8-3 NVM Commands

Opcode	Command Description
00h	Flush
01h	Write
02h	Read
04h	Write Uncorrectable
05h	Compare
08h	Write Zeroes
09h	Dataset Management

8.2 S.M.A.R.T.

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

Table 8-4 SMART (02h)

Byte	Length	Description
0	1	Critical Warning
1-2	2	Composite Temperature
3	1	Available Spare
4	1	Available Spare Threshold
5	1	Percentage Used
6-31	26	Reserved
32-47	16	Data Units Read
48-63	16	Data Units Written
64-79	16	Host Read Commands
80-95	16	Host Write Commands
96-111	16	Controller Busy Time
112-127	16	Power Cycles
128-143	16	Power On Hours
144-159	16	Unsafe Shutdowns
160-175	16	Media and Data Integrity Errors
176-191	16	Number of Error Information Log Entries
192-195	4	Warning Composite Temperature Time
196-199	4	Critical Composite Temperature Time
200-201	2	Temperature Sensor 1
202-203	2	Temperature Sensor 2
204-205	2	Temperature Sensor 3
206-207	2	Temperature Sensor 4
208-209	2	Temperature Sensor 5
210-211	2	Temperature Sensor 6
212-213	2	Temperature Sensor 7
214-215	2	Temperature Sensor 8
216-511	296	Reserved

Table 8-5 SMART (C0h)

Byte	Length	Description
2-3	2	SMART Version (0x3033)
4-7	4	P/E Cycle
8-9	2	Flash Type**
10-255	246	Reserved
256-257	2	SSD Protect Mode***
258-261	4	ECC Fail Count
262-265	4	PHY Error Count
266-269	4	CRC Error Count
274-277	4	Total Later Bad Block Count
278-281	4	Max Erase Count
282-285	4	Average Erase Count
286-289	4	Program Fail Count
290-293	4	Erase Fail Count
294-301	8	FlashWriteSector
302-511	210	Reserved

9. Electrical Specifications

9.1 Operating Voltage

Table 9-1 lists the supply voltage for PV130-CFX.

Table 9-1 Operating Range

Item	Range
Supply Voltage	3.3V ± 5%

9.2 Power Consumption

Table 9-2 lists the power consumption for PV130-CFX.

Table 9-2 Power Consumption

Mode \ Capacity	120 GB	240 GB	480 GB
Active (mA)	770	900	970
Idle (mA)	135	135	135

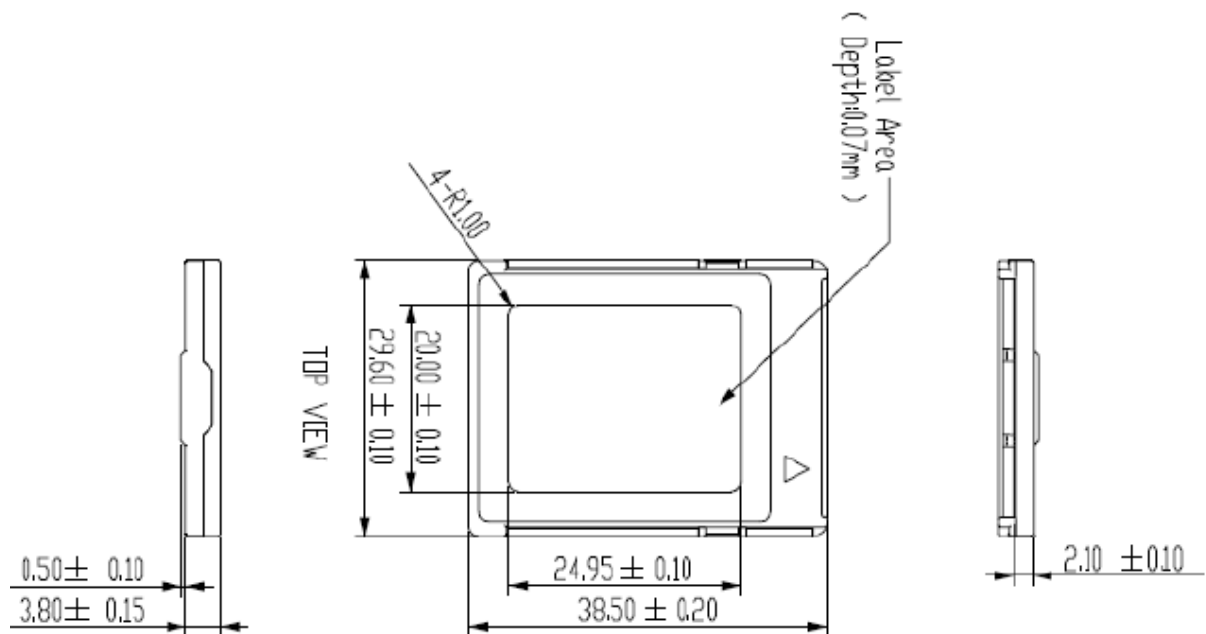
Note:

*All values are typical and may vary depending on flash configurations or host system settings.

**Active power is an average power measurement performed using CrystalDiskMark with 128KB sequential read/write transfers.

10. Physical Characteristics

10.1 Dimensions



Unit: mm

10.2 Net Weight

Capacity	Net Weight (g)
120GB	7.5
240GB	8.5
480GB	8.5

11. Product Ordering Information

11.1 Product Code Designations

Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	B	D	6	.	1	3	X	X	G	A	.	X	X	X	X	X

Code 1st~3th (Product Line & form factor)	PCIe CFexpress (CFX)
Code 5th~6th (Model/Solution)	PV130
Code 7th~8th (Product Capacity)	5H: 120GB 5J: 240GB 5K: 480GB
Code 9th (Flash Type & Product Temp)	G: 3D TLC C-grade
Code 10th (Product Spec)	CFexpress TypeB
Code 12th~14th (Version Number)	Random numbers generated by system
Code 15th~16th (Firmware Version)	01: Standard

11.2 Valid Combinations

Capacity	Part Number
120GB	BD6.135HGA.00101
240GB	BD6.135JGA.00101
480GB	BD6.135KGA.00101

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Revision History

Revision	Description	Date
0.1	Preliminary release	9/28/2018
1.0	<ul style="list-style-type: none">- Added 240-480GB support- Removed wide temperature support- Renamed Power Failure Management to DataDefender at Flash Management on Specifications Overview page and 5.5 section and updated the technology description- Removed thermal sensor support- Updated Performance and Power Consumption Specifications Overview page and 4.2 Performance and 9.2 Power Consumption- Updated 11. Product Ordering Information	12/20/2018

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