RoHS Compliant

ATA Disk Chip 3G

Product Specifications

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Version 1.1

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Features:

- **Standard ATA/IDE bus interface**
  - ATA command set compatible
  - ATA operating mode supports up to:
    PIO Mode-4
    Multiword DMA Mode-2
    Ultra DMA Mode-5
- **Connector type**
  - 32-pin male connector
- **Power consumption (typical)***
  - Supply voltage: 3.3V / 5V
  - Active: 175 mA
  - Idle: 7 mA
- **Performance***
  - Sustained read: Up to 50 MB/sec
  - Sustained write: Up to 40 MB/sec
- **Capacity**
  - 128, 256, 512 MB
    1, 2, 4, 8 GB
- **NAND Flash Type:** SLC
- **Temperature ranges**
  - Operating:
    Standard: 0℃ to 70℃ (32 ~ 158℉)
    Extended: -40℃ to 85℃ (-40° ~ 185℉)
  - Storage: -40℃ to 100℃ (-40° ~ 212℉)
- **Flash Management**
  - *Wear-leveling algorithms*
  - *Built-in Hardware ECC*, enabling up to 24 bit correction per 1024 bytes
  - *Flash Block Management*
  - Power Failure Management
  - S.M.A.R.T
  - ATA Secure Erase
- **Shock & Vibration****
  - Shock: 1,500 G
  - Vibration: 15 G
- **Dimensions:** 42.60 x 19.30 x 9.55, unit: mm
- **RoHS compliant**

*Varies from capacities. The values addressed here for performance and power consumption are typical and may vary depending on various settings and platforms.

**Non-operating

Table of Contents

1. General Description

Apacer's ATA-Disk Chip (ADC) is a reliable, embedded flash memory data storage system. This product is designed for embedded flash storage applications with expanded functionality and is a cost effective replacement for a conventional IDE hard disk drive. ADC supports standard ATA/IDE protocol with up to PIO Mode-4 and Multiword DMA Mode-2 interfaces and has a built-in micro-controller and file management firmware that communicates with ATA standard interfaces. ADC is designed to work at either 3.3 or 5 Volts and use a standard ATA driver that is part of all major operating systems such as Microsoft's Windows series.

Every ADC is packaged in a 600 mil 32-pin DIP package for easy and cost effective mounting to a system motherboard. In addition, every ADC offers users selectable Master/Slave operation through an external setting.

Featuring technologies as S.M.A.R.T, Wear-leveling algorithms, Built-In Hardware ECC, Power Failure Management, Flash Block Management, and ATA Secure Erase, Apacer's ADC assures users of a versatile device on data storage.

2. Functional Block

The ATA-Disk Chip (ADC) includes the ATA controller and flash media, as well as the ATA standard interface. Figure 2-1 shows the functional block diagram.

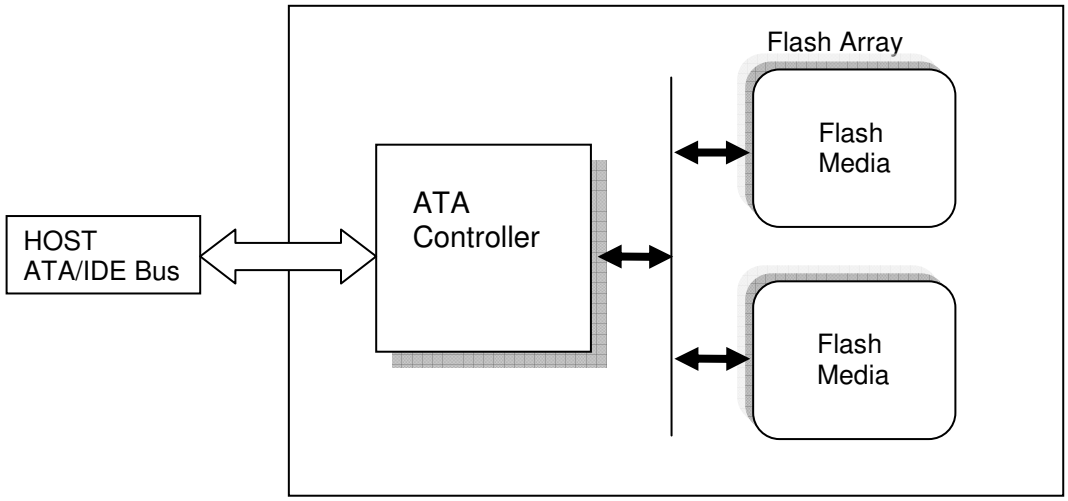


FIGURE 2-1: FUNCTIONAL BLOCK DIAGRAM

3. Electrical Interface

3.1 Pin Assignment

The ADC functions in ATA mode, which is compatible with IDE hard disk drive. The signal/pin assignments are listed in Tables 3-1. Active low signals have a "#" suffix. Pin types are Input, Output or Input/Output.

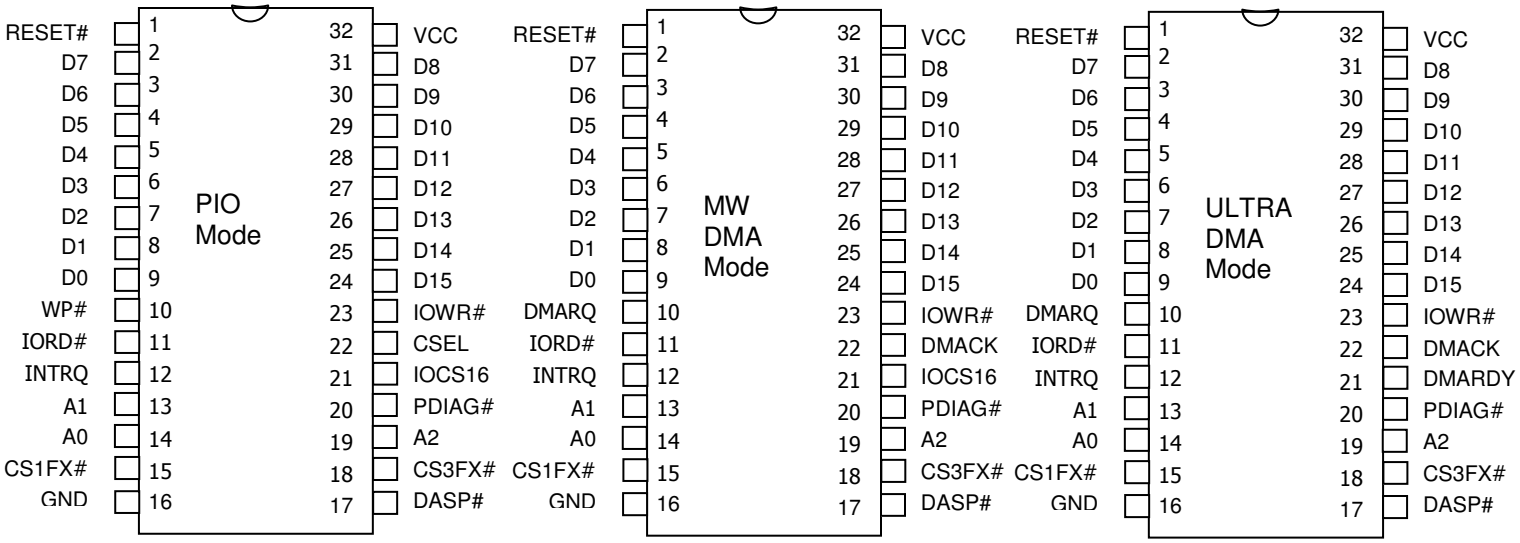


FIGURE 3-1: PIN ASSIGNMENT FOR 32-PIN PSDIP

TABLE 3-1: 32-PIN PIN ASSIGNMENT

Pin No.	Signal Name	Pin Type	I/O Type[1]	Pin No.	Signal Name	Pin Type	I/O Type[1]
1	RESET#	I	I2U	32	VDD	-	Power
2	D7	I/O	I1Z, O2	31	D8	I/O	I1Z, O2
3	D6	I/O	I1Z, O2	30	D9	I/O	I1Z, O2
4	D5	I/O	I1Z, O2	29	D10	I/O	I1Z, O2
5	D4	I/O	I1Z, O2	28	D11	I/O	I1Z, O2
6	D3	I/O	I1Z, O2	27	D12	I/O	I1Z, O2
7	D2	I/O	I1Z, O2	26	D13	I/O	I1Z, O2
8	D1	I/O	I1Z, O2	25	D14	I/O	I1Z, O2
9	D0	I/O	I1Z, O2	24	D15	I/O	I1Z, O2
10	WP#/DMARQ	O/I	O1/ I2U-	23	IOWR#	I	I2Z
11	IORD#	I	I2Z	22	CSEL/DMACK	I	I2U-
12	INTRQ	O	O1	21	IOCS16#/DMARDY	O	O2, O1
13	A1	I	I1Z	20	PDIAG#	I/O	I1U, O1
14	A0	I	I1Z	19	A2	I	I1Z
15	CS1FX#	I	I2Z	18	CS3FX#	I	I2Z
16	GND	-	Ground	17	DASP#	I/O	I1U, O6

4. Product Specifications

4.1 Capacity

TABLE 4-1: Capacity Specifications

Capacity	Total bytes	Cylinders	Heads	Sectors	Max LBA
128 MB	128,057,344	977	8	32	250,122
256 MB	256,901,120	980	16	32	501,760
512 MB	512,483,328	993	16	63	1,000,944
1 GB	1,024,966,656	1986	16	63	2,001,888
2 GB	2,048,385,024	3969	16	63	4,000,752
4 GB	4,096,253,952	7937	16	63	8,000,496
8 GB	8,001,552,384	15504	16	63	15,628,032

*Display of total bytes varies from file systems. LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the ADC is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

4.2 Performance

TABLE 4-2: Performance

Capacity / Performance	128 MB	256 MB	512 MB	1 GB	2 GB	4 GB	8 GB
Sustained read (MB/s)	24	24	23	28	29	47	50
Sustained write (MB/s)	6	11	10	14	20	31	40

*Performance varies with flash configurations or host system settings.

4.3 Environmental Specification

Environmental specification of the ATA-Disk Chip (ADC) product family follows the MIL-STD-810F standard which is shown in Table 4-3.

TABLE 4-3: Environmental Specifications

Environment		Specification
Temperature	Operating	0℃ to 70℃; -40℃ to 85℃ (Extended Temperature)
	Storage	-40℃ to 100℃
Vibration (Non-Operating)		Sine wave: 10~2000Hz, 15G (X, Y, Z 3-axis)
Shock (Non-Operating)		Half sine wave, 1500G, 0.5msec (X, Y, Z ; All 6-axis)

5. Flash Management

5.1. Advanced wear-leveling algorithms

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Wear leveling is an important mechanism that level out the wearing of blocks so that the wearing-down of blocks can be almost evenly distributed. This will increase the lifespan of SSDs. Commonly used wear leveling types are Static and Dynamic.

5.2 Built-in hardware ECC

The ATA-Disk Chip uses BCH Error Correction Code (ECC) algorithms which correct up to 24 random bits errors for each 1024 byte block of data. High performance is fulfilled through hardware-based error detection and correction.

5.3 Flash block management

Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. When host performs program/erase command on a block, bad block may appear in Status Register. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, block mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

5.5 Power Failure Management

Power Failure Management plays a crucial role when experiencing unstable power supply. Power disruption may occur when users are storing data into the SSD. In this urgent situation, the controller would run multiple write-to-flash cycles to store the metadata for later block rebuilding. This urgent operation requires about several milliseconds to get it done. At the next power up, the firmware will perform a status tracking to retrieve the mapping table and resume previously programmed NAND blocks to check if there is any incompleteness of transmission.

5.6 ATA Security Erase

ATA Secure Erase is an ATA disk purging command currently embedded in most of the storage drives. Defined in ATA specifications, (ATA) Secure Erase is part of Security Feature Set that allows storage drives to erase all user data areas. The erase process usually runs on the firmware level as most of the ATA-based storage media currently in the market are built-in with this command. ATA Secure Erase can securely wipe out the user data in the drive and protects it from malicious attack.

6. Software Interface

6.1 Command Set

This section defines the software requirements and the format of the commands the host sends to the ATA-Disk Chip. Commands are issued to ADC by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command register. The manner in which a command is accepted varies.

TABLE 6-1: COMMAND SET (1 OF 2)

Command	Code	Command Protocol
Check-Power-Mode	E5H or 98H	Non-data
Erase-Sector(s)	C0H	Non-data
Execute-Drive-Diagnostic	90H	Device Diagnostic
Flush-Cache	E7H	Non-data
Format-Track	50H	PIO data-out
Identify-Drive	ECH	PIO data-in
Idle	E3H or 97H	Non-data
Idle-Immediate	E1H or 95H	Non-data
Initialize-Drive-Parameters	91H	Non-data
NOP	00H	Non-data
Read DMA	C8H	DMA
Read-Buffer	E4H	PIO data-in
Read-Multiple	C4H	PIO data-in
Read-Sector(s)	20H or 21H	PIO data-in
Read-Verify-Sector(s)	40H or 41H	Non-data
Recalibrate	1XH	Non-data
Request Sense	03H	Non-data
Security Disable Password	F6H	PIO data-out
Security Erase Prepare	F3H	Non-data
Security Erase Unit	F4H	PIO data-out
Security Freeze Lock	F5H	Non-data
Security Set Password	F1H	PIO data-out
Security Unlock	F2H	PIO data-out
Seek	7XH	Non-data

TABLE 6-1: COMMAND SET (2 OF 2)

Command	Code	Command Protocol
Set-Features	EFH	Non-data
SMART	B0H	Non-data / PIO data-out
Set-Multiple-mode	C6H	Non-data
Sleep	E6H or 99H	Non-data
Standby	E2H or 96H	Non-data
Standby-Immediate	E0H or 94H	Non-data
Translate-Sector	87H	PIO data-in
Write Buffer	E8H	PIO data-out
Write DMA	CAH	DMA
Write Multiple	C5H	PIO data-out
Write-Multiple-Without-Erase	CDH	PIO data-out
Write Sector(s)	30H or 31H	PIO data
Write-Sector(s)-Without-Erase	38H	PIO data-out
Write Verify	3CH	PIO data
Wear Level	F5H	Non-data

6.2 S.M.A.R.T

S.M.A.R.T. is an acronym for Self-Monitoring, Analysis and Reporting Technology, an open standard allowing disk drives to automatically monitor their own health and report potential problems. It protects the user from unscheduled downtime by monitoring and storing critical drive performance and calibration parameters. Ideally, this should allow taking proactive actions to prevent impending drive failure. Apacer SMART feature adopts the standard SMART command B0h to read data from the drive. When the Apacer SMART Utility running on the host, it analyzes and reports the disk status to the host before the device is in critical condition.

7. Electrical Specification

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Table 7-1: Operating range

Standard Operating Temperature	0℃ to +70℃
Extended Operating Temperature	-40℃ to +85℃
Supply voltage	5V± 5% (4.75-5.25V)
	3.3V ± 5% (3.135-3.465V)

TABLE 7-2 ABSOLUTE MAXIMUM POWER PIN STRESS RATINGS

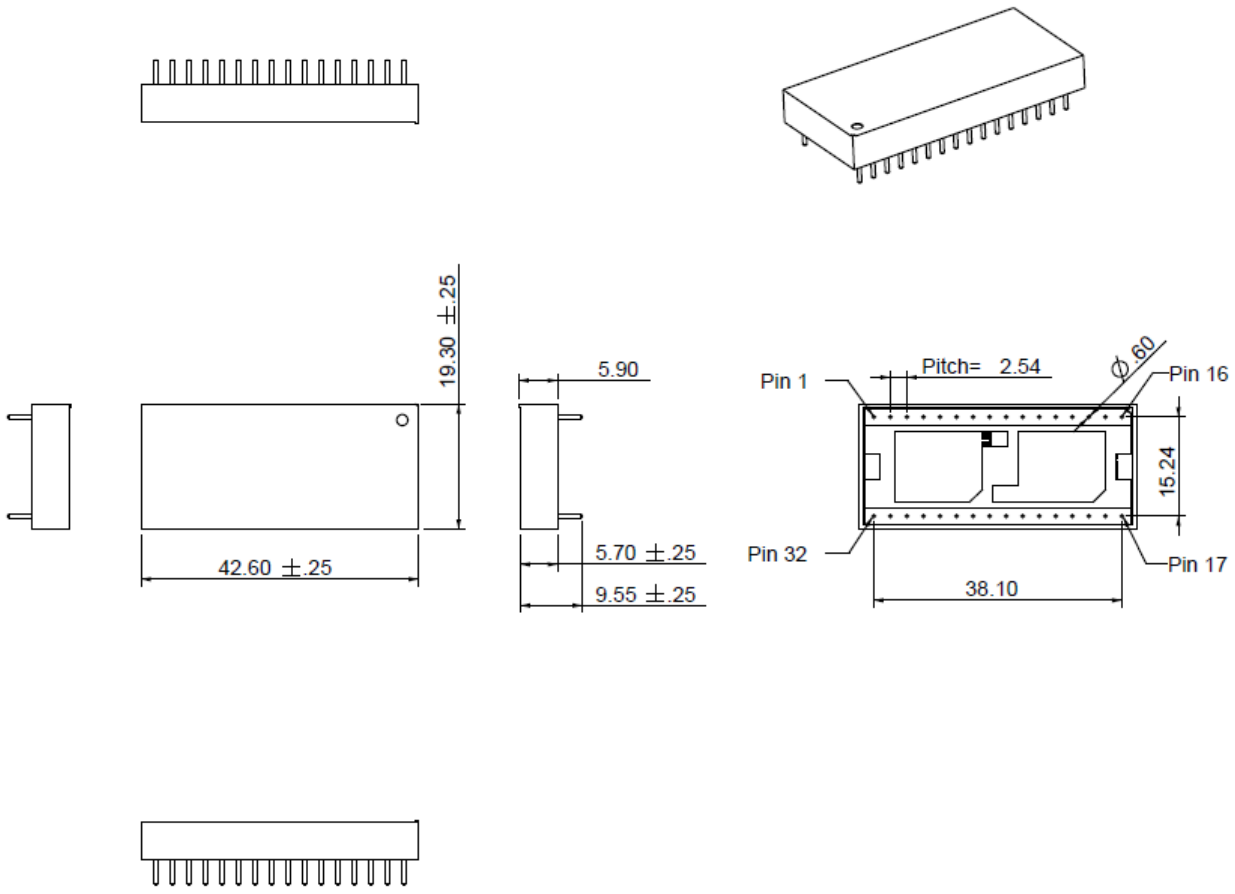
Parameter	Symbol	Conditions
Power Supply	V_{DD}	6V to -0.5V
Input pin voltage	V	5.5v to -0.3V

TABLE 7-3: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Maximum	Units
$T_{PU-READY}$[1]	Power-up to Ready Operation	1000	ms
$T_{PU-WRITE}$[1]	Power-up to Write Operation	500	ms

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

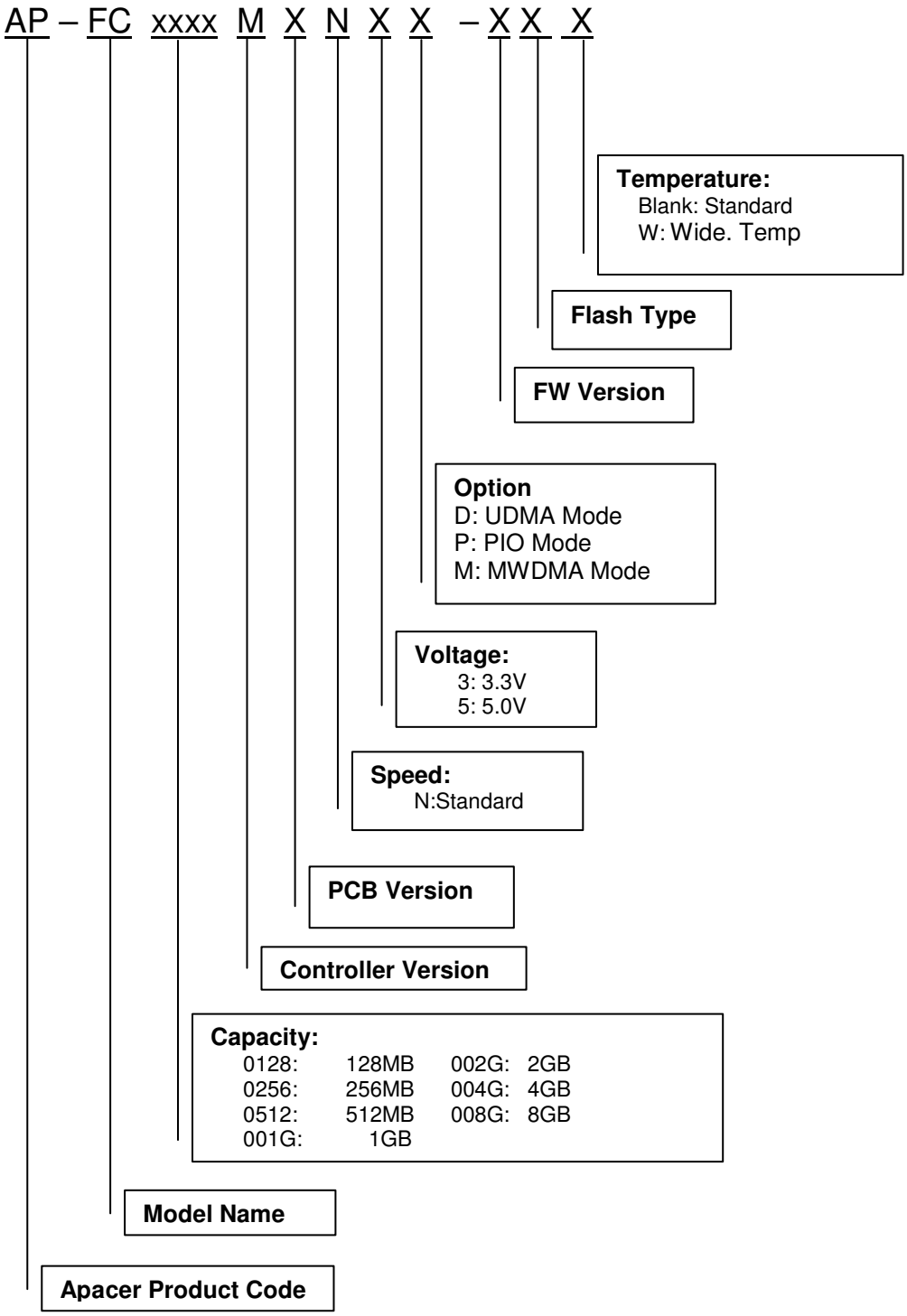
8. Physical Characteristics



Unit: mm
Tolerance: ± 0.2

9. Product Ordering Information

9.1 Product Code Designations



9.2 Valid Combinations

9.2.1 UDMA Mode

Capacity	P/N (3.3V)	P/N (5V)
128MB	AP-FC0128M0N3D-2T	AP-FC0128M0N5D-2T
256MB	AP-FC0256M0N3D-2T	AP-FC0256M0N5D-2T
512MB	AP-FC0512M0N3D-2T	AP-FC0512M0N5D-2T
1GB	AP-FC001GM0N3D-2T	AP-FC001GM0N5D-2T
2GB	AP-FC002GM0N3D-2T	AP-FC002GM0N5D-2T
4GB	AP-FC004GM0N3D-2T	AP-FC004GM0N5D-2T
8GB	AP-FC008GM0N3D-2T	AP-FC008GM0N5D-2T

9.2.2 PIO Mode

Capacity	P/N (3.3V)	P/N (5V)
128MB	AP-FC0128M0N3P-2T	AP-FC0128M0N5P-2T
256MB	AP-FC0256M0N3P-2T	AP-FC0256M0N5P-2T
512MB	AP-FC0512M0N3P-2T	AP-FC0512M0N5P-2T
1GB	AP-FC001GM0N3P-2T	AP-FC001GM0N5P-2T
2GB	AP-FC002GM0N3P-2T	AP-FC002GM0N5P-2T
4GB	AP-FC004GM0N3P-2T	AP-FC004GM0N5P-2T
8GB	AP-FC008GM0N3P-2T	AP-FC008GM0N5P-2T

9.2.3 MWDMA Mode

Capacity	P/N (3.3V)	P/N (5V)
128MB	AP-FC0128M0N3M-2T	AP-FC0128M0N5M-2T
256MB	AP-FC0256M0N3M-2T	AP-FC0256M0N5M-2T
512MB	AP-FC0512M0N3M-2T	AP-FC0512M0N5M-2T
1GB	AP-FC001GM0N3M-2T	AP-FC001GM0N5M-2T
2GB	AP-FC002GM0N3M-2T	AP-FC002GM0N5M-2T
4GB	AP-FC004GM0N3M-2T	AP-FC004GM0N5M-2T
8GB	AP-FC008GM0N3M-2T	AP-FC008GM0N5M-2T

9.2.4 Ext. Temp UDMA Mode

Capacity	P/N (3.3V)	P/N (5V)
128MB	AP-FC0128M0N3D-2TW	AP-FC0128M0N5D-2TW
256MB	AP-FC0256M0N3D-2TW	AP-FC0256M0N5D-2TW
512MB	AP-FC0512M0N3D-2TW	AP-FC0512M0N5D-2TW
1GB	AP-FC001GM0N3D-2TW	AP-FC001GM0N5D-2TW
2GB	AP-FC002GM0N3D-2TW	AP-FC002GM0N5D-2TW
4GB	AP-FC004GM0N3D-2TW	AP-FC004GM0N5D-2TW
8GB	AP-FC008GM0N3D-2TW	AP-FC008GM0N5D-2TW

9.2.5 Ext. Temp PIO Mode

Capacity	P/N (3.3V)	P/N (5V)
128MB	AP-FC0128M0N3P-2TW	AP-FC0128M0N5P-2TW
256MB	AP-FC0256M0N3P-2TW	AP-FC0256M0N5P-2TW
512MB	AP-FC0512M0N3P-2TW	AP-FC0512M0N5P-2TW
1GB	AP-FC001GM0N3P-2TW	AP-FC001GM0N5P-2TW
2GB	AP-FC002GM0N3P-2TW	AP-FC002GM0N5P-2TW
4GB	AP-FC004GM0N3P-2TW	AP-FC004GM0N5P-2TW
8GB	AP-FC008GM0N3P-2TW	AP-FC008GM0N5P-2TW

9.2.6 Ext. Temp MWDMA Mode

Capacity	P/N (3.3V)	P/N (5V)
128MB	AP-FC0128M0N3M-2TW	AP-FC0128M0N5M-2TW
256MB	AP-FC0256M0N3M-2TW	AP-FC0256M0N5M-2TW
512MB	AP-FC0512M0N3M-2TW	AP-FC0512M0N5M-2TW
1GB	AP-FC001GM0N3M-2TW	AP-FC001GM0N5M-2TW
2GB	AP-FC002GM0N3M-2TW	AP-FC002GM0N5M-2TW
4GB	AP-FC004GM0N3M-2TW	AP-FC004GM0N5M-2TW
8GB	AP-FC008GM0N3M-2TW	AP-FC008GM0N5M-2TW

Revision History

Revision	Date	Description	Remark
1.0	04/26/2012	Official release	
1.1	10/03/2013	Updated performance due to change in flash configurations	

Global Presence

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