Apacer

RoHS Compliant

ATA Disk Chip 4

Product Specifications

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Version 1.2

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Specifications Overview:

- **Standard ATA/IDE bus interface**
  - ATA command set compatible
  - ATA operating mode supports up to:
    - PIO Mode-4
    - Multiword DMA Mode-2
    - Ultra DMA Mode-5
- **Capacity**
  - 128, 256, 512 MB
  - 1, 2, 4, 8, 16 GB
- **Performance***
  - Sequential read: Up to 41 MB/sec
  - Sequential write: Up to 35 MB/sec
- **Flash Management**
  - Built-in hardware ECC
  - Global Wear Leveling
  - Enhanced Data Integrity
  - Intelligent power failure recovery
  - S.M.A.R.T.
  - ATA Secure Erase
- **NAND Flash Type:** SLC
- **Temperature Range**
  - Operating:
    - Standard: 0°C to 70°C
    - Wide: -40°C to 85°C
  - Storage: -40°C to 100°C
- **Supply Voltage**
  - 3.3 V
  - 5V
- **Power Consumption***
  - Active mode: 170 mA
  - Idle mode: 3 mA
- **Connector Type**
  - 32-pin male connector
- **RoHS Compliant**

*Varies from capacities. The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings. The term idle refers to the standby state of the device.

Table of Contents

1. General Descriptions

Apacer's ATA-Disk Chip (ADC) is a high performance, embedded flash memory data storage system. This product is designed for embedded flash storage applications with expanded functionality and is a cost effective replacement for a conventional IDE hard disk drive. ADC supports standard ATA/IDE protocol with up to PIO Mode-4 and Multiword DMA Mode-2 interfaces and has a built-in micro-controller and file management firmware that communicates with ATA standard interfaces; therefore, ADC does not require additional or proprietary host software such as Flash File System (FFS) and Memory Technology Driver (MTD) software. ADC is designed to use a standard ATA driver that is part of all major operating systems such as Microsoft's Windows series.

Every ADC is packaged in a 600 mil 32-pin DIP package for easy and cost effective mounting to a system motherboard. In addition, every ADC offers users selectable Master/Slave operation through an external setting.

Featuring technologies as S.M.A.R.T, Global Wear-leveling algorithms, Built-In Hardware ECC, Enhanced Data Integrity, Intelligent Power Failure Recovery, and ATA Secure Erase, Apacer's ADC assures users of a versatile device on data storage.

1.1 Performance-optimized ATA Chip

The kernel of an ATA-Disk Chip is the ATA controller, which translates standard ATA signals into the data and controls of the flash media. This proprietary ATA controller is specifically designed to attain high data throughput from the host to the flash.

1.1.1 SRAM Buffer

The ATA-Disk Chip Controller performs as an SRAM buffer to optimize the host's data transfer to and from the flash media.

1.1.2 Power Management Unit (PMU)

The power management unit (PMU) controls the power consumption of the ATA-Disk Chip. It reduces the power consumption of the ATA-Disk Chip Controller by putting circuitry not in operation into sleep mode. The PMU has zero wake-up latency.

2. Functional Block

The ATA-Disk Chip (ADC) includes the ATA controller and flash media, as well as the ATA standard interface. Figure 2-1 shows the functional block diagram.

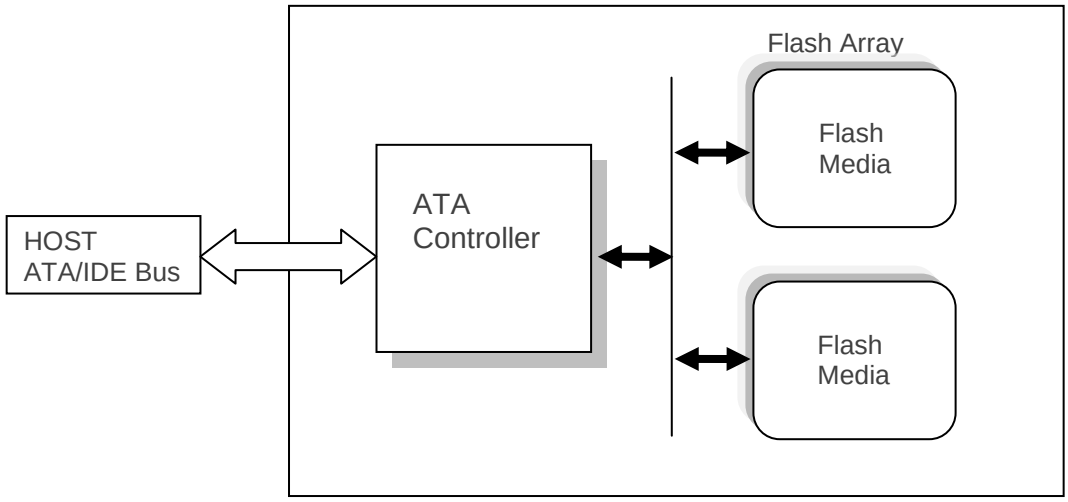


Figure 2-1 Functional Block Diagram

3. Electrical Interface

3.1 Pin Assignment

The ADC functions in ATA mode, which is compatible with IDE hard disk drive. The signal/pin assignments are listed in Tables 3-1. Active low signals have a "#" suffix. Pin types are Input, Output or Input/Output.

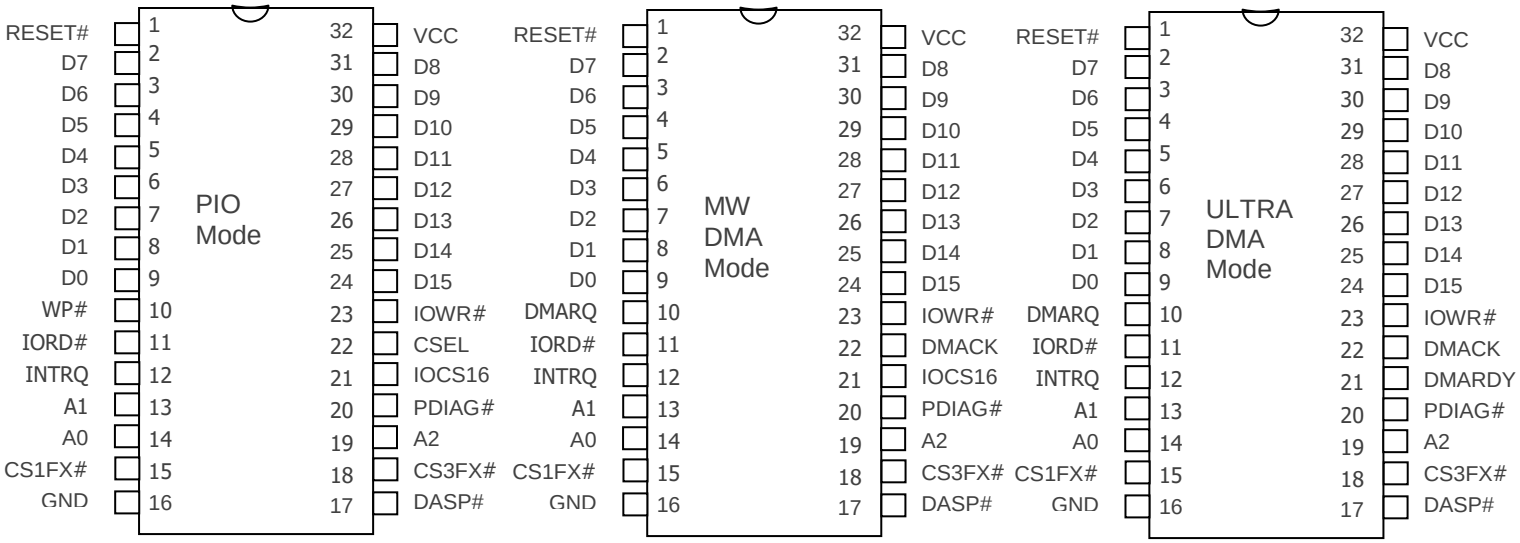


Figure 3-1 Pin Assignment for 32-Pin PSDIP

Table 3-1 Pin Assignment

Pin No.	Signal Name	Pin Type	I/O Type	Pin No.	Signal Name	Pin Type	I/O Type
1	RESET#	I	I2U	32	VDD	-	Power
2	D7	I/O	I1Z, O2	31	D8	I/O	I1Z, O2
3	D6	I/O	I1Z, O2	30	D9	I/O	I1Z, O2
4	D5	I/O	I1Z, O2	29	D10	I/O	I1Z, O2
5	D4	I/O	I1Z, O2	28	D11	I/O	I1Z, O2
6	D3	I/O	I1Z, O2	27	D12	I/O	I1Z, O2
7	D2	I/O	I1Z, O2	26	D13	I/O	I1Z, O2
8	D1	I/O	I1Z, O2	25	D14	I/O	I1Z, O2
9	D0	I/O	I1Z, O2	24	D15	I/O	I1Z, O2
10	WP#/DMARQ	O/I	O1/ I2U-	23	IOWR#	I	I2Z
11	IORD#	I	I2Z	22	CSEL/DMACK	I	I2U-
12	INTRQ	O	O1	21	IOCS16#/DMARDY	O	O2, O1
13	A1	I	I1Z	20	PDIAG#	I/O	I1U, O1
14	A0	I	I1Z	19	A2	I	I1Z
15	CS1FX#	I	I2Z	18	CS3FX#	I	I2Z
16	GND	-	Ground	17	DASP#	I/O	I1U, O6

4. Product Specifications

4.1 Capacity

Capacity specification of ATA-Disk Chip (ADC) product family is available as shown in Table 4-1 which lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

Table 4-1 Capacity Specifications

Capacity	Total bytes*	Cylinders	Heads	Sectors	Max LBA
128 MB	128,057,344	977	8	32	250,112
256 MB	256,901,120	980	16	32	501,760
512 MB	512,483,328	993	16	63	1,000,944
1 GB	1,024,966,656	1986	16	63	2,001,888
2 GB	2,048,385,024	3969	16	63	4,000,752
4 GB	4,096,253,952	7937	16	63	8,000,496
8 GB	8,001,552,384	15504	16	63	15,628,032

4.2 Performance

Performances of the ATA-Disk Chip are listed in Table 4-2.

Table 4-2 Performance Specifications

Capacity / Performance	128 MB	256 MB	512 MB	1 GB	2 GB	4 GB	8 GB	16 GB
Sequential Read* (MB/s)	24	24	32	31	35	38	41	41
Sequential Write* (MB/s)	11	11	23	22	26	33	35	35

Note:
Results may differ from various flash configurations or host system setting.
*Sequential performance is based on CrystalDiskMark 5.2.1 with file size 1,000MB.

4.3 Environmental Specifications

Environmental specifications of the ATA-Disk Chip (ADC) product family are shown in Table 4-3.

Table 4-3 Environmental Specifications

Environment	Specifications
Temperature	0°C to 70°C (Standard); -40°C to 85°C (Wide)
	-40°C to 100°C (Non-operating)
Humidity	5% to 95% RH (Non-condensing)
Vibration (Non-Operation)	Sine wave: 10~2000Hz, 15G (X, Y, Z axes)
Shock (Non-Operation)	Half sine wave, Peak acceleration 50 G, 11 ms (X, Y, Z ; All 6 axes)

5. Flash Management

5.1 Error Correction/Detection

The ATA-Disk Chip uses BCH Error Correction Code (ECC) algorithms which correct up to 24 random bits errors for each 1024 byte block of data. High performance is fulfilled through hardware-based error detection and correction.

5.2 Global Wear Leveling

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Global wear leveling is an important mechanism that levels out the wearing of all blocks so that the wearing-down of all blocks can be almost evenly distributed. This will increase the lifespan of SSDs.

5.3 Enhanced Data Integrity

The properties of NAND flash memory make it ideal for applications that require high integrity while operating in challenging environments. The integrity of data to NAND flash memory is generally maintained through ECC algorithms and bad block management. Flash controllers can support ECC capability for accuracy of data transactions, and bad block management is a preventive mechanism from loss of data by retiring unusable media blocks and relocating the data to the other blocks, along with the integration of global wear leveling algorithms, so that the lifespan of device can be expanded.

5.4 Intelligent Power Failure Recovery

The Low Power Detection on the controller initiates cached data saving before the power supply to the device is too low. This feature prevents the device from crash and ensures data integrity during an unexpected blackout. Once power was failure before cached data writing back into flash, data in the cache will lost. The next time the power is on, the controller will check these fragmented data segment, and, if necessary, replace them with old data kept in flash until programmed successfully.

5.5 ATA Secure Erase

Accomplished by the Secure Erase (SE) command, which added to the open ANSI standards that control disk drives, “ATA Secure Erase” is built into the disk drive itself and thus far less susceptible to malicious software attacks than external software utilities. It is a positive easy-to-use data destroy command, amounting to electronic data shredding. Executing the command causes a drive to internally completely erase all possible user data. This command is carried out within disk drives, so no additional software is required. Once executed, neither data nor the erase counter on the device would be recoverable, which blurs the accuracy of device lifespan. The process to erase will not be stopped until finished while encountering power failure, and will be continued when power is back on.

6. Software Interface

6.1 Command Set

This section defines the software requirements and the format of the commands the host sends to the ATA-Disk Chip. Commands are issued to ADC by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command register. The manner in which a command is accepted varies.

Table 6-1 Command Set

Code	Command	Command Protocol
E5H or 98H	CHECK-POWER-MODE	Non-data
C0H	ERASE-SECTOR(S)	Non-data
90H	EXECUTE-DRIVE-DIAGNOSTIC	Device Diagnostic
E7H	FLUSH-CACHE	Non-data
50H	FORMAT-TRACK	PIO data-out
ECH	IDENTIFY-DRIVE	PIO data-in
E3H or 97H	IDLE	Non-data
E1H or 95H	IDLE-IMMEDIATE	Non-data
91H	INITIALIZE-DRIVE-PARAMETERS	Non-data
00H	NOP	Non-data
C8H	READ DMA	DMA
E4H	READ-BUFFER	PIO data-in
C4H	READ-MULTIPLE	PIO data-in
20H or 21H	READ-SECTOR(S)	PIO data-in
40H or 41H	READ-VERIFY-SECTOR(S)	Non-data
1XH	RECALIBRATE	Non-data
03H	REQUEST SENSE	Non-data
F6H	SECURITY DISABLE PASSWORD	PIO data-out
F3H	SECURITY ERASE PREPARE	Non-data
F4H	SECURITY ERASE UNIT	PIO data-out
F5H	SECURITY FREEZE LOCK	Non-data
F1H	SECURITY SET PASSWORD	PIO data-out
F2H	SECURITY UNLOCK	PIO data-out
7XH	SEEK	Non-data
EFH	SET-FEATURES	Non-data
B0H	SMART	Non-data / PIO data-out
C6H	SET-MULTIPLE-MODE	Non-data
E6H or 99H	SLEEP	Non-data
E2H or 96H	STANDBY	Non-data
E0H or 94H	STANDBY-IMMEDIATE	Non-data
87H	TRANSLATE-SECTOR	PIO data-in

Code	Command	Command Protocol
E8H	WRITE BUFFER	PIO data-out
CAH	WRITE DMA	DMA
C5H	WRITE MULTIPLE	PIO data-out
CDH	WRITE-MULTIPLE-WITHOUT-ERASE	PIO data-out
30H or 31H	WRITE SECTOR(S)	PIO data
38H	WRITE-SECTOR(S)-WITHOUT-ERASE	PIO data-out
3CH	WRITE VERIFY	PIO data
F5H	WEAR LEVEL	Non-data

6.2 S.M.A.R.T.

S.M.A.R.T. (SMART), an acronym stands for Self-Monitoring, Analysis and Reporting Technology, is an open standard allowing an individual disk drive in the ATA/IDE or SCSI interface to automatically monitor its own health and report potential problems in order to prevent data loss. This failure warning technology provides predictions from unscheduled downtime by observing and storing critical drive performance and calibration parameters. Ideally, this should allow taking hands-on actions to keep from impending drive failure.

Failures are divided into two categories: those that can be predicted and those that cannot. Predictable failures occur gradually over time, and the decline in performance can be detected; on the other hand, unpredictable failures happen very sudden without any warning. These failures may be caused by power surges or related to electronic components. The purpose of the SMART implementation is to predict near-term failures of each individual disk drive and generate a warning to prevent unfortunate loss.

Apacer's S.M.A.R.T. features comply with ATA/ATAPI-7 specification by using the standard SMART command to read data from the flash drive. Running on the host, Apacer's SMART utility analyzes and reports the disk status periodically to the host before the drive is in critical condition as well as allows taking hands-on actions to keep from failures. Together with Apacer's wear-leveling and ECC schemes, S.M.A.R.T. will ensure a level of data reliability and integrity that has never been achieved before.

7. Electrical Specifications

Caution: **Absolute Maximum Stress Ratings –** Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.

Table 7-1 Operating Range

Item	3.3V	5V
Supply Voltage	2.97-3.63V	4.5-5.5V

Table 7-2 Absolute Maximum Power PIN Stress Ratings

Parameter	Symbol	Conditions
Power Supply	V_{DD}	6V to -0.5V
Input pin voltage	V	5.5v to -0.3V

Table 7-3 Recommended System Power-up Timings

Symbol	Parameter	Maximum	Unit
$T_{PU-READY}$[1]	Power-up to Ready Operation	1000	ms
$T_{PU-WRITE}$[1]	Power-up to Write Operation	500	ms

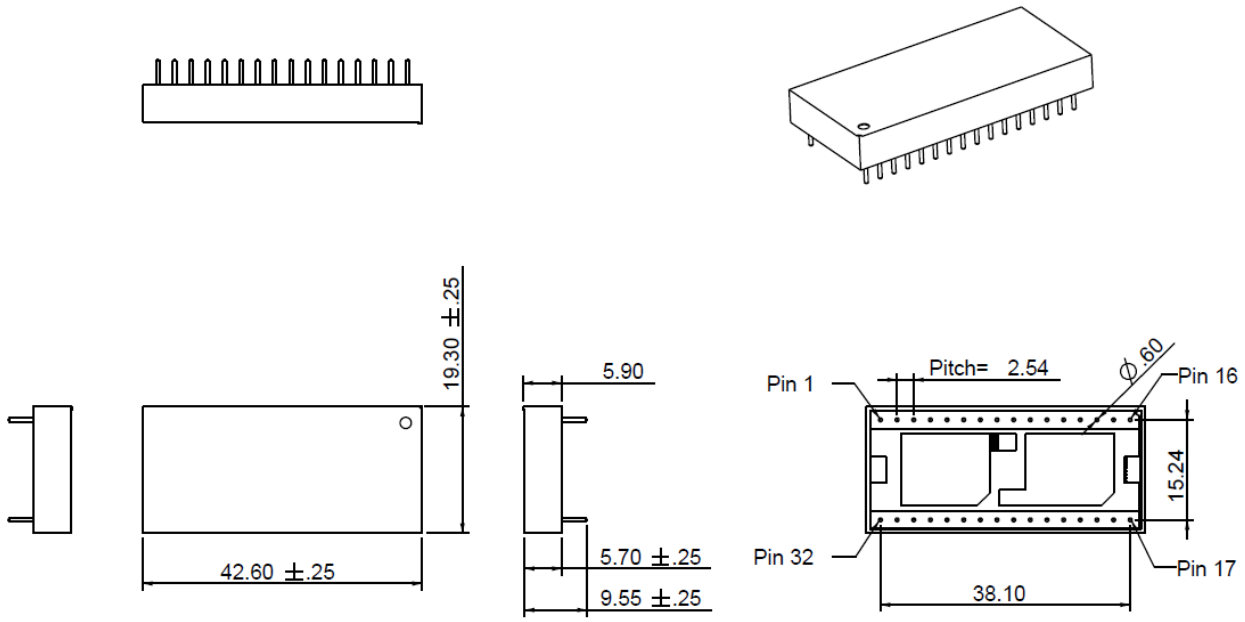
1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 7-4 Power Consumption

Capacity / Mode	128 MB	256 MB	512 MB	1 GB	2 GB	4 GB	8 GB	16 GB
Active (mA)	125	120	130	130	140	160	170	170
Idle (mA)	3	3	3	3	3	3	3	3

Note:
*All values are typical and may vary depending on flash configurations or host system settings.
**Active power is an average power measurement performed using CrystalDiskMark with 128KB sequential read/write transfers.

8. Physical Characteristics



Unit: mm

Tolerance: ± 0.2

9. Product Ordering Information

9.1 Product Code Designations

AP – FC 0xxX C 1 N x X – X X X

Operating Temperature Range
Blank: Standard Temperature
W: WideTemperature

Flash Type

Firmware Version

Option
D: UDMA Mode
P: PIO Mode
M: MWDMA Mode

Voltage
3: 3.3V
5: 5.0V

Speed
N: Standard

PCB Version

Controller Version

Capacity

0128:	128MB	002G:	2GB
0256:	256MB	004G:	4GB
0512:	512MB	008G:	8GB
001G:	1GB	016G:	16GB

Model Name

Apacer Product Code

9.2 Valid Combinations

A. Standard Temperature

9.2.1 UDMA Mode

Capacity	Part Number (3.3V)	Part Number (5V)
128MB	AP-FC0128C1N3D-T	AP-FC0128C1N5D-T
256MB	AP-FC0256C1N3D-T	AP-FC0256C1N5D-T
512MB	AP-FC0512C1N3D-T	AP-FC0512C1N5D-T
1GB	AP-FC001GC1N3D-T	AP-FC001GC1N5D-T
2GB	AP-FC002GC1N3D-T	AP-FC002GC1N5D-T
4GB	AP-FC004GC1N3D-T	AP-FC004GC1N5D-T
8GB	AP-FC008GC1N3D-T	AP-FC008GC1N5D-T

9.2.2 PIO Mode

Capacity	Part Number (3.3V)	Part Number (5V)
128MB	AP-FC0128C1N3P-T	AP-FC0128C1N5P-T
256MB	AP-FC0256C1N3P-T	AP-FC0256C1N5P-T
512MB	AP-FC0512C1N3P-T	AP-FC0512C1N5P-T
1GB	AP-FC001GC1N3P-T	AP-FC001GC1N5P-T
2GB	AP-FC002GC1N3P-T	AP-FC002GC1N5P-T
4GB	AP-FC004GC1N3P-T	AP-FC004GC1N5P-T
8GB	AP-FC008GC1N3P-T	AP-FC008GC1N5P-T

9.2.3 MWDMA Mode

Capacity	Part Number (3.3V)	Part Number (5V)
128MB	AP-FC0128C1N3M-T	AP-FC0128C1N5M-T
256MB	AP-FC0256C1N3M-T	AP-FC0256C1N5M-T
512MB	AP-FC0512C1N3M-T	AP-FC0512C1N5M-T
1GB	AP-FC001GC1N3M-T	AP-FC001GC1N5M-T
2GB	AP-FC002GC1N3M-T	AP-FC002GC1N5M-T
4GB	AP-FC004GC1N3M-T	AP-FC004GC1N5M-T
8GB	AP-FC008GC1N3M-T	AP-FC008GC1N5M-T

B. Wide Temperature

9.2.4 UDMA Mode

Capacity	Part Number (3.3V)	Part Number (5V)
128MB	AP-FC0128C1N3D-TW	AP-FC0128C1N5D-TW
256MB	AP-FC0256C1N3D-TW	AP-FC0256C1N5D-TW
512MB	AP-FC0512C1N3D-TW	AP-FC0512C1N5D-TW
1GB	AP-FC001GC1N3D-TW	AP-FC001GC1N5D-TW
2GB	AP-FC002GC1N3D-TW	AP-FC002GC1N5D-TW
4GB	AP-FC004GC1N3D-TW	AP-FC004GC1N5D-TW
8GB	AP-FC008GC1N3D-TW	AP-FC008GC1N5D-TW

9.2.5 PIO Mode

Capacity	Part Number (3.3V)	Part Number (5V)
128MB	AP-FC0128C1N3P-TW	AP-FC0128C1N5P-TW
256MB	AP-FC0256C1N3P-TW	AP-FC0256C1N5P-TW
512MB	AP-FC0512C1N3P-TW	AP-FC0512C1N5P-TW
1GB	AP-FC001GC1N3P-TW	AP-FC001GC1N5P-TW
2GB	AP-FC002GC1N3P-TW	AP-FC002GC1N5P-TW
4GB	AP-FC004GC1N3P-TW	AP-FC004GC1N5P-TW
8GB	AP-FC008GC1N3P-TW	AP-FC008GC1N5P-TW

9.2.6 MWDMA Mode

Capacity	Part Number (3.3V)	Part Number (5V)
128MB	AP-FC0128C1N3M-TW	AP-FC0128C1N5M-TW
256MB	AP-FC0256C1N3M-TW	AP-FC0256C1N5M-TW
512MB	AP-FC0512C1N3M-TW	AP-FC0512C1N5M-TW
1GB	AP-FC001GC1N3M-TW	AP-FC001GC1N5M-TW
2GB	AP-FC002GC1N3M-TW	AP-FC002GC1N5M-TW
4GB	AP-FC004GC1N3M-TW	AP-FC004GC1N5M-TW
8GB	AP-FC008GC1N3M-TW	AP-FC008GC1N5M-TW

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Revision History

Revision	Description	Date
1.0	Initial release	12/31/2014
1.1	Added 128MB support	1/27/2015
1.2	Modified 128MB total bytes at Table 4-1 Capacity Specifications	2/7/2020

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