Apacer

RoHS Recast Compliant

Industrial MicroSD

R1 Product Specifications

September 16, 2020

Version 1.8

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Apacer

Specifications Overview:

- **Fully Compatible with SD Card Specifications 3.0, 2.0 and 1.1**
  - Part 1, Physical Layer Specification, Ver 3.00 Final
  - Part 2, File System Specification, Ver 3.00
  - Part 3, Security Specification, Ver 3.00 Final
- **Capacity**
  - SD 2.0: 1, 2 GB
  - SD 3.0: 4, 8 GB
- **Performance***
  - Sequential read: Up to 34 MB/sec
  - Sequential write: Up to 28 MB/sec
- **Flash Management**
  - Built-in advanced ECC algorithm
  - Global Wear Leveling
  - Flash bad-block management
  - Power Management
  - S.M.A.R.T.
  - Page Mapping
  - Power Failure Management
- **SD-Protocol Compatible**
- **Supports SD SPI Mode**
- **NAND Flash Type: SLC**
- **Temperature Range**
  - Operating: -40°C to 85°C
  - Storage: -40°C to 85°C
- **Operating Voltage: 2.7V ~ 3.6V**
- **Power Consumption***
  - Operating: 115 mA
  - Standby: 265 µA
- **Standard Interface**
  - 8-pin SD interface
- **Bus Speed Mode: Supports Class 6 and Class 10 with UHS-I****
  - DS: Default Speed up to 25MHz 3.3V signaling
  - HS: High Speed up to 50MHz 3.3V signaling
  - SDR12: SDR up to 25MHz 1.8V signaling
  - SDR25: SDR up to 50MHz 1.8V signaling
  - SDR50: SDR up to 100MHz 1.8V signaling
  - SDR104: SDR up to 208MHz 1.8V signaling
  - DDR50: DDR up to 50MHz 1.8V signaling
- **Physical Dimensions**
  - 15mm (L) x 11mm (W) x 1mm (H)
- **RoHS Recast Compliant (2011/65/EU)**

*Performance values presented here are typical and measured based on USB 3.0 card reader. The results may vary depending on settings and platforms.
**Class 6 is only supported on 1GB and 2GB. Timing in 1.8V signaling is different from that of 3.3V signaling. Operation mode selection command is complaint with SD 3.0, referring to SDA's Part 1, Physical Layer Specification, Ver 3.01 (Section 3.9).

Table of Contents

1. General Descriptions

As the demand of reliable and high-performance data storage in a small form factor increases, Apacer's MicroSD card is designed specifically for multiple applications by offering high endurance, reliability, and agility, where extreme flexibility, endurance, data integrity, and exceptionally transmission are required.

The MicroSD card fully complies with SD Card Association standard. The Command List is compatible with [Part 1 Physical Layer Specification Ver3.0 Final] definitions, while the Card Capacity of Non-secure Area, Secure Area supports [Part 3 Security Specification Ver3.0 Final] Specifications. The card allows selection of either SD or SPI mode for compatibility in data communication.

The card also comes with endurance features for data error detection and correction.

1.1 Product Functional Block

The MicroSD contains a card controller and a memory core for the SD standard interface.

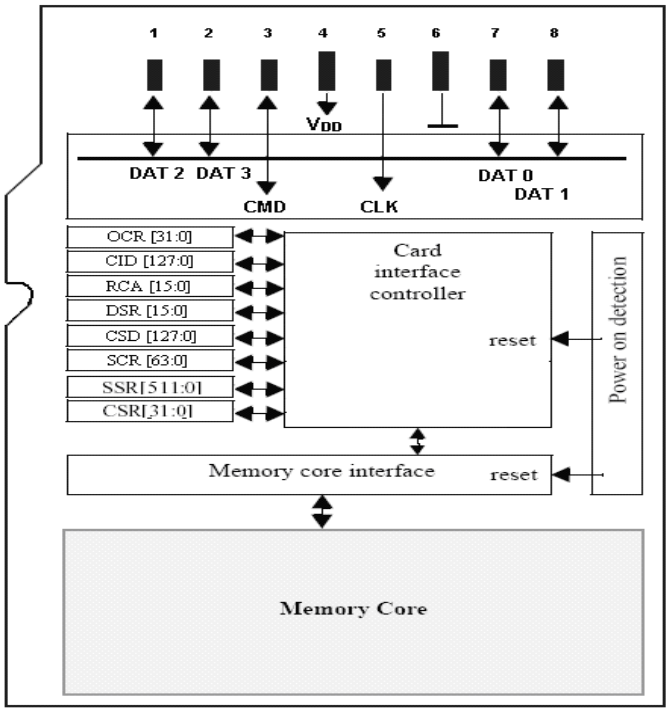


Figure 1-1 Functional Block Diagram

1.2 Flash Management

1.2.1 Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. Apacer implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

1.2.2 ECC Algorithms

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, the MicroSD card applies the BCH ECC Algorithm, which can detect and correct errors occur during read process, ensure data been read correctly, as well as protect data from corruption. The MicroSD controller can detect and correct up to 43 bits error in 1K bytes.

1.2.3 Power Management

A power saving feature of the MicroSD is automatic entrance and exit from sleep mode. Upon completion of an operation, the SD will enter the sleep mode to conserve power if no further commands are received within X seconds, where X is programmable by software. The master does not have to take any action for this to occur. The SD is in sleep mode except when the host is accessing it, thus conserving power.

Any command issued by the master to the MicroSD will cause it to exit sleep mode and response to the master.

1.2.4 S.M.A.R.T.

S.M.A.R.T. (SMART), an acronym stands for Self-Monitoring, Analysis and Reporting Technology, is an open standard allowing an individual disk drive in the ATA/IDE or SCSI interface to automatically monitor its own health and report potential problems in order to prevent data loss. This failure warning technology provides predictions from unscheduled downtime by observing and storing critical drive performance and calibration parameters. Ideally, this should allow taking hands-on actions to keep from impending drive failure.

Failures are divided into two categories: those that can be predicted and those that cannot. Predictable failures occur gradually over time, and the decline in performance can be detected; on the other hand, unpredictable failures happen very sudden without any warning. These failures may be caused by power surges or related to electronic components. The purpose of the SMART implementation is to predict near-term failures of each individual disk drive and generate a warning to prevent unfortunate loss.

1.2.5 Global Wear Leveling

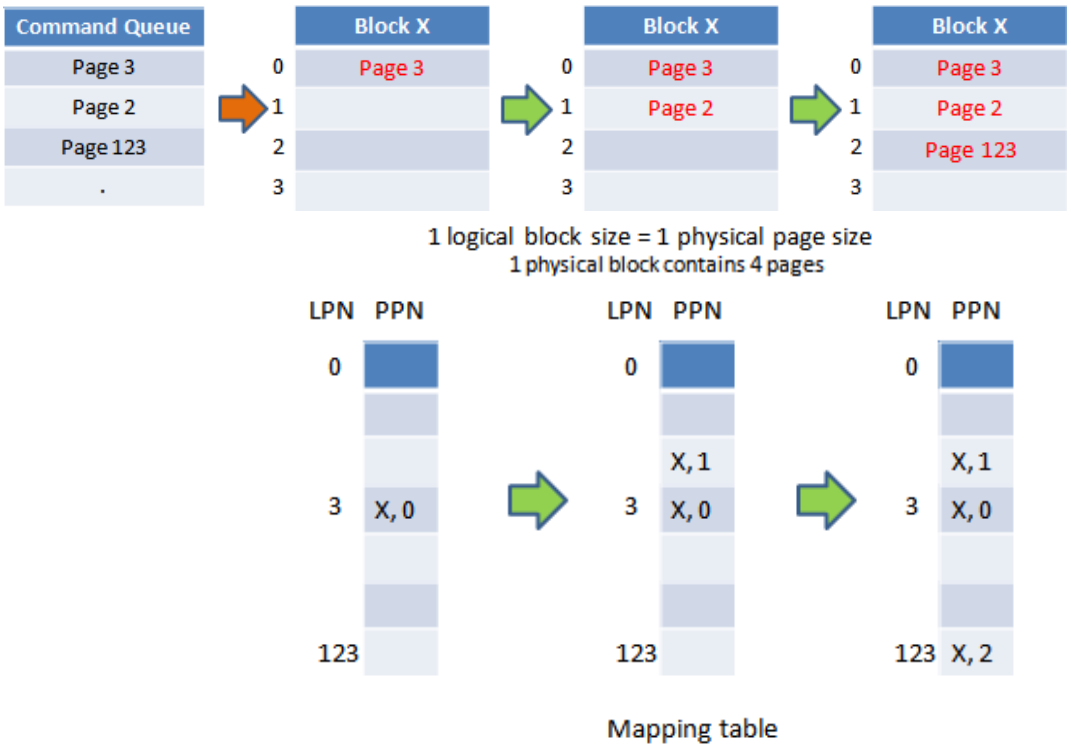
NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some area get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Global Wear Leveling technique is applied to extend the lifespan of NAND Flash by evenly distributing writes and erase cycles across the media.

Apacer provides Global Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing Global Wear Leveling algorithm, the life expectancy of the NAND Flash is greatly improved.

1.2.6 Page Mapping

Page-level mapping uses one page as the unit of mapping. The most important characteristic of page-level mapping is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different size of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. The below example shows how page-level mapping performs a write command:

Host instructs three write commands: page 3, 2, and 123. The three pages are written into block X in sequence of command queue. Once all write commands are completed, the mapping table updates itself automatically.



Note: The example only shows the concept of how page-level mapping work and do not necessary happen in an actual case.

This fine-grained page-level mapping scheme makes better capability for handling random data, and increases overall performance and endurance significantly. However, page-level mapping requires SSDs to incorporate a larger RAM in order to maintain its mapping table.

1.2.7 Power Failure Management

Apacer industrial SD and MicroSD cards provide complete data protection mechanism during every abnormal power shutdown situation, such as power failure at programming data, updating system tables, erasing blocks, etc. Apacer Power-Loss Protection mechanism includes:

- Maintaining data correctness and increasing the reliability of the data stored in the NAND Flash memory.
- Protecting F/W table and the data written to flash from data loss in the event of power off.

2. Product Specifications

2.1 Card Architecture

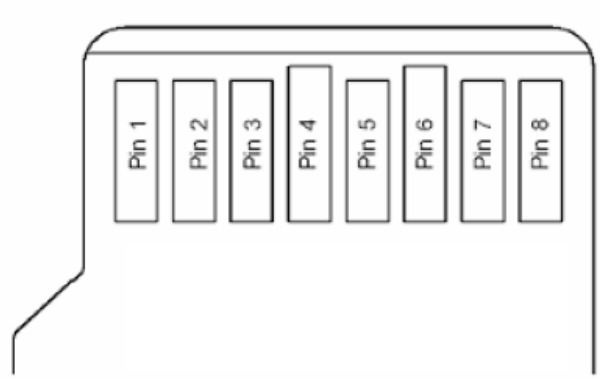


Figure 2-1 Card Architecture

2.2 Pin Assignment

Table 2-1 Pin Descriptions

Pin	SD Mode		SPI Mode	
	Name	Description	Name	Description
1	DAT2	Data Line[Bit 2]	RSV	Reserved
2	CD/DAT3	Card Detect/Data Line[Bit 3]	CS	Chip Select (neg true)
3	CMD	Command/Response	DI	Data In
4	VDD	Supply Voltage	VDD	Supply Voltage
5	CLK	Clock	SCLK	Clock
6	VSS	Supply Voltage Ground	VSS	Supply Voltage Ground
7	DAT0	Data Line[Bit 0]	DO	Data Out
8	DAT1	Data Line[Bit 1]	RSV	Reserved

2.3 Capacity Specifications

The following table shows the specific capacity for the SD 6.1 card.

Table 2-2 Capacity Specifications

Capacity	Total bytes*
1 GB	969,605,120
2 GB	1,938,489,344
4 GB	3,875,504,128
8 GB	7,751,041,024

Note: Total bytes are viewed under Windows operating system and were measured by SD format too.

2.4 Performance Specifications

Performances of the SD 6.1 card are shown in the table below.

Table 2-3 Performance Specifications

Capacity / Performance	1 GB	2 GB	4 GB	8 GB
Sequential Read* (MB/s)	23	23	34	33
Sequential Write* (MB/s)	16	18	28	28

Note: Results may differ from various flash configurations or host system setting.

2.5 Electrical Specifications

Table 2-4 Operating Voltages

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Power Supply Voltage	2.7	3.6	V

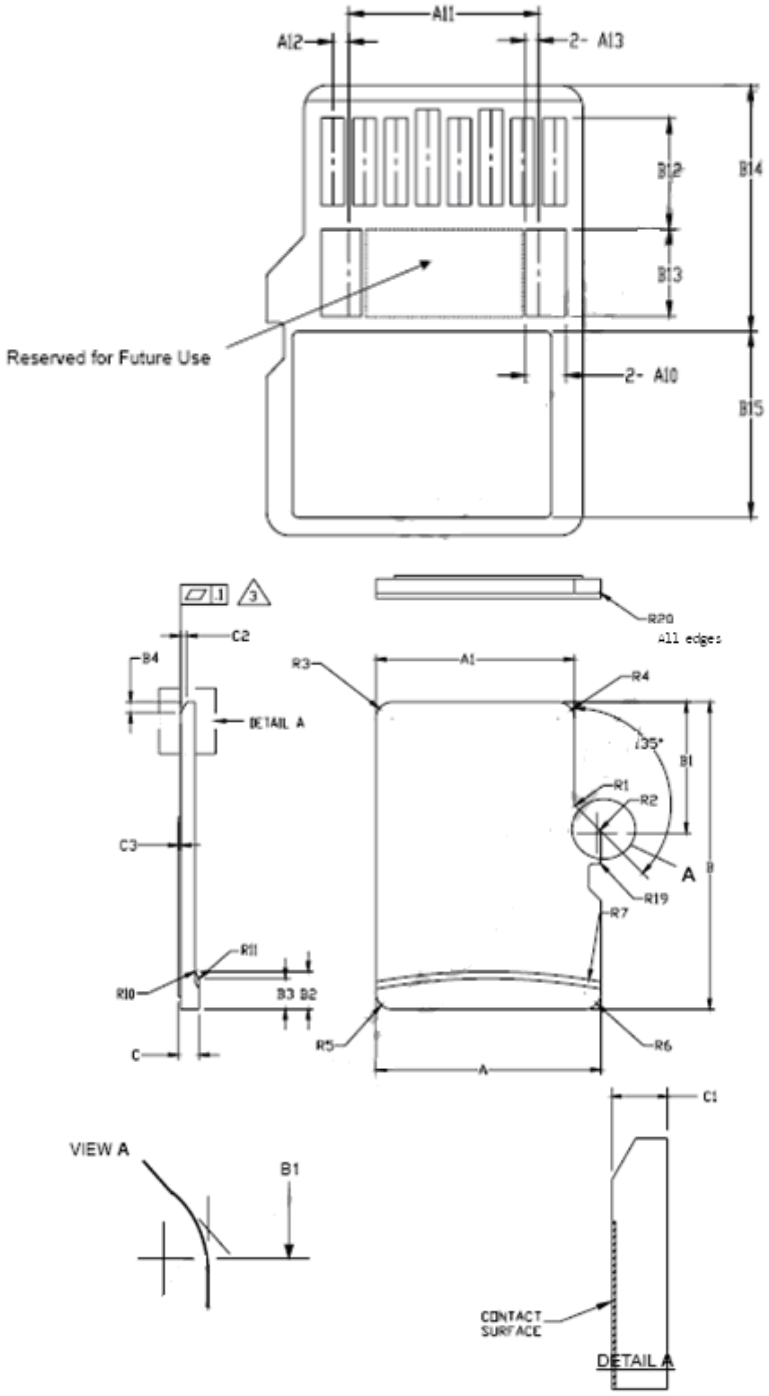
Table 2-5 Power Consumption

Capacity / Mode	1 GB	2 GB	4 GB	8 GB
Operating (mA)	110	110	110	115
Standby (µA)	160	160	260	265

Note: All values are typical and may vary depending on flash configurations or host system settings.

3. Physical Characteristics

3.1 Physical Dimensions



	COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX	NOTE
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.80	-	-	
A10	1.35	1.40	1.45	
A11	6.50	6.60	6.70	
A12	0.50	0.55	0.60	
A13	0.40	0.45	0.50	
B	14.90	15.00	15.10	
B1	6.30	6.40	6.50	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	5.50	-	-	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	-	-	9.00	
B10	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
B12	3.60	3.70	3.80	
B13	2.80	2.90	3.00	
B14	8.20	-	-	
B15	-	-	6.20	
C	0.90	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	
D1	1.00	-	-	
D2	1.00	-	-	
D3	1.00	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.70	0.80	0.90	
R6	0.70	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	
R20	0.02	-	0.15	

Notes:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. COPLANARITY IS ADDITIVE TO C1 MAX. THICKNESS.

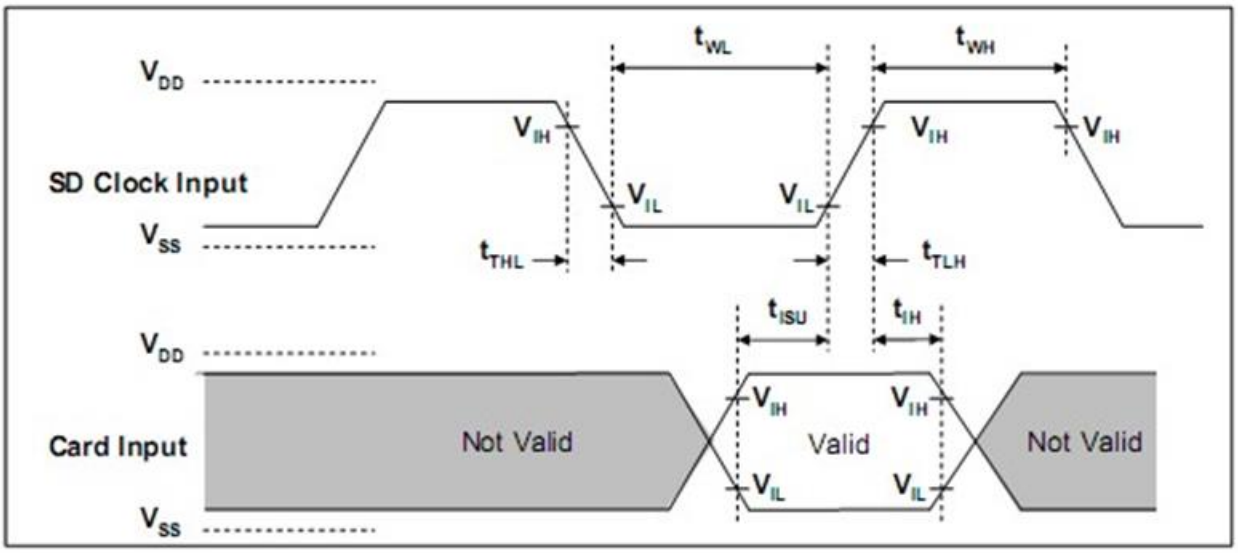
3.2 Durability Specifications

Table 3-1 Durability Specifications

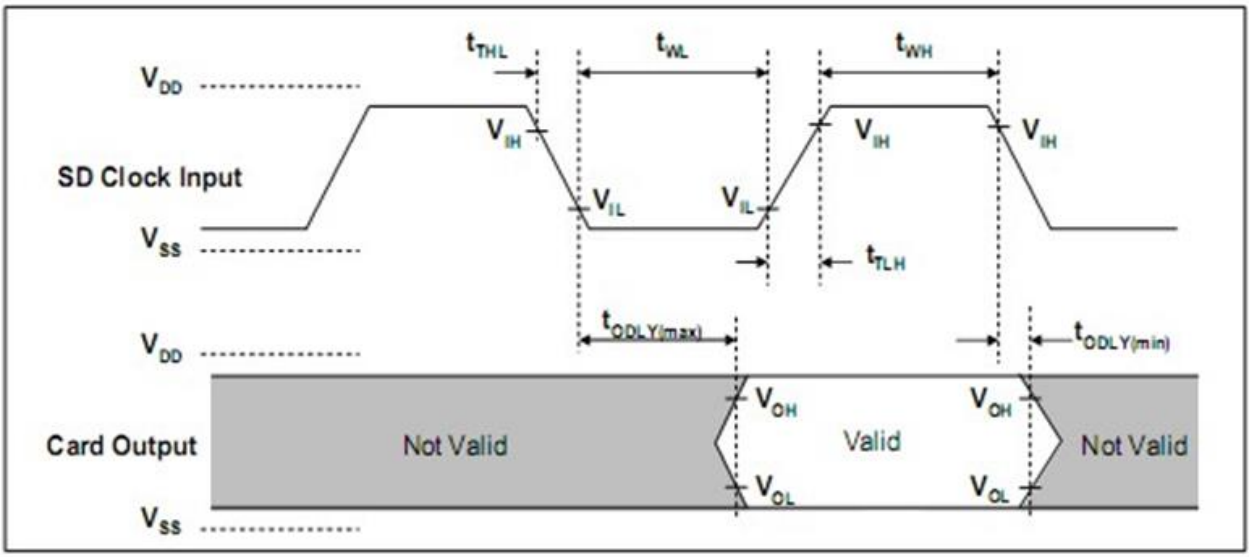
Item	Specifications
Temperature	-40°C to 85°C (Operating)
	-40°C to 85°C (Storage)
Shock	1,500G, 0.5ms
Vibration	20Hz~80Hz/1.52mm (frequency/displacement) 80Hz~2000Hz/20G (frequency/displacement) X, Y, Z axis/60mins each
Drop	150cm free fall, 6 face of each
Bending	≧10N, hold 1min/5times
Torque	0.1N-m or 2.5deg, hold 5min/5times
Salt Spray	Concentration: 3% NaCl at 35°C (storage for 24 hours)
Waterproof	JIS IPX7 compliance Water temperature 25°C Water depth: the lowest point of unit is locating 1000mm below surface (storage for 30 mins)
X-Ray Exposure	0.1 Gy of medium-energy radiation (70 KeV to 140 KeV, cumulative dose per year) to both sides of the card (storage for 30 mins)
Durability	10,000 times mating cycle
ESD	Pass

4. AC Characteristics

4.1 MicroSD Interface Timing (Default)



Card input Timing (Default Speed Card)

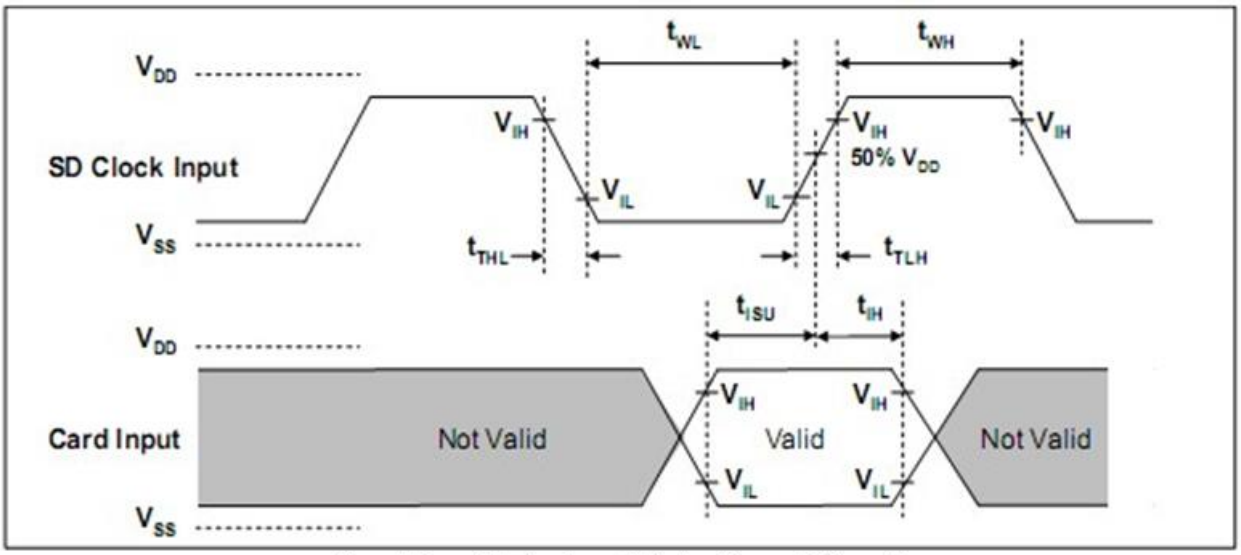


Card Output Timing (Default Speed Mode)

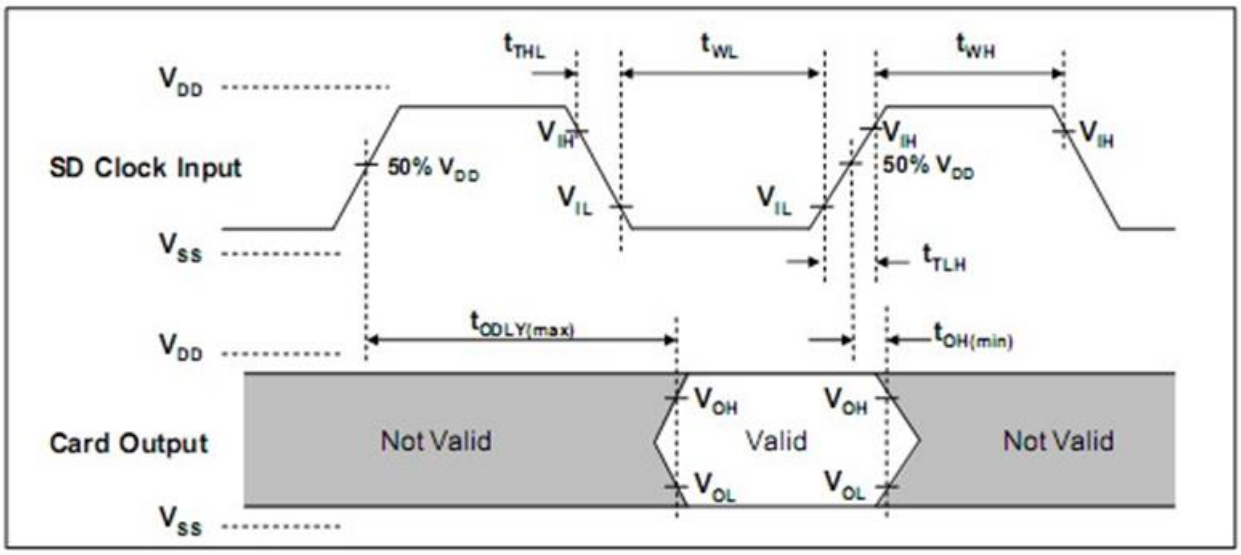
SYMBOL	PARAMETER	MIN	MAX	UNIT	REMARK
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
f_{PP}	Clock frequency data transfer	0	25	MHz	C_{card} ≤ 10 pF (1 card)
f_{OD}	Clock frequency identification	0[(1)]/100	400	KHz	C_{card} ≤ 10 pF (1 card)
t_{WL}	Clock low time	10	-	ns	C_{card} ≤ 10 pF (1 card)
t_{WH}	Clock high time	10	-	ns	C_{card} ≤ 10 pF (1 card)
t_{TLH}	Clock rise time	-	10	ns	C_{card} ≤ 10 pF (1 card)
t_{THL}	Clock fall time	-	10	ns	C_{card} ≤ 10 pF (1 card)
Inputs CMD, DAT (Referenced to CLK)					
t_{ISU}	Input setup time	5	-	ns	C_{card} ≤ 10 pF (1 card)
t_{TH}	Input hold time	5	-	ns	C_{card} ≤ 10 pF (1 card)
Outputs CMD, DAT (Referenced to CLK)					
t_{ODLY}	Output delay time during data transfer mode	0	14	ns	C_L ≤ 40 pF (1 card)
t_{OH}	Output hold time	0	50	ns	C_L ≤ 40 pF (1 card)

(1)0Hz means to stop the clock. The given minimum frequency range is for cases that require the clock to be continued.

4.2 MicroSD Interface Timing (High Speed Mode)



Card Input Timing (High Speed Card)



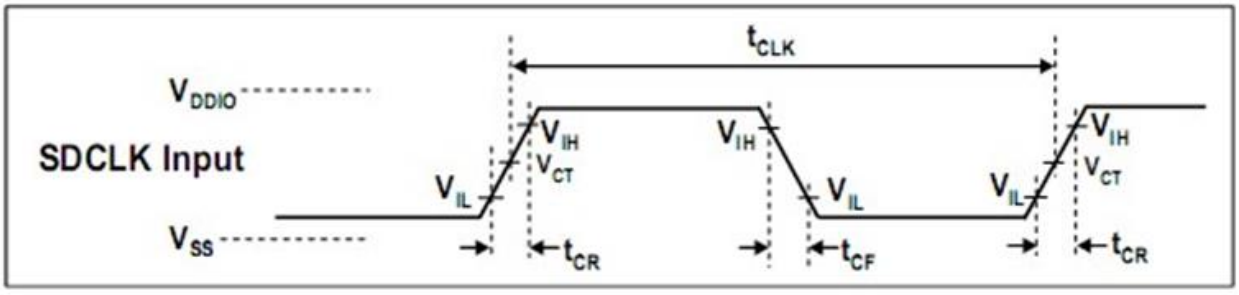
Card Output Timing (High Speed Mode)

SYMBOL	PARAMETER	MIN	MAX	UNIT	REMARK
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
f_{PP}	Clock frequency data transfer	0	50	MHz	Ccard ≤ 10 pF (1 card)
t_{WL}	Clock low time	7	-	ns	Ccard ≤ 10 pF (1 card)
t_{WH}	Clock high time	7	-	ns	Ccard ≤ 10 pF (1 card)
t_{TLH}	Clock rise time	-	3	ns	Ccard ≤ 10 pF (1 card)
t_{THL}	Clock fall time	-	3	ns	Ccard ≤ 10 pF (1 card)
Inputs CMD, DAT (Referenced to CLK)					
t_{ISU}	Input setup time	6	-	ns	Ccard ≤ 10 pF (1 card)
t_{TH}	Input hold time	2	-	ns	Ccard ≤ 10 pF (1 card)
Outputs CMD, DAT (Referenced to CLK)					
t_{ODLY}	Output delay time during data transfer made	-	14	ns	CL ≤ 40 pF (1 card)
t_{OH}	Output hold time	2.5	-	ns	CL ≥ 15 pF (1 card)
C_L	Total system capacitance for each line*	-	40	pF	1 card

*In order to satisfy severe timing, host shall run on only one card

4.3 MicroSD Interface Timing (SDR12, SDR25, SDR50 and SDR104 Modes)

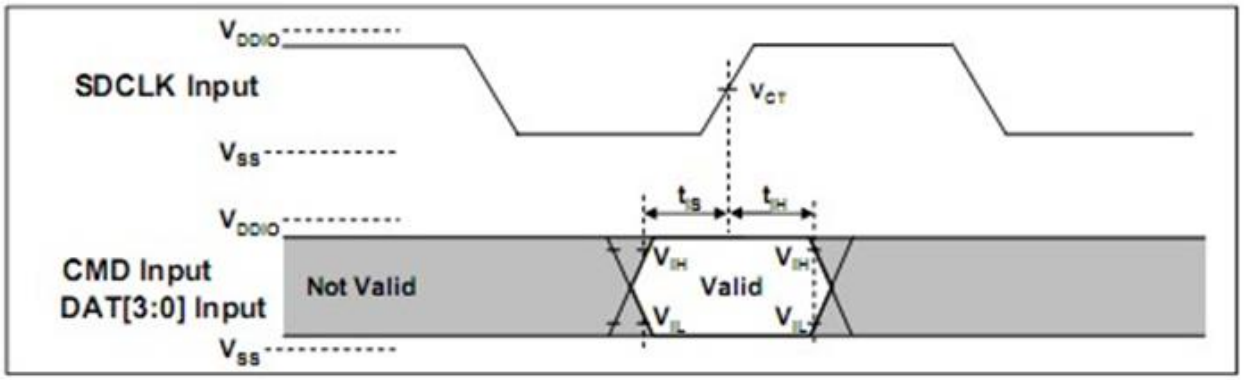
4.3.1 Clock Timing



Clock Signal Timing

SYMBOL	MIN	MAX	UNIT	REMARK
t_{CLK}	4.8	-	ns	208MHz (Max.), Between rising edge, V_{CT} = 0.975V
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 2.00ns (max.) at 208MHz, C_{CARD}=10pF t_{CR}, t_{CF} < 2.00ns (max.) at 100MHz, C_{CARD}=10pF The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	

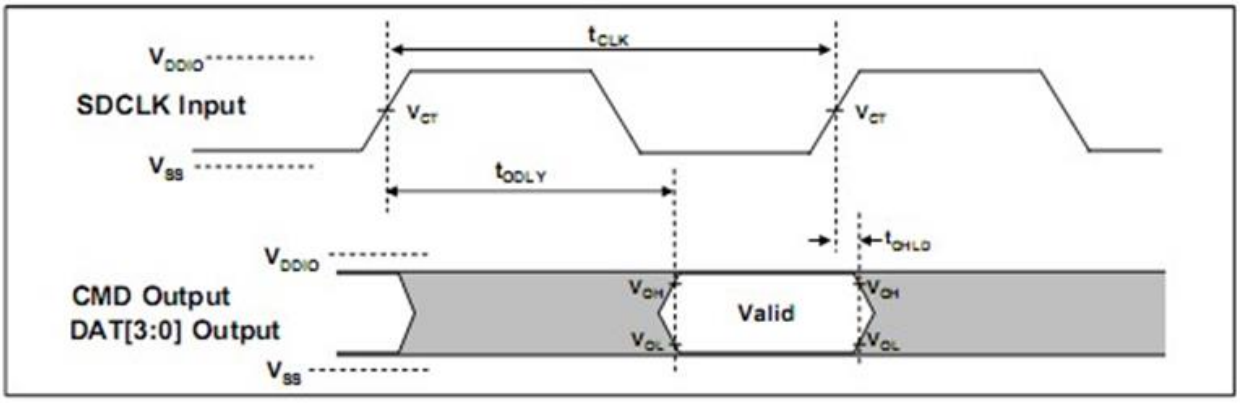
4.3.2 Card Input Timing



Card Input Timing

SYMBOL	MIN	MAX	UNIT	SDR104 MODE
t_{IS}	1.40	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5pF, V_{CT} = 0.975V
SYMBOL	**MIN**	**MAX**	**UNIT**	**SDR12, SDR25 and SDR50 MODES**
t_{IS}	3.00	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5pF, V_{CT} = 0.975V

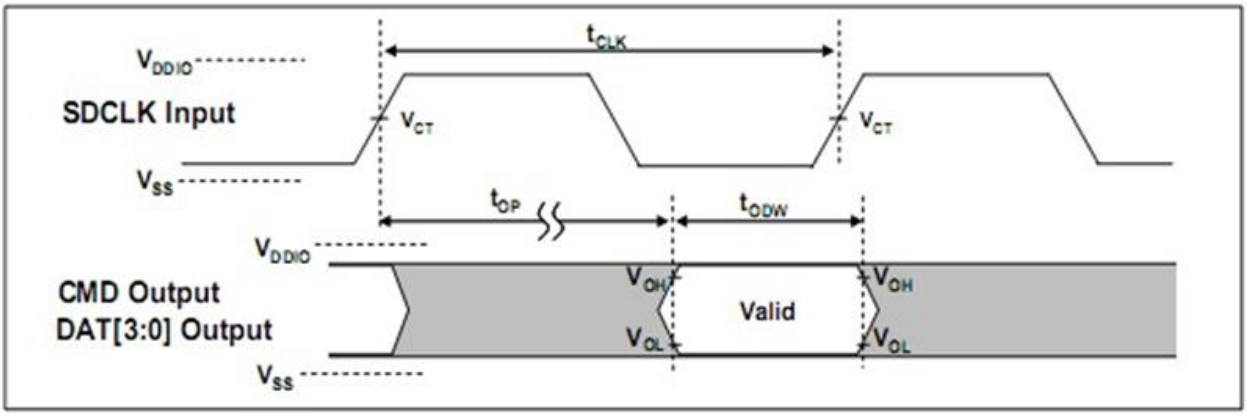
4.3.3 Card Output Timing of Fixed Data Window (SDR12, SDR25 and SDR50)



Output Timing of Fixed Date Window

SYMBOL	MIN	MAX	UNIT	REMARK
t_{ODLY}	-	7.5	ns	t_{CLK} ≥10.0ns, CL=30pF, using driver Type B, for SDR50.
t_{ODLY}		14	ns	t_{CLK} ≥20.0ns, CL=40pF, using driver Type B, for SDR25 and SDR12.
t_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.). CL=15pF

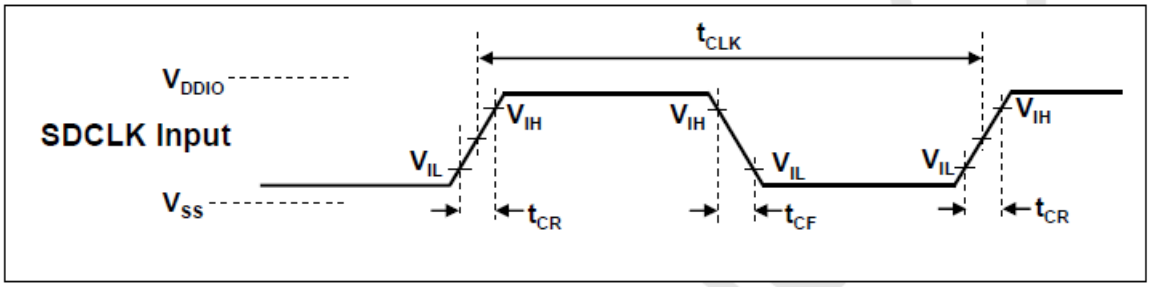
4.3.4 Output Timing of Variable Window (SDR104)



Output Timing of Variable Data Window

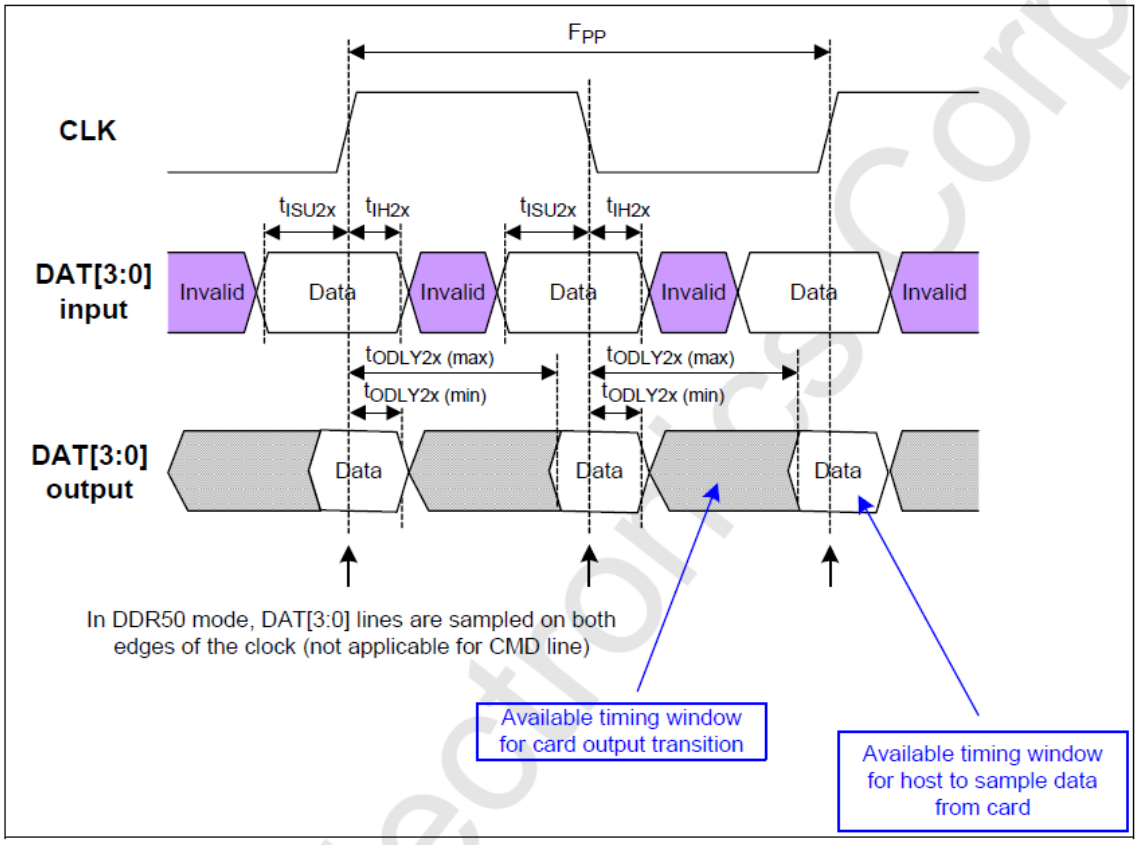
SYMBOL	MIN	MAX	UNIT	REMARK
t_{OP}	-	2	UI	Card Output Phase
Δt_{OP}	-350	+1550	ps	Delay variation due to temperature change after tuning
t_{ODW}	0.60	-	UI	t_{ODW} = 2.88ns at 208MHz

4.3.5 SD Interface Timing (DDR50 Mode)



Clock Signal Timing

SYMBOL	MIN	MAX	UNIT	REMARK
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 4.00ns (max.) at 50MHz, CCARD=10pF
Clock Duty	45	55	%	



Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

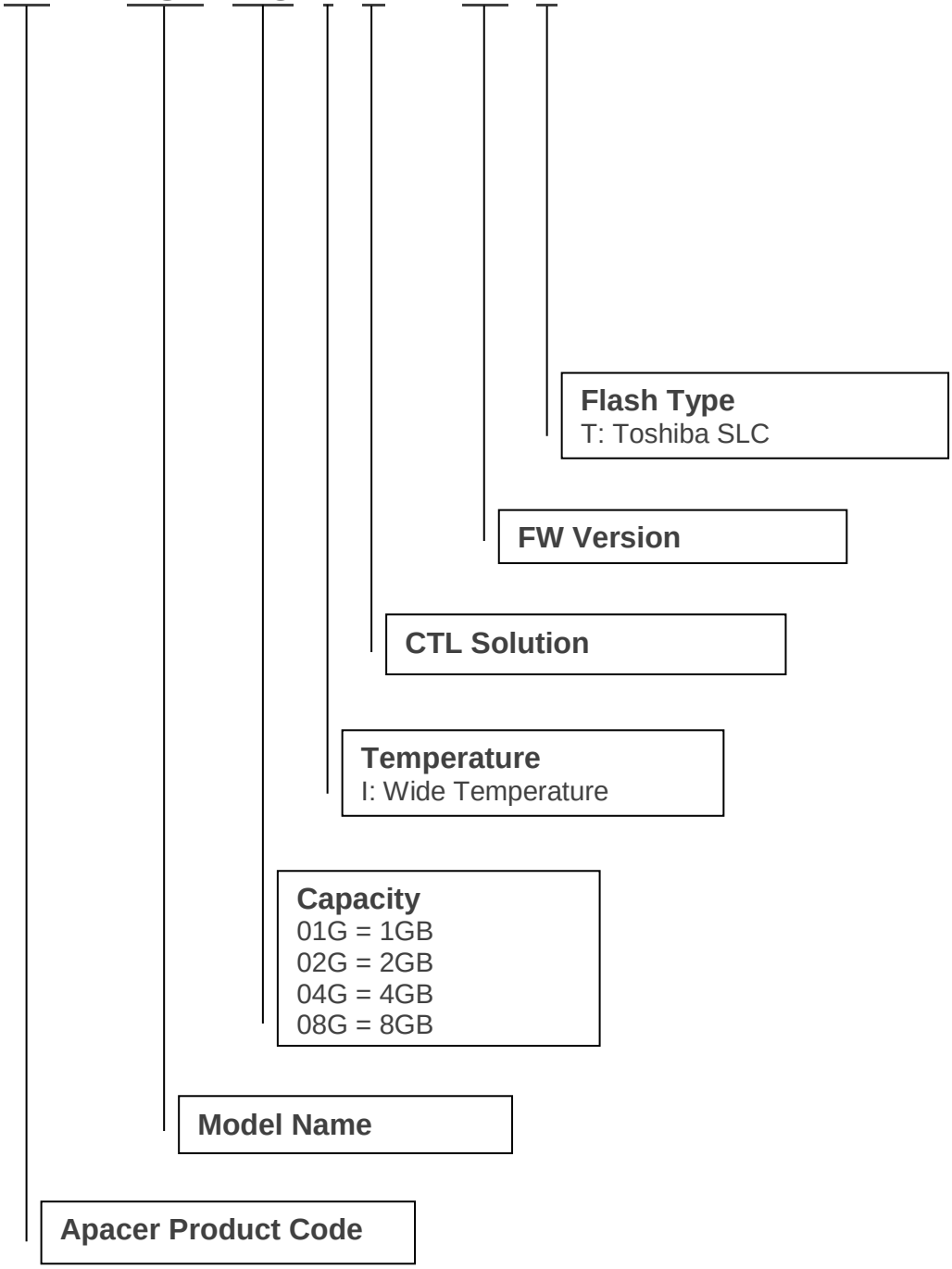
4.3.6 Bus Timings – Parameters Values (DDR50 Mode)

Symbol	Parameters	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
t_{ISU}	Input set-up time	6	-	ns	C_{card}≤ 10 pF (1 card)
t_{IH}	Input hold time	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Output CMD (referenced to CLK rising edge)					
t_{ODLY}	Output Delay time during Data Transfer Mode	-	13.7	ns	C_L≤30 pF (1 card)
T_{OH}	Output Hold time	1.5	-	ns	C_L≥15 pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
t_{ISU2x}	Input set-up time	3	-	ns	C_{card}≤ 10 pF (1 card)
t_{IH2x}	Input hold time	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
t_{ODLY2x}	Output Delay time during Data Transfer Mode	-	7.0	ns	C_L≤25 pF (1 card)
T_{OH2x}	Output Hold time	1.5	-	ns	C_L≥15 pF (1 card)

5. Product Ordering Information

5.1 Product Code Designations

AP – MSD xxG I E – AA T



5.2 Valid Combinations

Capacity	Part Number
1GB	AP-MSD01GIE-AAT
2GB	AP-MSD02GIE-AAT
4GB	AP-MSD04GIE-AAT
8GB	AP-MSD08GIE-AAT

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Revision History

Revision	Description	Date
1.0	Official release	12/22/2015
1.1	- Added S.M.A.R.T. chapter - Revised product ordering information	1/13/2016
1.2	Specified supported capacity for SD 2.0 and SD 3.0 respectively	1/18/2016
1.3	Removed S.M.A.R.T. chapter	2/1/2016
1.4	Added support for page mapping	6/7/2016
1.5	Added Power Failure Management to Features and General Description	10/3/2016
1.6	Removed “The data written at the exact moment power off will be lost, and the max data loss is 16 sectors.” from 1.2.7 Power Failure Management	10/7/2016
1.7	Added bus speed mode support to Specifications Overview	8/25/2020
1.8	Updated 1.2.2 Powerful ECC Algorithms	9/16/2020

Global Presence

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