

RoHS Recast Compliant

Industrial MicroSD

R1-M Product Specifications

October 16, 2017

Version 1.0



Apacer Technology Inc.

1F, No.32, Zhongcheng Rd., Tucheng Dist., New Taipei City, Taiwan, R.O.C

Tel: +886-2-2267-8000 Fax: +886-2-2267-2261

www.apacer.com

Features:

- **Fully Compatible with SD Card Specifications 3.0, 2.0 and 1.1**
 - Part 1, Physical Layer Specification, Ver 3.00 Final
 - Part 2, File System Specification, Ver 3.00
 - Part 3, Security Specification, Ver 3.00 Final
- **Capacity**
 - 8, 16 GB
- **Performance***
 - Burst read/write: 600 MB/sec
 - Sequential read: Up to 80 MB/sec
 - Sequential write: Up to 50 MB/sec
 - Random read (4K): Up to 1,200 IOPS
 - Random write (4K): Up to 145 IOPS
- **Flash Management**
 - Built-in advanced ECC algorithm
 - Global Wear Leveling
 - Flash bad-block management
 - Page Mapping
 - S.M.A.R.T.
 - Power Failure Management
 - Read Disturb Management
- **NAND Flash Type:** MLC
- **Standard Interface**
 - 8-pins SD interface
- **Temperature Range**
 - Operating: -25°C to 85°C
 - Storage: -40°C to 85°C
- **Operating Voltage: 2.7V ~ 3.6V**
- **Power Consumption***
 - Active mode: 150 mA
 - Idle mode: 315 mA
- **Bus Speed Mode: Support Class 10 with UHS-I****
 - DS: Default Speed up to 25MHz 3.3V signaling
 - HS: High Speed up to 50MHz 3.3V signaling
 - SDR12: SDR up to 25MHz 1.8V signaling
 - SDR25: SDR up to 50MHz 1.8V signaling
 - SDR50: SDR up to 100MHz 1.8V signaling
 - SDR104: SDR up to 208MHz 1.8V signaling
 - DDR50: DDR up to 50MHz 1.8V signaling
- **SD-Protocol Compatible**
- **Supports SD SPI Mode**
- **Physical Dimensions:**
15mm (L) x 11mm (W) x 1mm (H)
- **RoHS Recast Compliant (2011/65/EU)**

*Varies from capacities. Performance values presented here are typical and measured based on USB 3.0 card reader. The results may vary depending on settings and platforms.

**Timing in 1.8V signaling is different from that of 3.3V signaling. Operation mode selection command is compliant with SD 3.0, referring to SDA's Part 1, Physical Layer Specification, Ver 3.01 (Section 3.9)

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1. General Descriptions

As the demand of reliable and high-performance data storage in a small form factor increases, Apacer's MicroSD card is designed specifically for multiple applications by offering high endurance, reliability, and agility, where extreme flexibility, endurance, data integrity, and exceptionally transmission are required.

The MicroSD card fully complies with SD Card Association standard. The Command List is compatible with [Part 1 Physical Layer Specification Ver3.0 Final] definitions, while the Card Capacity of Non-secure Area, Secure Area supports [Part 3 Security Specification Ver3.0 Final] Specifications. The card allows selection of either SD or SPI mode for compatibility in data communication.

The card also comes with endurance features for data error detection and correction.

1.1 Product Functional Block

The MicroSD contains a card controller and a memory core for the SD standard interface.

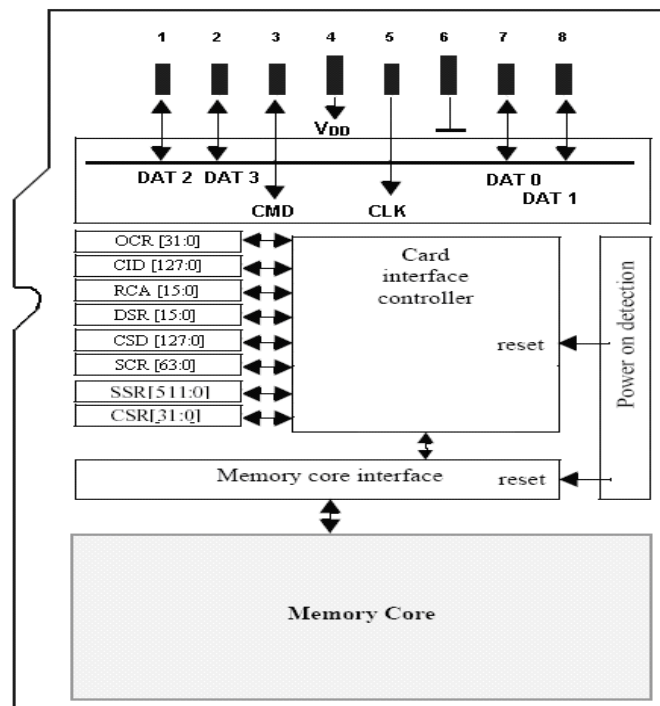


Figure 1-1 Block Diagram

1.2 Flash Management

1.2.1 Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. Apacer implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

1.2.2 Powerful ECC Algorithms

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, the MicroSD card applies the BCH ECC Algorithm, which can detect and correct errors occur during read process, ensure data been read correctly, as well as protect data from corruption.

1.2.3 Global Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some area get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Global Wear Leveling technique is applied to extend the lifespan of NAND Flash by evenly distributing writes and erase cycles across the media.

Apacer provides Global Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing Global Wear Leveling algorithm, the life expectancy of the NAND Flash is greatly improved.

1.2.4 S.M.A.R.T.

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is a special function that allows a memory device to automatically monitor its health. Apacer provides a program named SmartInfo Tool to observe Apacer’s SD and MicroSD cards. Note that this tool can only support Apacer’s industrial SD and MicroSD cards. This tool will display firmware version, endurance life ratio, good block ratio, and so forth.

1.2.5 Power Failure Management

Apacer industrial SD and MicroSD cards provide complete data protection mechanism during every abnormal power shutdown situation, such as power failure at programming data, updating system tables, erasing blocks, etc. Apacer Power-Loss Protection mechanism includes:

- Maintaining data correctness and increasing the reliability of the data stored in the NAND Flash memory.
- Protecting F/W table and the data written to flash from data loss in the event of power off.

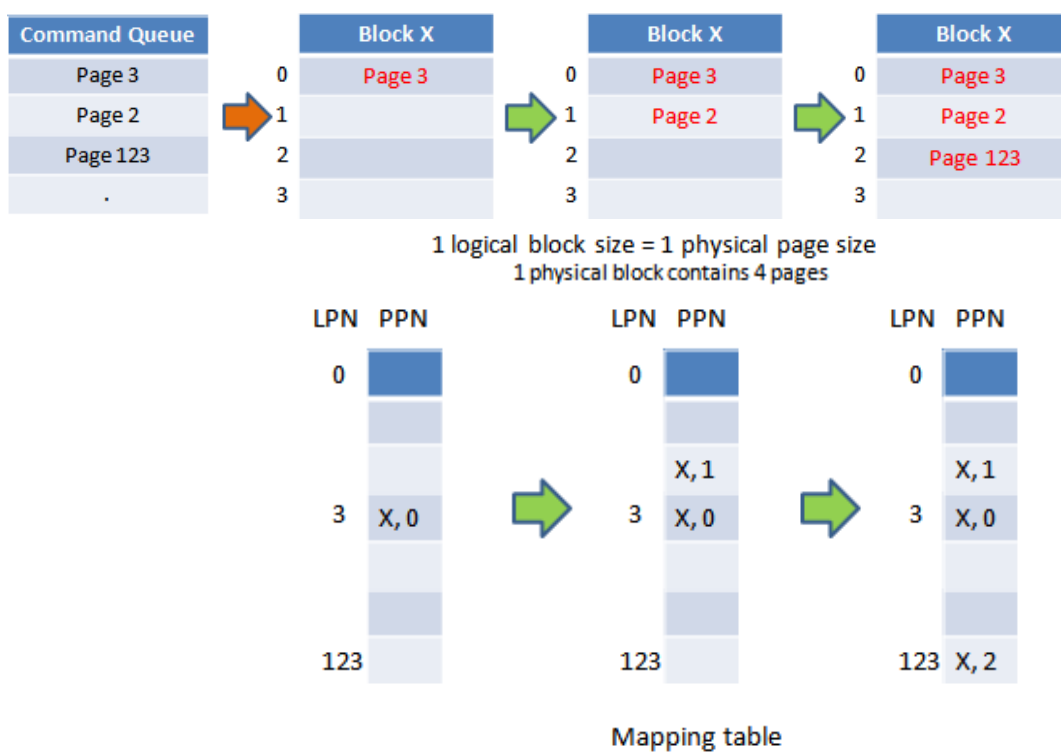
1.2.6 Read Disturb Management

When continuously being read, NAND flash memory cannot engage wear leveling since this applies while writing data. Subsequently, errors aggregated over time and become uncorrectable. To keep errors from going beyond ECC’s capability to recover and memory blocks in good hands, Apacer’s Auto-Read Refresh will spontaneously refresh the bit errors when the threshold is triggered by the error count in a block.

1.2.7 Page Mapping

Page-level mapping uses one page as the unit of mapping. The most important characteristic of page-level mapping is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different size of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. The below example shows how page-level mapping performs a write command:

Host instructs three write commands: page 3, 2, and 123. The three pages are written into block X in sequence of command queue. Once all write commands are completed, the mapping table updates itself automatically.

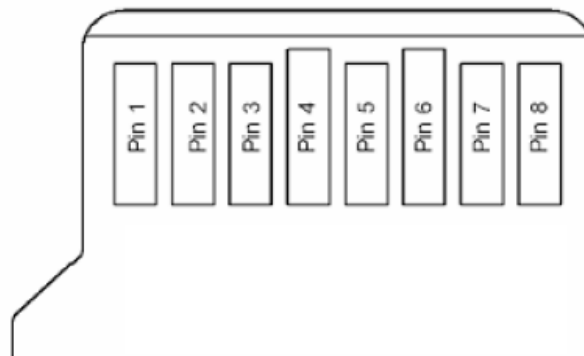


Note: The example only shows the concept of how page-level mapping work and do not necessary happen in an actual case.

This fine-grained page-level mapping scheme makes better capability for handling random data, and increases overall performance and endurance significantly. However, page-level mapping requires SSDs to incorporate a larger RAM in order to maintain its mapping table.

2. Electrical Characteristics

2.1 Card Architecture



2.2 Pin Assignment

Table 2-1 Pin Descriptions

Pin	SD Mode		SPI Mode	
	Name	Description	Name	Description
1	DAT2	Data Line[Bit 2]	RSV	Reserved
2	CD/DAT3	Card Detect/Data Line[Bit 3]	CS	Chip Select (neg true)
3	CMD	Command/Response	DI	Data In
4	VDD	Supply Voltage	VDD	Supply Voltage
5	CLK	Clock	SCLK	Clock
6	VSS	Supply Voltage Ground	VSS	Supply Voltage Ground
7	DAT0	Data Line[Bit 0]	DO	Data Out
8	DAT1	Data Line[Bit 1]	RSV	Reserved

2.3 Capacity Specifications

The following table shows the specific capacity for the SD card.

Table 2-2 Capacity Specifications

Capacity	Total bytes*
8 GB	7,734,296,576
16 GB	15,468,593,152

Note: Total bytes are viewed under Windows operating system and were measured by SD format too.

2.4 Performance Specifications

Performances of the SD card are shown in the table below.

Table 2-3 Performance Specifications

Capacity	8 GB	16 GB
Sequential Read* (MB/s)	75	80
Sequential Write* (MB/s)	26	50
Random Read IOPS** (4K)	1,200	1,100
Random Write IOPS** (4K)	105	145

Note:

Results may differ from various flash configurations or host system setting.

*Sequential performance is based on CrystalDiskMark 5.2.1 with file size 1,000MB.

**Random performance measured using IOMeter with Queue Depth 32.

2.5 Electrical Specifications

Table 2-4 Operating Voltage

Symbol	Parameter	Min.	Max.	Unit
V _{DD}	Power Supply Voltage	2.7	3.6	V

Table 2-5 Power Consumption

Capacity	8 GB	16 GB
Active (mA)	105	150
Idle (mA)	235	315

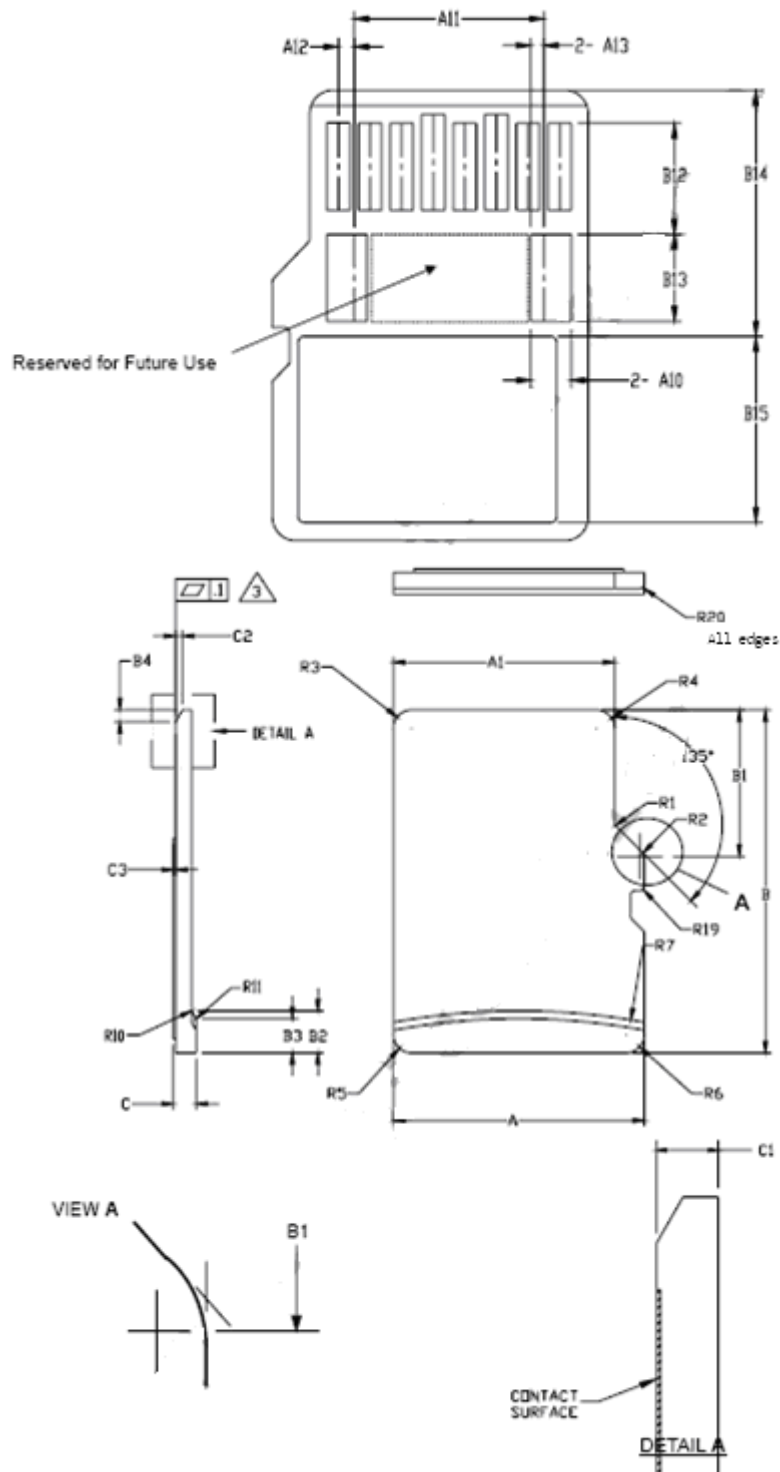
Note:

*All values are typical and may vary depending on flash configurations or host system settings.

**Active power is an average power measurement performed using CrystalDiskMark with 128KB sequential read/write transfers.


3. Physical Characteristics

3.1 Physical Dimensions



SYMBOL	COMMON DIMENSIONS			NOTE
	MIN	NOM	MAX	
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.80	-	-	
A10	1.35	1.40	1.45	
A11	6.50	6.60	6.70	
A12	0.50	0.55	0.60	
A13	0.40	0.45	0.50	
B	14.90	15.00	15.10	
B1	6.30	6.40	6.50	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	5.50	-	-	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	-	-	9.00	
B10	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
B12	3.60	3.70	3.80	
B13	2.80	2.90	3.00	
B14	8.20	-	-	
B15	-	-	6.20	
C	0.90	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	
D1	1.00	-	-	
D2	1.00	-	-	
D3	1.00	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.70	0.80	0.90	
R6	0.70	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	
R20	0.02	-	0.15	

Notes:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3.  COPLANARITY IS ADDITIVE TO C1 MAX THICKNESS.

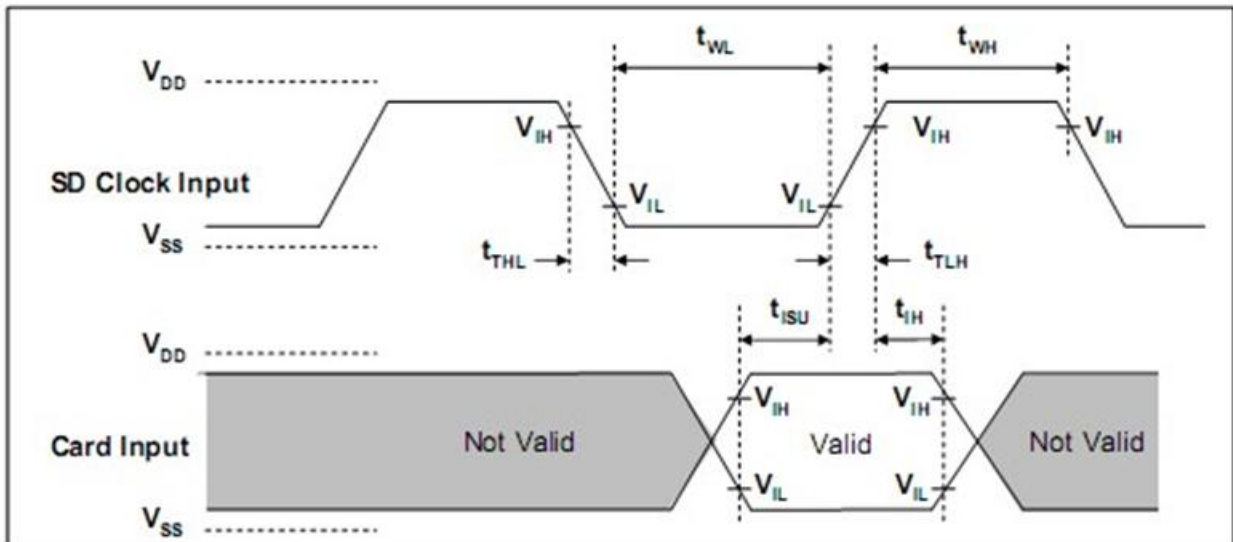
3.2 Durability Specifications

Table 3-1 Durability Specifications

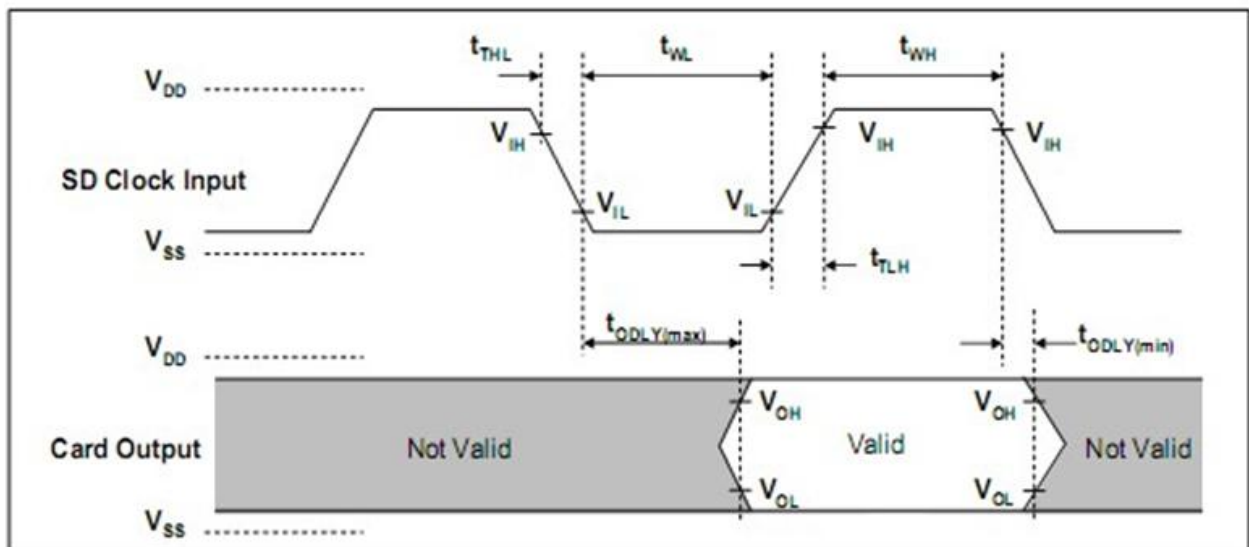
Item	Specifications
Temperature	-25°C to 85°C (Operating)
	-40°C to 85°C (Storage)
Shock	1,500G, 0.5ms
Vibration	20Hz~80Hz/1.52mm (frequency/displacement) 80Hz~2000Hz/20G (frequency/displacement) X, Y, Z axis/60mins each
Humidity	85% RH 85°C, 1,000 hrs
Drop	150cm free fall, 6 face of each
Bending	≥ 10N, hold 1min/5times
Torque	0.1N-m or 2.5deg, hold 5min/5times
Salt spray	Concentration: 3% NaCl at 35°C (storage for 24 hours)
Waterproof	JIS IPX7 compliance Water temperature 25°C Water depth: the lowest point of unit is locating 1000mm below surface (storage for 30 mins)
X-Ray Exposure	0.1 Gy of medium-energy radiation (70 KeV to 140 KeV, cumulative dose per year) to both sides of the card (storage for 30 mins)
Durability	10,000 times mating cycle
ESD	IEC 61000-4-2 & SDA spec

4. AC Characteristics

4.1 MicroSD Interface Timing (Default)



Card input Timing (Default Speed Card)

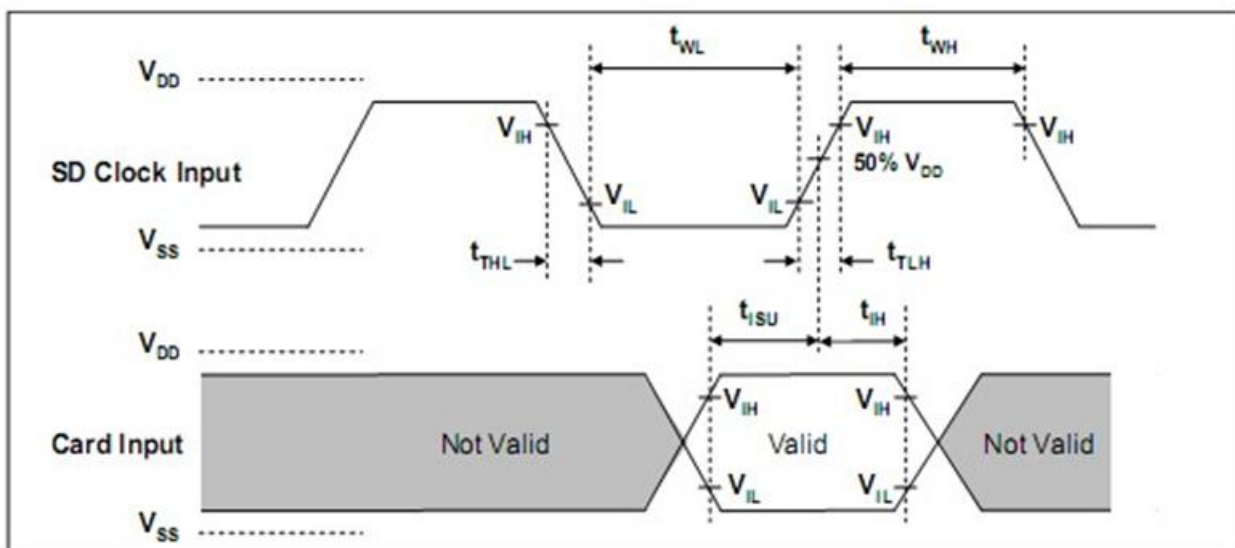


Card Output Timing (Default Speed Mode)

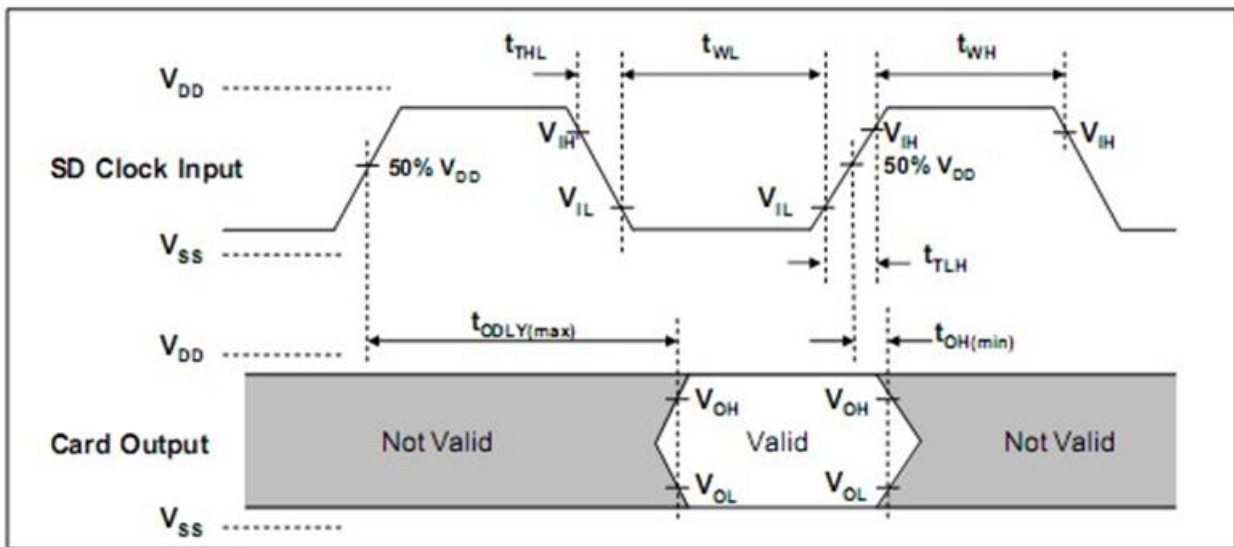
SYMBOL	PARAMETER	MIN	MAX	UNIT	REMARK
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
f _{PP}	Clock frequency data transfer	0	25	MHz	C _{card} ≤ 10 pF (1 card)
f _{OD}	Clock frequency identification	0 ⁽¹⁾ /100	400	KHz	C _{card} ≤ 10 pF (1 card)
t _{WL}	Clock low time	10	-	ns	C _{card} ≤ 10 pF (1 card)
t _{WH}	Clock high time	10	-	ns	C _{card} ≤ 10 pF (1 card)
t _{TLH}	Clock rise time	-	10	ns	C _{card} ≤ 10 pF (1 card)
t _{THL}	Clock fall time	-	10	ns	C _{card} ≤ 10 pF (1 card)
Inputs CMD, DAT (Referenced to CLK)					
t _{ISU}	Input setup time	5	-	ns	C _{card} ≤ 10 pF (1 card)
t _{TH}	Input hold time	5	-	ns	C _{card} ≤ 10 pF (1 card)
Outputs CMD, DAT (Referenced to CLK)					
t _{ODLY}	Output delay time during data transfer mode	0	14	ns	C _L ≤ 40 pF (1 card)
t _{OH}	Output hold time	0	50	ns	C _L ≤ 40 pF (1 card)

(1)0Hz means to stop the clock. The given minimum frequency range is for cases that require the clock to be continued.

4.2 MicroSD Interface Timing (High Speed Mode)



Card Input Timing (High Speed Card)



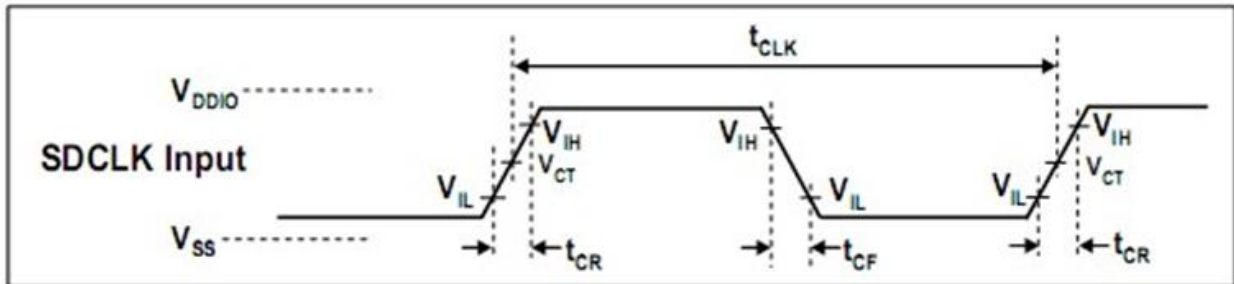
Card Output Timing (High Speed Mode)

SYMBOL	PARAMETER	MIN	MAX	UNIT	REMARK
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
f_{PP}	Clock frequency data transfer	0	50	MHz	$C_{card} \leq 10$ pF (1 card)
t_{WL}	Clock low time	7	-	ns	$C_{card} \leq 10$ pF (1 card)
t_{WH}	Clock high time	7	-	ns	$C_{card} \leq 10$ pF (1 card)
t_{TLH}	Clock rise time	-	3	ns	$C_{card} \leq 10$ pF (1 card)
t_{THL}	Clock fall time	-	3	ns	$C_{card} \leq 10$ pF (1 card)
Inputs CMD, DAT (Referenced to CLK)					
t_{ISU}	Input setup time	6	-	ns	$C_{card} \leq 10$ pF (1 card)
t_{TH}	Input hold time	2	-	ns	$C_{card} \leq 10$ pF (1 card)
Outputs CMD, DAT (Referenced to CLK)					
t_{ODLY}	Output delay time during data transfer made	-	14	ns	$CL \leq 40$ pF (1 card)
t_{OH}	Output hold time	2.5	-	ns	$CL \geq 15$ pF (1 card)
C_L	Total system capacitance for each line*	-	40	pF	1 card

*In order to satisfy severe timing, host shall run on only one card

4.3 MicroSD Interface Timing (SDR12, SDR25, SDR50 and SDR104 Modes) Input

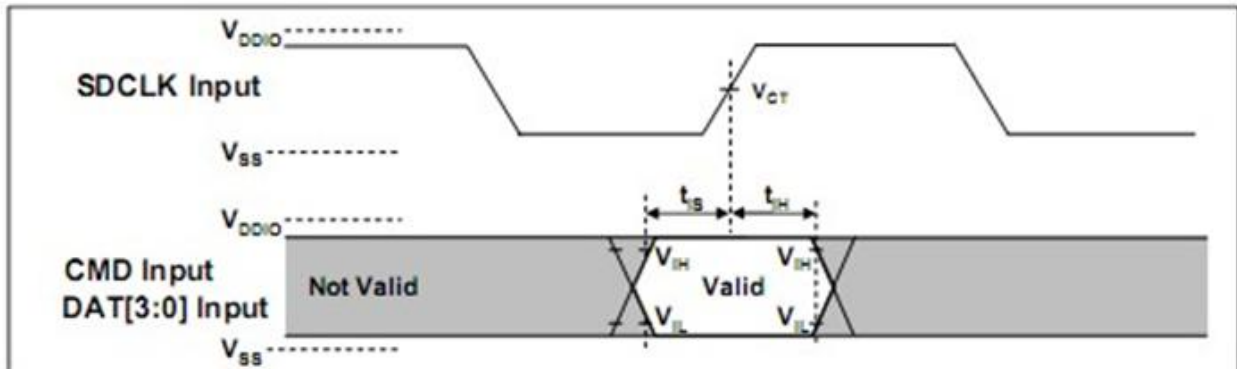
4.3.1 Clock Timing



Clock Signal Timing

SYMBOL	MIN	MAX	UNIT	REMARK
t_{CLK}	4.8	-	ns	208MHz (Max.), Between rising edge, $V_{CT} = 0.975V$
t_{CR}, t_{CF}	-	$0.2 * t_{CLK}$	ns	$t_{CR}, t_{CF} < 2.00ns$ (max.) at 208MHz, $C_{CARD}=10pF$ $t_{CR}, t_{CF} < 2.00ns$ (max.) at 100MHz, $C_{CARD}=10pF$ The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	

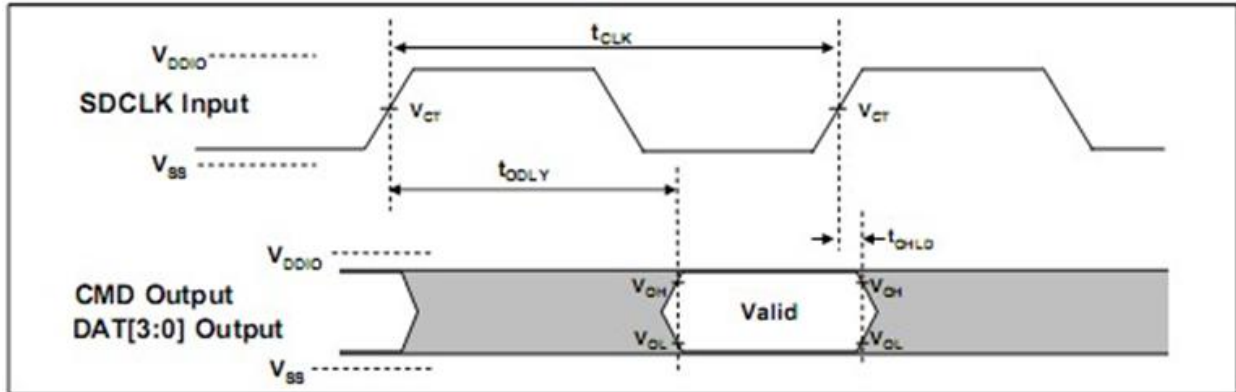
4.3.2 Card Input Timing



Card Input Timing

SYMBOL	MIN	MAX	UNIT	SDR104 MODE
t_{IS}	1.40	-	ns	$C_{CARD} = 10pF, V_{CT} = 0.975V$
t_{IH}	0.80	-	ns	$C_{CARD} = 5pF, V_{CT} = 0.975V$
SYMBOL	MIN	MAX	UNIT	SDR12, SDR25 and SDR50 MODES
t_{IS}	3.00	-	ns	$C_{CARD} = 10pF, V_{CT} = 0.975V$
t_{IH}	0.80	-	ns	$C_{CARD} = 5pF, V_{CT} = 0.975V$

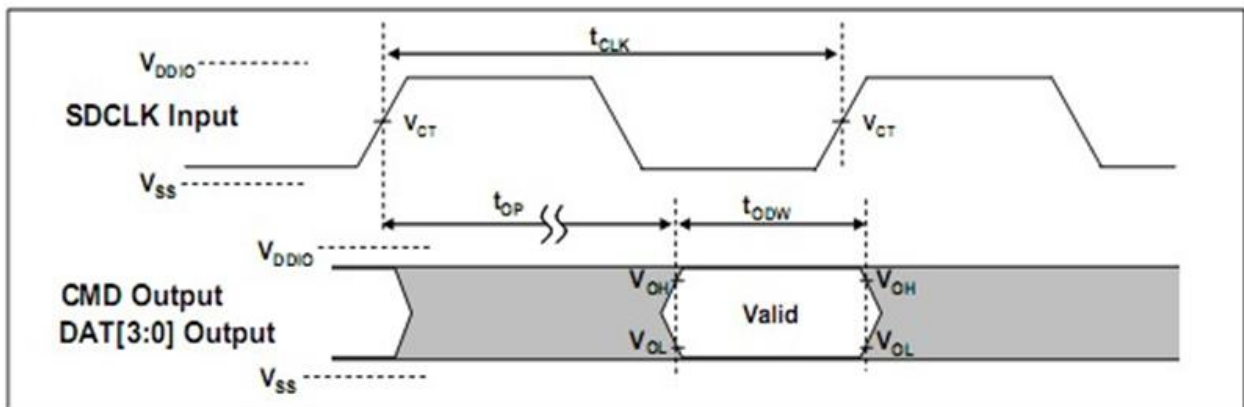
4.3.3 Card Output Timing of Fixed Data Window (SDR12, SDR25 and SDR50)



Output Timing of Fixed Date Window⁴⁾

SYMBOL	MIN	MAX	UNIT	REMARK
t_{ODLY}	-	7.5	ns	$t_{CLK} \geq 10.0\text{ns}$, $CL=30\text{pF}$, using driver Type B, for SDR50.
t_{ODLY}		14	ns	$t_{CLK} \geq 20.0\text{ns}$, $CL=40\text{pF}$, using driver Type B, for SDR25 and SDR12.
t_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.). $CL=15\text{pF}$

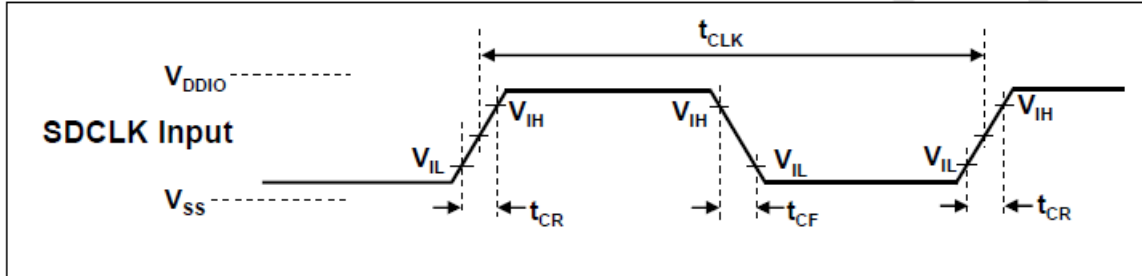
4.3.4 Output Timing of Variable Window (SDR104)



Output Timing of Variable Data Window⁴⁾

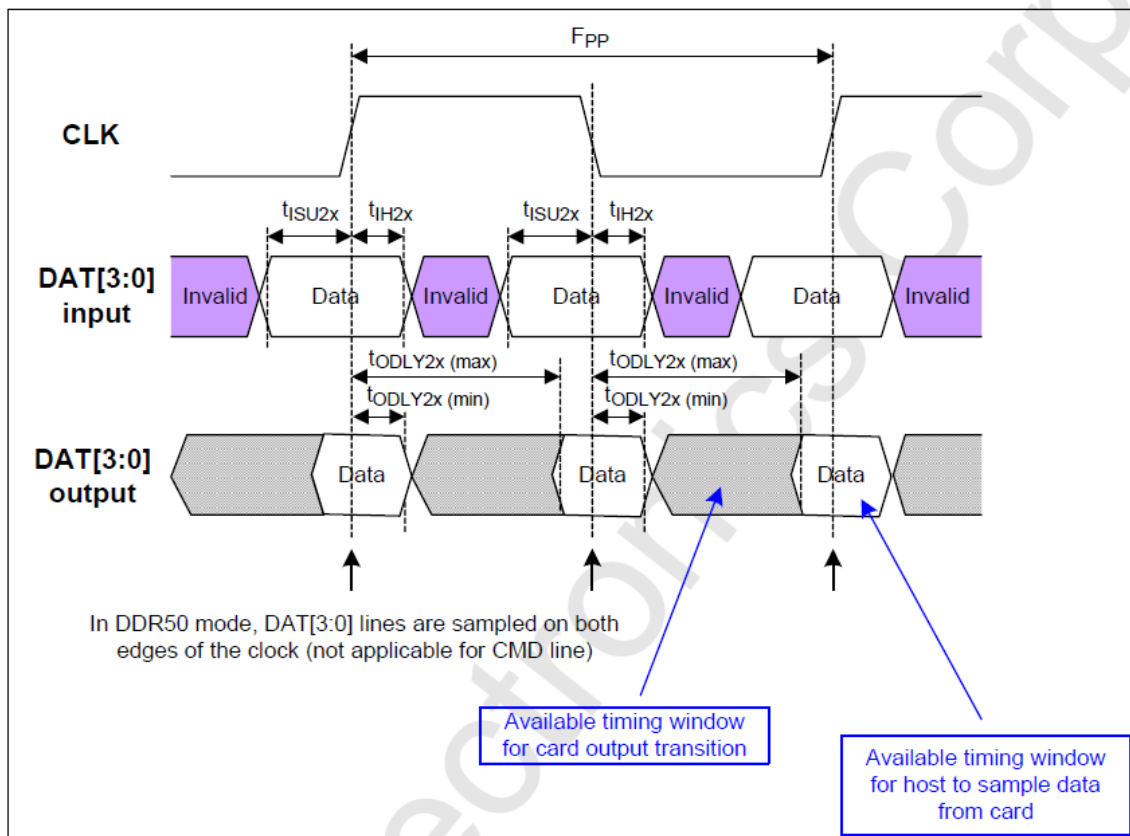
SYMBOL	MIN	MAX	UNIT	REMARK
t_{OP}	-	2	UI	Card Output Phase
Δt_{OP}	-350	+1550	ps	Delay variation due to temperature change after tuning
t_{ODW}	0.60	-	UI	$t_{ODW} = 2.88\text{ns}$ at 208MHz

4.3.5 SD Interface Timing (DDR50 Mode)



Clock Signal Timing

SYMBOL	MIN	MAX	UNIT	REMARK
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	$0.2 * t_{CLK}$	ns	$t_{CR}, t_{CF} < 4.00ns$ (max.) at 50MHz, CCARD=10pF
Clock Duty	45	55	%	



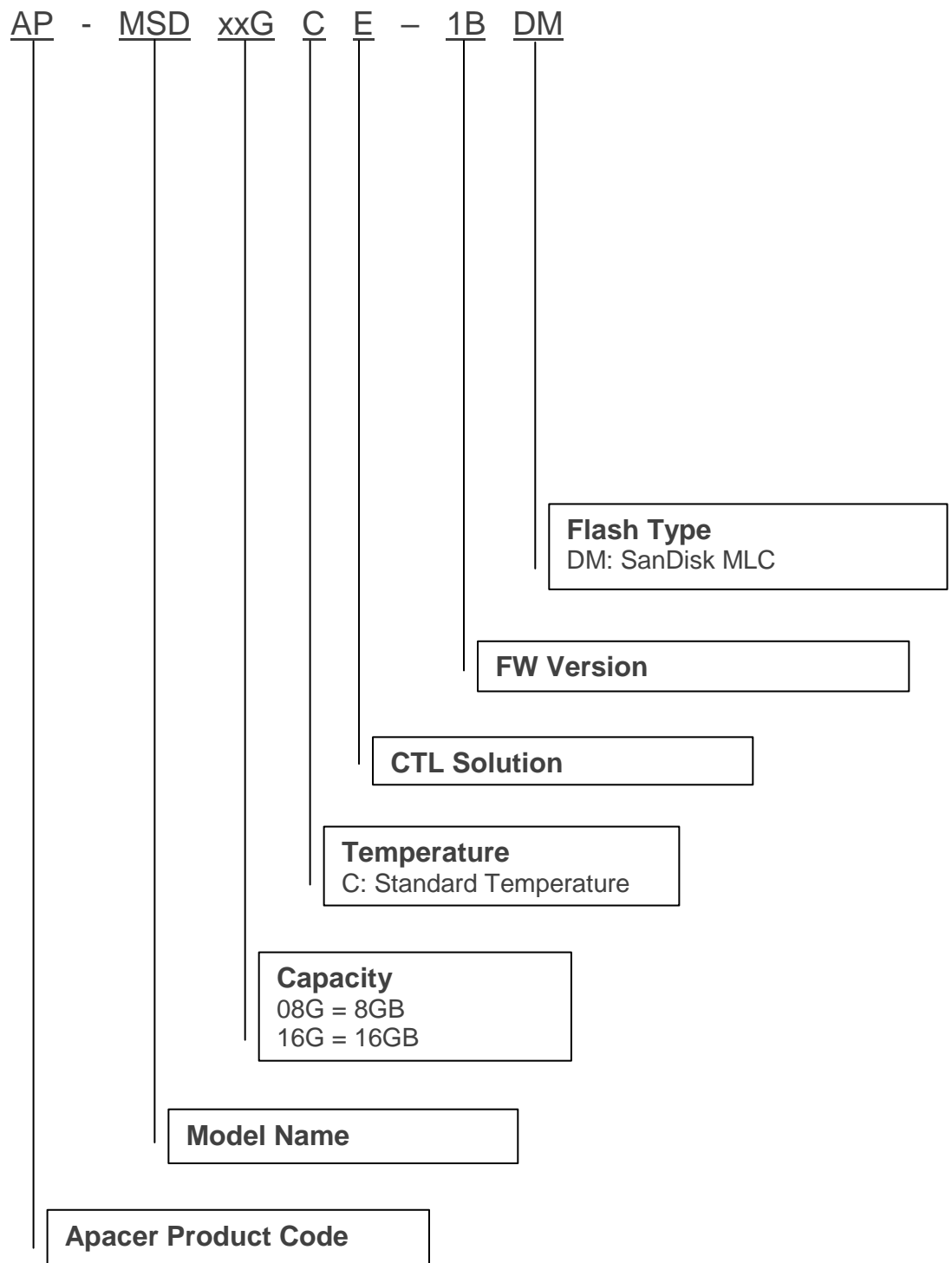
Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

4.3.6 Bus Timings – Parameters Values (DDR50 Mode)

Symbol	Parameters	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
t_{ISU}	Input set-up time	6	-	ns	$C_{card} \leq 10$ pF (1 card)
t_{IH}	Input hold time	0.8	-	ns	$C_{card} \leq 10$ pF (1 card)
Output CMD (referenced to CLK rising edge)					
t_{ODLY}	Output Delay time during Data Transfer Mode	-	13.7	ns	$C_L \leq 30$ pF (1 card)
T_{OH}	Output Hold time	1.5	-	ns	$C_L \geq 15$ pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
t_{ISU2x}	Input set-up time	3	-	ns	$C_{card} \leq 10$ pF (1 card)
t_{IH2x}	Input hold time	0.8	-	ns	$C_{card} \leq 10$ pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
t_{ODLY2x}	Output Delay time during Data Transfer Mode	-	7.0	ns	$C_L \leq 25$ pF (1 card)
T_{OH2x}	Output Hold time	1.5	-	ns	$C_L \geq 15$ pF (1 card)

5. Product Ordering Information

5.1 Product Code Designations



5.2 Valid Combinations

Capacity	Part Number
8GB	AP-MSD08GCE-1BDM
16GB	AP-MSD16GCE-1BDM

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Revision History

Revision	Date	Description	Remark
1.0	10/16/2017	Official release	

Global Presence

Taiwan (Headquarters)

Apacer Technology Inc.

1F., No.32, Zhongcheng Rd., Tucheng Dist.,
New Taipei City 236, Taiwan R.O.C.
Tel: 886-2-2267-8000
Fax: 886-2-2267-2261
amtsales@apacer.com

U.S.A.

Apacer Memory America, Inc.

46732 Lakeview Blvd., Fremont, CA 94538
Tel: 1-408-518-8699
Fax: 1-510-249-9551
sa@apacerus.com

Japan

Apacer Technology Corp.

5F, Matsura Bldg., Shiba, Minato-Ku
Tokyo, 105-0014, Japan
Tel: 81-3-5419-2668
Fax: 81-3-5419-0018
jpservices@apacer.com

Europe

Apacer Technology B.V.

Science Park Eindhoven 5051 5692 EB Son,
The Netherlands
Tel: 31-40-267-0000
Fax: 31-40-290-0686
sales@apacer.nl

China

Apacer Electronic (Shanghai) Co., Ltd

Room D, 22/FL, No.2, Lane 600, JieyunPlaza,
Tianshan RD, Shanghai, 200051, China
Tel: 86-21-6228-9939
Fax: 86-21-6228-9936
sales@apacer.com.cn

India

Apacer Technologies Pvt Ltd,

Unit No.201, "Brigade Corner", 7th Block
Jayanagar,
Yediyur Circle, Bangalore – 560082, India
Tel: 91-80-4152-9061
Fax: 91-80-4170-0215
sales_india@apacer.com