

RoHS Recast Compliant

Industrial MicroSD 3.0

MicroSDHC H1-SL Product Specifications
(Toshiba 15nm)

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Version 1.9



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Specifications Overview:

- **Fully Compatible with SD Card Association Specifications**
 - Part 1, Physical Layer Specification, Ver 3.01 Final
 - Part 2, File System Specification, Ver 3.00
 - Part 3, Security Specification, Ver 3.00 Final
- **Capacity**
 - 4, 8, 16, 32 GB
- **Performance***
 - Sequential read: Up to 90 MB/sec
 - Sequential write: Up to 80 MB/sec
- **Flash Management**
 - Built-in hardware ECC
 - Global Wear Leveling
 - Flash bad-block management
 - S.M.A.R.T.
 - Read Disturb Management
 - Power Failure Management
 - SLC-lite Technology
- **SD-Protocol Compatible**
- **Supports SD SPI Mode**
- **Backward Compatible with 2.0**
- **NAND Flash Type: MLC**
- **Firmware Version: SLC-Lite**
- **UHS-I Bus Speed Mode**
- **Temperature Range**
 - Operating:
 - Standard: -25°C to 85°C
 - Extended: -40°C to 85°C
 - Storage: -40°C to 100°C
- **Supply Voltage**
 - 2.7V ~ 3.6V
- **Power Consumption***
 - Operating: 140 mA
 - Standby: 270 μ A
- **Physical Dimensions :**
 - 15mm (L) x 11mm (W) x 1mm (H)
- **RoHS Recast Compliant**

*Varies from capacities. The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings.

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1. General Descriptions

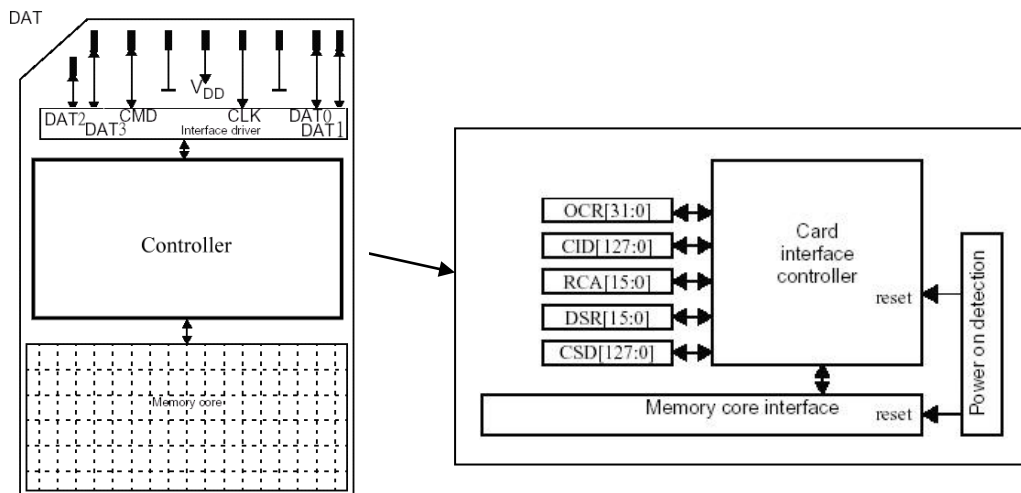
The Micro Secure Digital (MicroSD) card version 3.0 is fully compliant to the specification released by SD Card Association. The Command List supports [Part 1 Physical Layer Specification Ver3.01 Final] definitions. Card Capacity of Non-secure Area, Secure Area Supports [Part 3 Security Specification Ver3.00 Final] Specifications.

The MicroSD 3.0 card comes with 8-pin interface, designed to operate at optimal performance. It can alternate communication protocol between the SD mode and SPI mode. It performs data error detection and correction with very low power consumption.

Apacer Industrial micro Secure Digital 3.0 card is ideal for its high performance and wide compatibility. Not to mention that it's well adapted for hand-held applications in semi-industrial/medical markets already. In regard of reliability, Apacer MicroSD H1-SL comes with Apacer's SLC-lite technology, enhanced P/E cycles up to 20,000 times, and various implementations including powerful hardware ECC engine, wear leveling and flash block management.

1.1 Functional Block

The MicroSD contains a card controller and a memory core for the SD standard interface.



1.2 Flash Management

1.2.1 Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. Apacer implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

1.2.2 Powerful ECC Algorithms

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, the MicroSD card applies the BCH ECC Algorithm, which can detect and correct errors occur during read process, ensure data been read correctly, as well as protect data from corruption.

1.2.3 Global Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some area get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Global Wear Leveling technique is applied to extend the lifespan of NAND Flash by evenly distributing writes and erase cycles across the media.

Apacer provides Global Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing Global Wear Leveling algorithm, the life expectancy of the NAND Flash is greatly improved.

1.2.4 S.M.A.R.T.

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is a special function that allows a memory device to automatically monitor its health. Apacer provides a program named SmartInfo Tool to observe Apacer’s SD and MicroSD cards. Note that this tool can only support Apacer’s industrial SD and MicroSD cards. This tool will display firmware version, endurance life ratio, good block ratio, and so forth.

1.2.5 Read Disturb Management

When continuously being read, NAND flash memory cannot engage wear leveling since this applies while writing data. Subsequently, errors aggregated over time and become uncorrectable. To keep errors from going beyond ECC’s capability to recover and memory blocks in good hands, Apacer’s Auto-Read Refresh will spontaneously refresh the bit errors when the threshold is triggered by the error count in a block.

1.2.6 Power Failure Management

Apacer industrial SD and MicroSD cards provide complete data protection mechanism during every abnormal power shutdown situation, such as power failure at programming data, updating system tables, erasing blocks, etc. Apacer Power-Loss Protection mechanism includes:

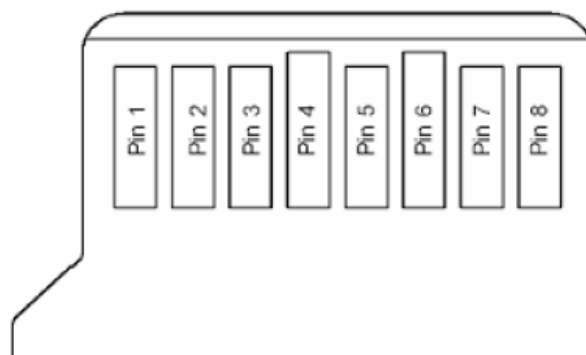
- Maintaining data correctness and increasing the reliability of the data stored in the NAND Flash memory.
- Protecting F/W table and the data written to flash from data loss in the event of power off.

1.2.7 SLC-lite Technology

SLC-lite is Apacer's proprietary technology that strikes a cost-performance balance between MLC and SLC flash types and it is an ideal alternative solution for mission-critical embedded or industrial applications. It utilizes the infrastructure of MLC flash together with the special firmware to simulate the performance and durability of industrial grade flash SLC, which enable the maximum endurance, retention and performance but lower cost.

2. Electrical Characteristics

2.1 Card Architecture



2.2 Pin Assignment

Table 2-1 Pin Descriptions

Pin	SD Mode		SPI Mode	
	Name	Description	Name	Description
1	DAT2	Data line[bit 2]	Reserved	
2	CD/DAT3	Card Detect/Data line [bit 3]	CS	Chip select
3	CMD	Command/Response	DI	Data in
4	VDD	Supply voltage	VDD	Supply voltage
5	CLK	Clock	SCLK	Clock
6	VSS	Supply voltage ground	VSS	Supply voltage ground
7	DAT0	Data line[bit 0]	DO	Data out
8	DAT1	Data line[bit 1]	Reserved	

2.3 Capacity

Capacity specifications of the SD 3.0 card are available as shown in Table 2-2. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

Table 2-2 Capacity Specifications

Capacity	Total bytes*
4 GB	3,972,005,888
8 GB	7,960,788,992
16 GB	16,013,852,672
32 GB	32,094,814,208

Note: Total bytes are viewed under Windows operating system and were measured by SD format too.

2.4 Performance

Performance of the SD 3.0 card is listed below in Table 2-3.

Table 2-3 Performance Specifications

Capacity	4 GB	8 GB	16 GB	32 GB
Performance				
Sequential Read* (MB/s)	90	90	90	90
Sequential Write* (MB/s)	75	75	75	80

Note:

Results may differ from various flash configurations or host system setting.

*Sequential performance is based on CrystalDiskMark 5.2.1 with file size 1,000MB.

2.5 Operating Voltage

Table 2-4 lists the supply voltage for the SD 3.0 card.

Table 2-4 Operating Range

Symbol	Parameter	Min.	Max.	Unit
V _{DD}	Power Supply Voltage	2.7	3.6	V

2.6 Power Consumption

Table 2-5 lists the power consumption for the SD 3.0 card.

Table 2-5 Power Consumption

Capacity	4 GB	8 GB	16 GB	32 GB
Mode				
Operating (mA)	110	110	135	140
Standby (µA)	195	220	250	270

Note:

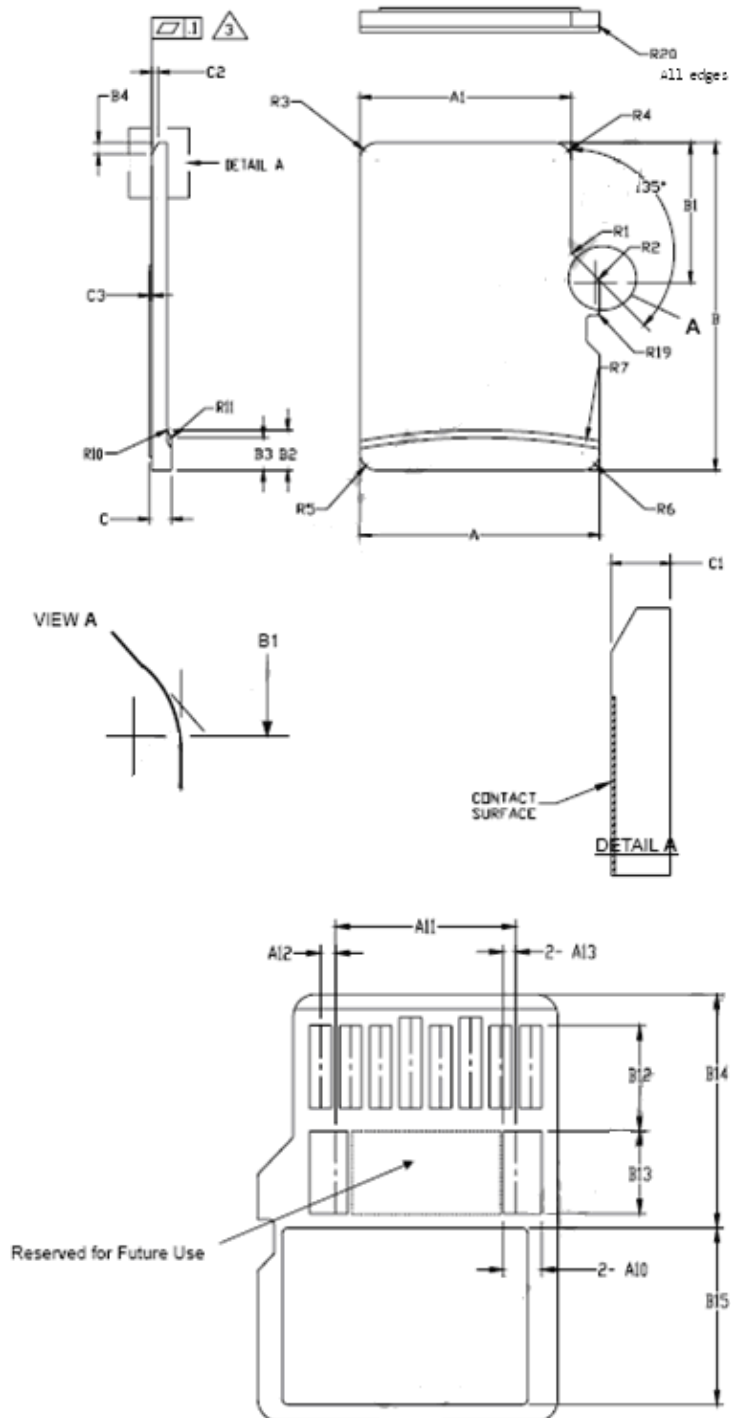
*All values are typical and may vary depending on flash configurations or host system settings.

**Active power is an average power measurement performed using CrystalDiskMark with 128KB sequential read/write transfers.

***Power is measured based on USB 3.0 card reader.


3. Physical Characteristics

3.1 Physical Dimensions



SYMBOL	COMMON DIMENSIONS			NOTE
	MIN	NOM	MAX	
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.80	-	-	
A10	1.35	1.40	1.45	
A11	6.50	6.60	6.70	
A12	0.50	0.55	0.60	
A13	0.40	0.45	0.50	
B	14.90	15.00	15.10	
B1	6.30	6.40	6.50	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	5.50	-	-	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	-	-	9.00	
B10	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
B12	3.60	3.70	3.80	
B13	2.80	2.90	3.00	
B14	8.20	-	-	
B15	-	-	6.20	
C	0.90	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	
D1	1.00	-	-	
D2	1.00	-	-	
D3	1.00	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.70	0.80	0.90	
R6	0.70	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	
R20	0.02	-	0.15	

Notes:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3.  COPLANARITY IS ADDITIVE TO C1 MAX THICKNESS.

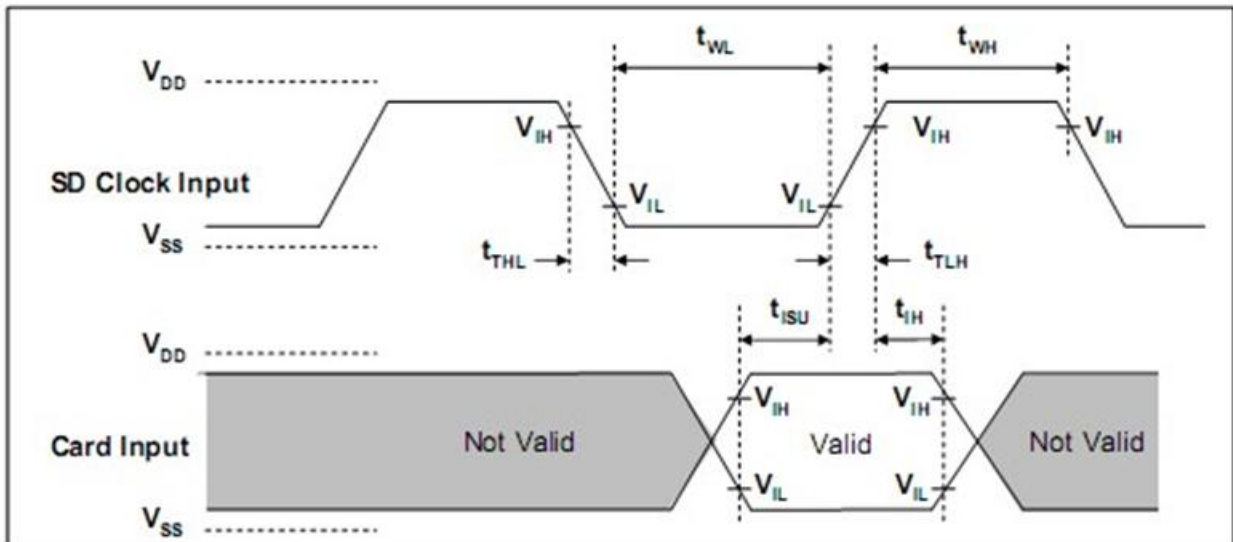
3.2 Durability Specifications

Table 3-1 Durability Specifications

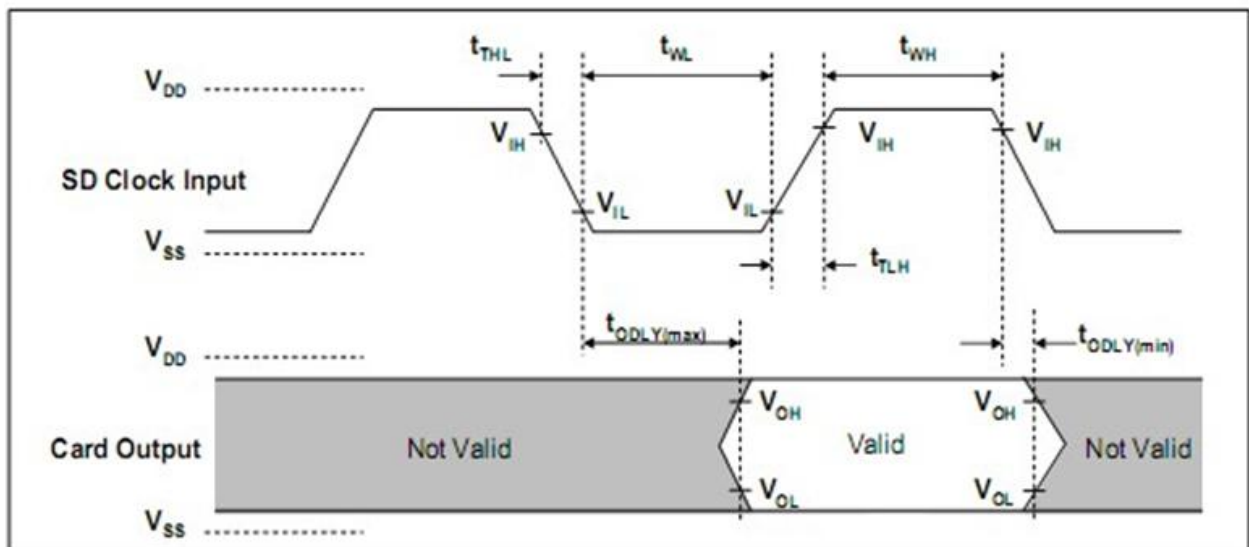
Environment	Specifications
Temperature	-25°C to 85°C (Operating) -40°C to 85°C (Extended)
	-40°C to 100°C (Storage)
Shock	1,500G, 0.5ms
Vibration	20Hz~80Hz/1.52mm (frequency/displacement) 80Hz~2000Hz/20G (frequency/displacement) X, Y, Z axis/60mins each
Drop	150cm free fall, 6 face of each
Bending	≥ 10N, hold 1min/5times
Torque	0.1N-m or 2.5deg, hold 5min/5times
Salt spray	Concentration: 3% NaCl at 35°C (storage for 24 hours)
Waterproof	JIS IPX7 compliance Water temperature 25°C Water depth: the lowest point of unit is locating 1000mm below surface (storage for 30 mins)
X-Ray Exposure	0.1 Gy of medium-energy radiation (70 KeV to 140 KeV, cumulative dose per year) to both sides of the card (storage for 30 mins)
Switch cycle	0.4~0.5N, 1000 times
Durability	10,000 times mating cycle
ESD	Pass

4. AC Characteristics

4.1 MicroSD Interface Timing (Default)



Card input Timing (Default Speed Card)

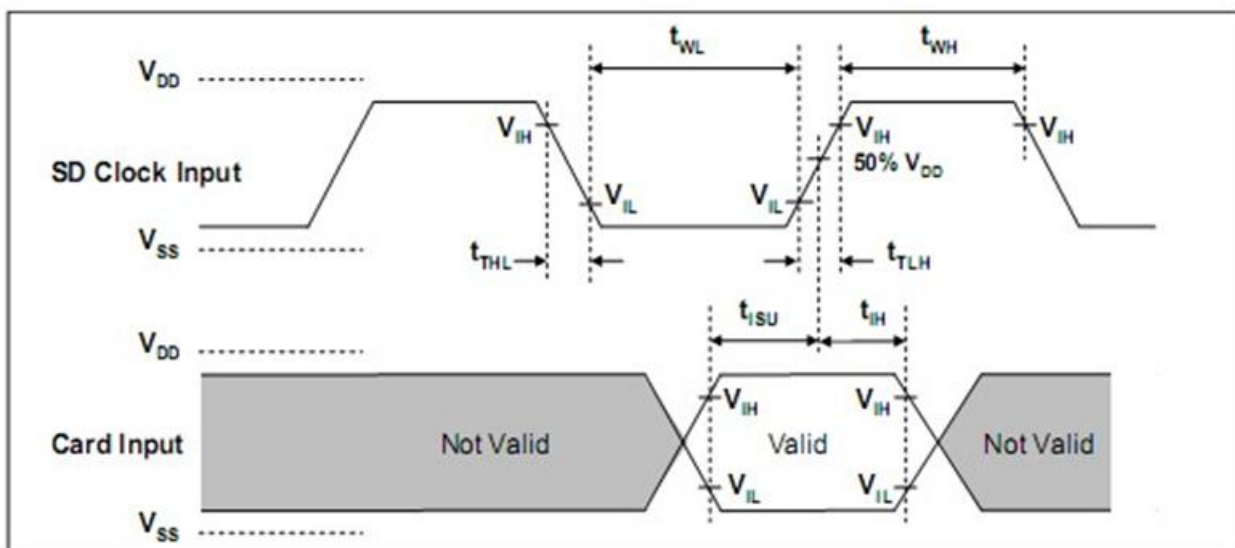


Card Output Timing (Default Speed Mode)

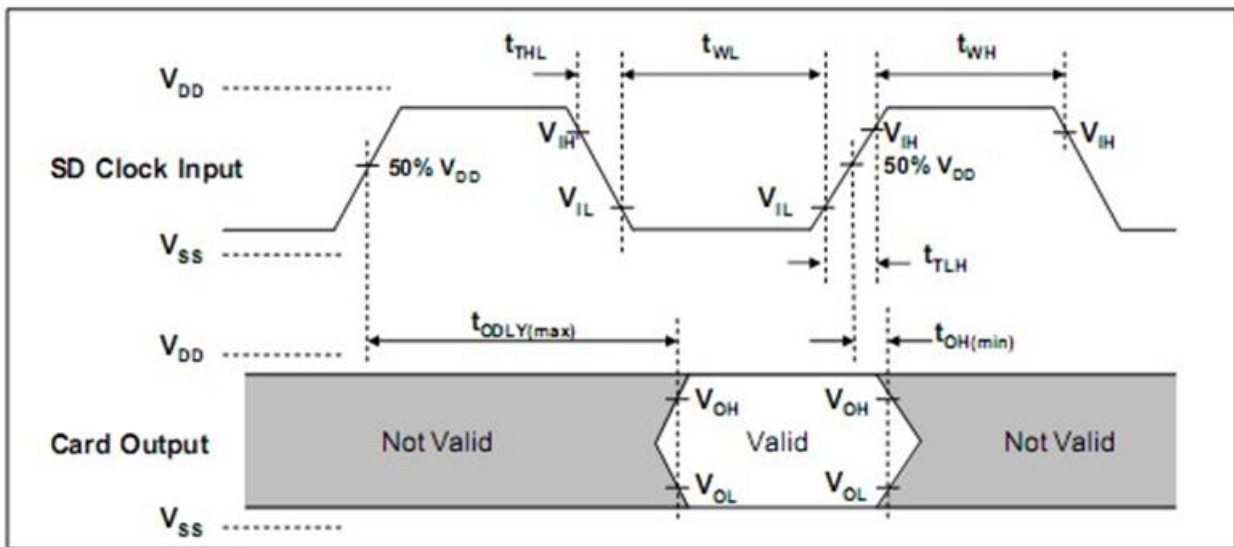
SYMBOL	PARAMETER	MIN	MAX	UNIT	REMARK
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
f _{PP}	Clock frequency data transfer	0	25	MHz	C _{card} ≤ 10 pF (1 card)
f _{OD}	Clock frequency identification	0 ⁽¹⁾ /100	400	KHz	C _{card} ≤ 10 pF (1 card)
t _{WL}	Clock low time	10	-	ns	C _{card} ≤ 10 pF (1 card)
t _{WH}	Clock high time	10	-	ns	C _{card} ≤ 10 pF (1 card)
t _{TLH}	Clock rise time	-	10	ns	C _{card} ≤ 10 pF (1 card)
t _{THL}	Clock fall time	-	10	ns	C _{card} ≤ 10 pF (1 card)
Inputs CMD, DAT (Referenced to CLK)					
t _{ISU}	Input setup time	5	-	ns	C _{card} ≤ 10 pF (1 card)
t _{TH}	Input hold time	5	-	ns	C _{card} ≤ 10 pF (1 card)
Outputs CMD, DAT (Referenced to CLK)					
t _{ODLY}	Output delay time during data transfer mode	0	14	ns	C _L ≤ 40 pF (1 card)
t _{OH}	Output hold time	0	50	ns	C _L ≤ 40 pF (1 card)

(1)0Hz means to stop the clock. The given minimum frequency range is for cases that require the clock to be continued.

4.2 MicroSD Interface Timing (High Speed Mode)



Card Input Timing (High Speed Card)



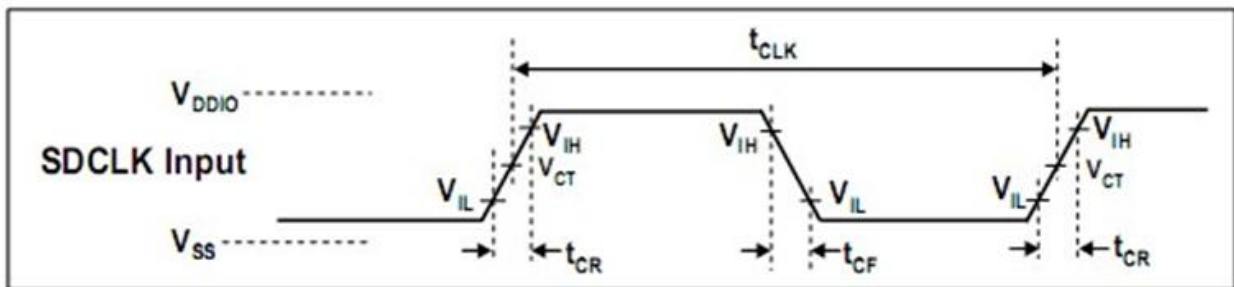
Card Output Timing (High Speed Mode)

SYMBOL	PARAMETER	MIN	MAX	UNIT	REMARK
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
f _{PP}	Clock frequency data transfer	0	50	MHz	C _{card} ≤ 10 pF (1 card)
t _{WL}	Clock low time	7	-	ns	C _{card} ≤ 10 pF (1 card)
t _{WH}	Clock high time	7	-	ns	C _{card} ≤ 10 pF (1 card)
t _{TLH}	Clock rise time	-	3	ns	C _{card} ≤ 10 pF (1 card)
t _{THL}	Clock fall time	-	3	ns	C _{card} ≤ 10 pF (1 card)
Inputs CMD, DAT (Referenced to CLK)					
t _{ISU}	Input setup time	6	-	ns	C _{card} ≤ 10 pF (1 card)
t _{TH}	Input hold time	2	-	ns	C _{card} ≤ 10 pF (1 card)
Outputs CMD, DAT (Referenced to CLK)					
t _{ODLY}	Output delay time during data transfer made	-	14	ns	CL ≤ 40 pF (1 card)
t _{OH}	Output hold time	2.5	-	ns	CL ≥ 15 pF (1 card)
C _L	Total system capacitance for each line*	-	40	pF	1 card

*In order to satisfy severe timing, host shall run on only one card

4.3 MicroSD Interface Timing (SDR12, SDR25, SDR50 and SDR104 Modes) Input

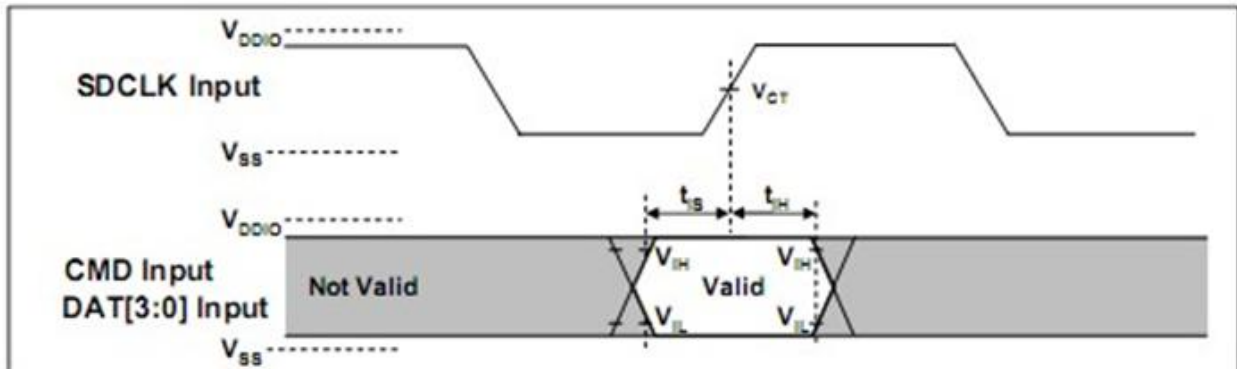
4.3.1 Clock Timing



Clock Signal Timing

SYMBOL	MIN	MAX	UNIT	REMARK
t_{CLK}	4.8	-	ns	208MHz (Max.), Between rising edge, $V_{CT} = 0.975V$
t_{CR}, t_{CF}	-	$0.2 * t_{CLK}$	ns	$t_{CR}, t_{CF} < 2.00ns$ (max.) at 208MHz, $C_{CARD}=10pF$ $t_{CR}, t_{CF} < 2.00ns$ (max.) at 100MHz, $C_{CARD}=10pF$ The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	

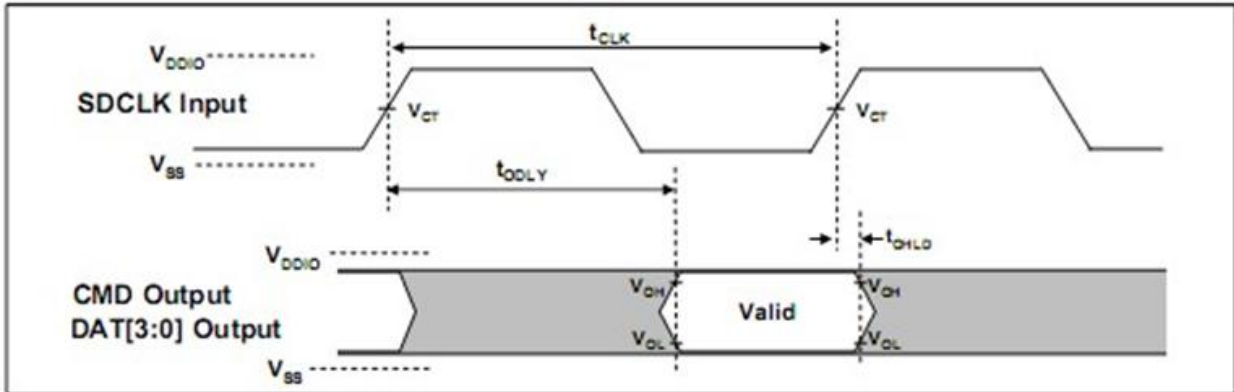
4.3.2 Card Input Timing



Card Input Timing

SYMBOL	MIN	MAX	UNIT	SDR104 MODE
t_{IS}	1.40	-	ns	$C_{CARD} = 10pF, V_{CT} = 0.975V$
t_{IH}	0.80	-	ns	$C_{CARD} = 5pF, V_{CT} = 0.975V$
SYMBOL	MIN	MAX	UNIT	SDR12, SDR25 and SDR50 MODES
t_{IS}	3.00	-	ns	$C_{CARD} = 10pF, V_{CT} = 0.975V$
t_{IH}	0.80	-	ns	$C_{CARD} = 5pF, V_{CT} = 0.975V$

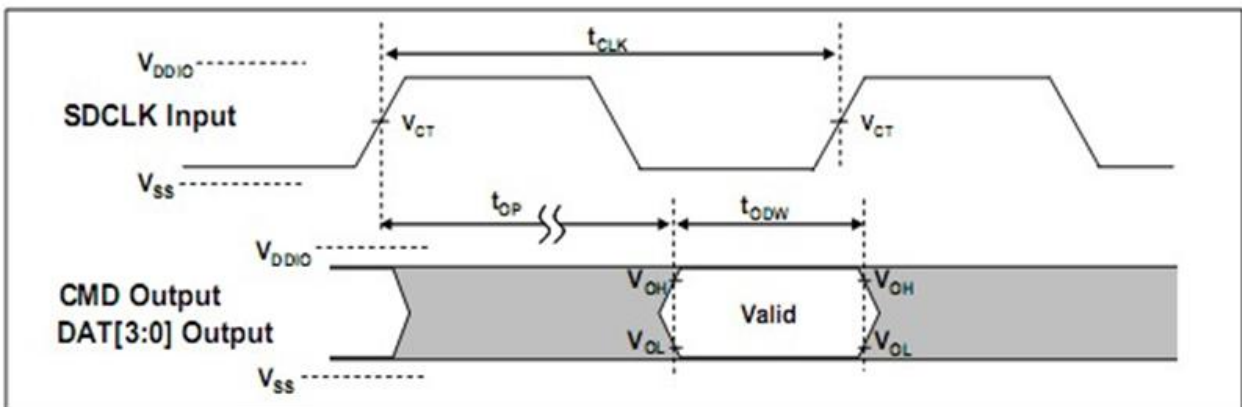
4.3.3 Card Output Timing of Fixed Data Window (SDR12, SDR25 and SDR50)



Output Timing of Fixed Date Window⁴⁾

SYMBOL	MIN	MAX	UNIT	REMARK
t_{ODLY}	-	7.5	ns	$t_{CLK} \geq 10.0\text{ns}$, $CL=30\text{pF}$, using driver Type B, for SDR50.
t_{ODLY}		14	ns	$t_{CLK} \geq 20.0\text{ns}$, $CL=40\text{pF}$, using driver Type B, for SDR25 and SDR12.
t_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.). $CL=15\text{pF}$

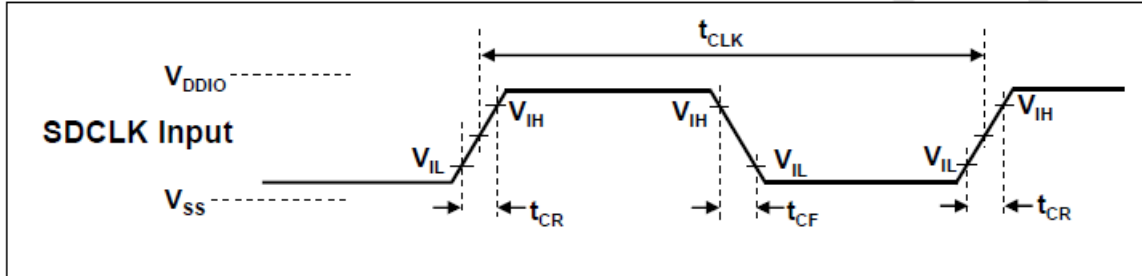
4.3.4 Output Timing of Variable Window (SDR104)



Output Timing of Variable Data Window⁴⁾

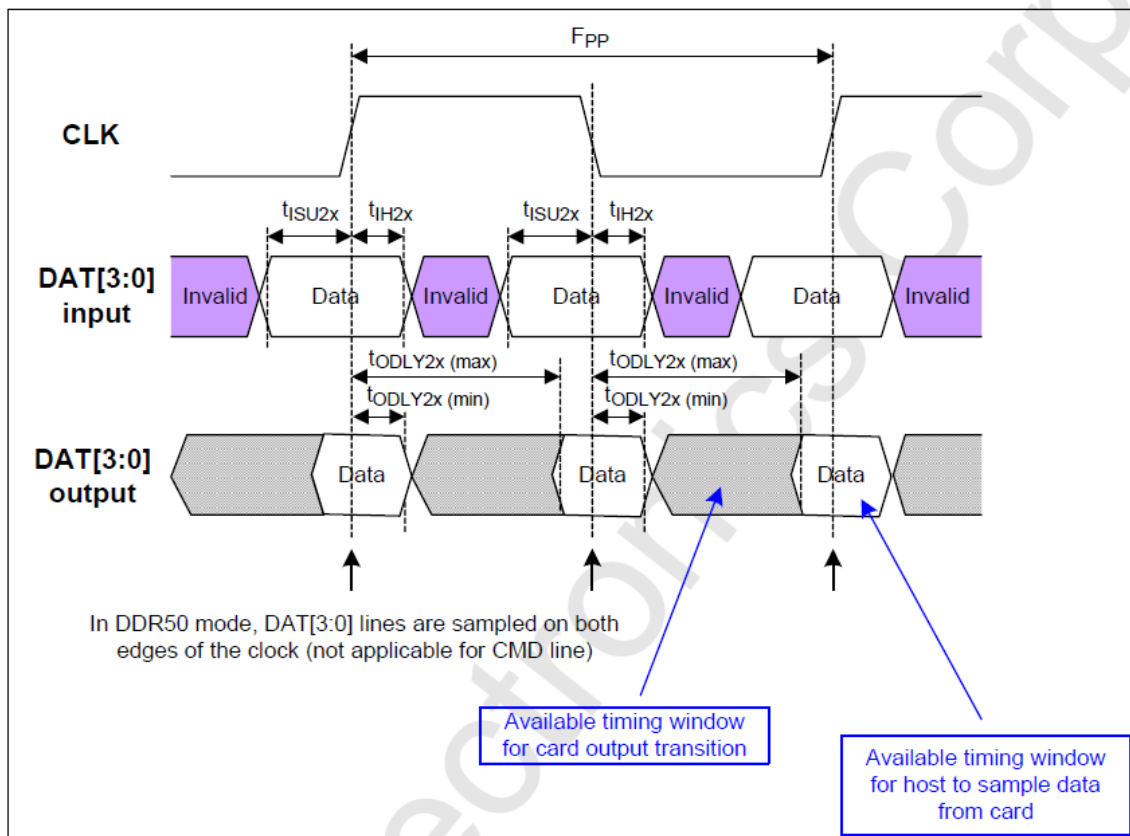
SYMBOL	MIN	MAX	UNIT	REMARK
t_{OP}	-	2	UI	Card Output Phase
Δt_{OP}	-350	+1550	ps	Delay variation due to temperature change after
t_{ODW}	0.60	-	UI	$t_{ODW} = 2.88\text{ns}$ at 208MHz

4.3.5 SD Interface Timing (DDR50 Mode)



Clock Signal Timing

SYMBOL	MIN	MAX	UNIT	REMARK
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	$0.2 * t_{CLK}$	ns	$t_{CR}, t_{CF} < 4.00ns$ (max.) at 50MHz, CCARD=10pF
Clock Duty	45	55	%	



Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

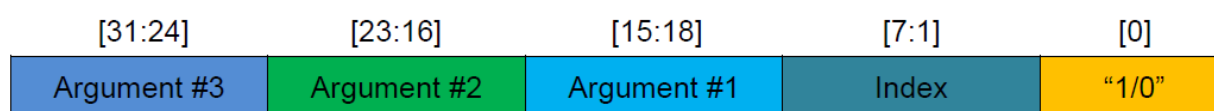
4.3.6 Bus Timings – Parameters Values (DDR50 Mode)

Symbol	Parameters	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
t_{ISU}	Input set-up time	6	-	ns	$C_{card} \leq 10$ pF (1 card)
t_{IH}	Input hold time	0.8	-	ns	$C_{card} \leq 10$ pF (1 card)
Output CMD (referenced to CLK rising edge)					
t_{ODLY}	Output Delay time during Data Transfer Mode	-	13.7	ns	$C_L \leq 30$ pF (1 card)
T_{OH}	Output Hold time	1.5	-	ns	$C_L \geq 15$ pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
t_{ISU2x}	Input set-up time	3	-	ns	$C_{card} \leq 10$ pF (1 card)
t_{IH2x}	Input hold time	0.8	-	ns	$C_{card} \leq 10$ pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
t_{ODLY2x}	Output Delay time during Data Transfer Mode	-	7.0	ns	$C_L \leq 25$ pF (1 card)
T_{OH2x}	Output Hold time	1.5	-	ns	$C_L \geq 15$ pF (1 card)

5. S.M.A.R.T.

5.1 Direct Host Access to SMART Data via SD General Command (CMD56)

CMD 56 is structured as a 32-bit argument. The implementation of the general purpose functions will arrange the CMD56 argument into the following format:



- Bit [0]: Indicates Read Mode when bit is set to [1] or Write Mode when bit is cleared [0]. Depending on the function, either Read Mode or Write Mode can be used.
- Bit [7:1]: Indicates the index of the function to be executed:
 - Read Mode: Index = 0x10 Get SMART Command Information
 - Write Mode: Index = 0x08 Pre-Load SMART Command Information
- Bit [15:8]: Function argument #1 (1-byte)
- Bit [23:16]: Function argument #2 (1-byte)
- Bit [31:24]: Function argument #3 (1-byte)

5.2 Process for Retrieving SMART Data

Retrieving SMART data requires the following two commands executed in sequence and in accordance with the SD Association standard flowchart for CMD56 (see below).

Step 1: Write Mode – [0x08] Pre-Load SMART Command Information

Sequence	Command	Argument	Expected Data
Pre-Load SMART Command Information	CMD56	[0] "0" (Write Mode) [1:7] "0001 000" (Index = 0x08) [8:511] All '0' (Reserved)	No expected data

Step 2: Read Mode – [0x10] Get SMART Command Information

Sequence	Command	Argument	Expected Data
Get SMART Command Information	CMD56		1 sector (512 bytes) of response data
		[0] "1" (Read Mode) [1:7] "0010 000" (Index = 0x10) [8:31] All '0' (Reserved)	byte[0-8] Flash ID byte[9-10] IC Version byte[11-12] FW Version byte[13] Reserved byte[14] CE Number byte[15] Reserved byte[16-17] Bad Block Replace Maximum byte[18] Reserved byte[32-63] Bad Block count per Die byte[64-65] Good Block Rate(%) byte[66-79] Reserved byte[80-83] Total Erase Count byte[84-95] Reserved byte[96-97] Endurance (Remain Life) (%) byte[98-99] Average Erase Count – L* byte[100-101] Minimum Erase Count – L* byte[102-103] Maximum Erase Count – L* byte[104-105] Average Erase Count – H* byte[106-107] Minimum Erase Count – H* byte[108-109] Maximum Erase Count – H* byte[110-111] Reserved byte[112-115] Power Up Count byte[116-127] Reserved byte[128-129] Abnormal Power Off Count byte[130-159] Reserved byte[160-161] Total Refresh Count byte[176-183] Product "Marker" byte[184-215] Bad Block count per Die byte[216-511] Reserved

*Please refer to technical note for High/Low byte definition.

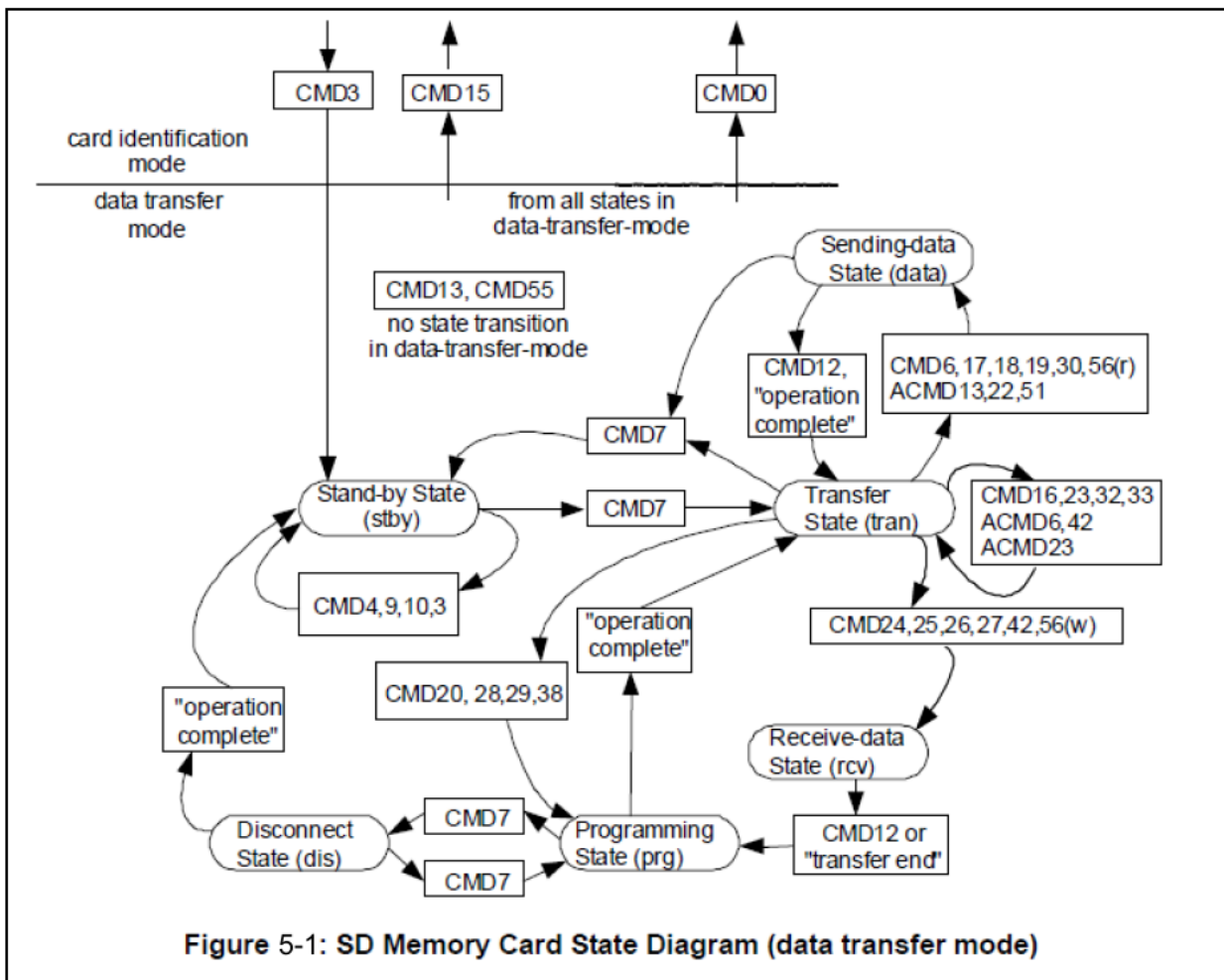
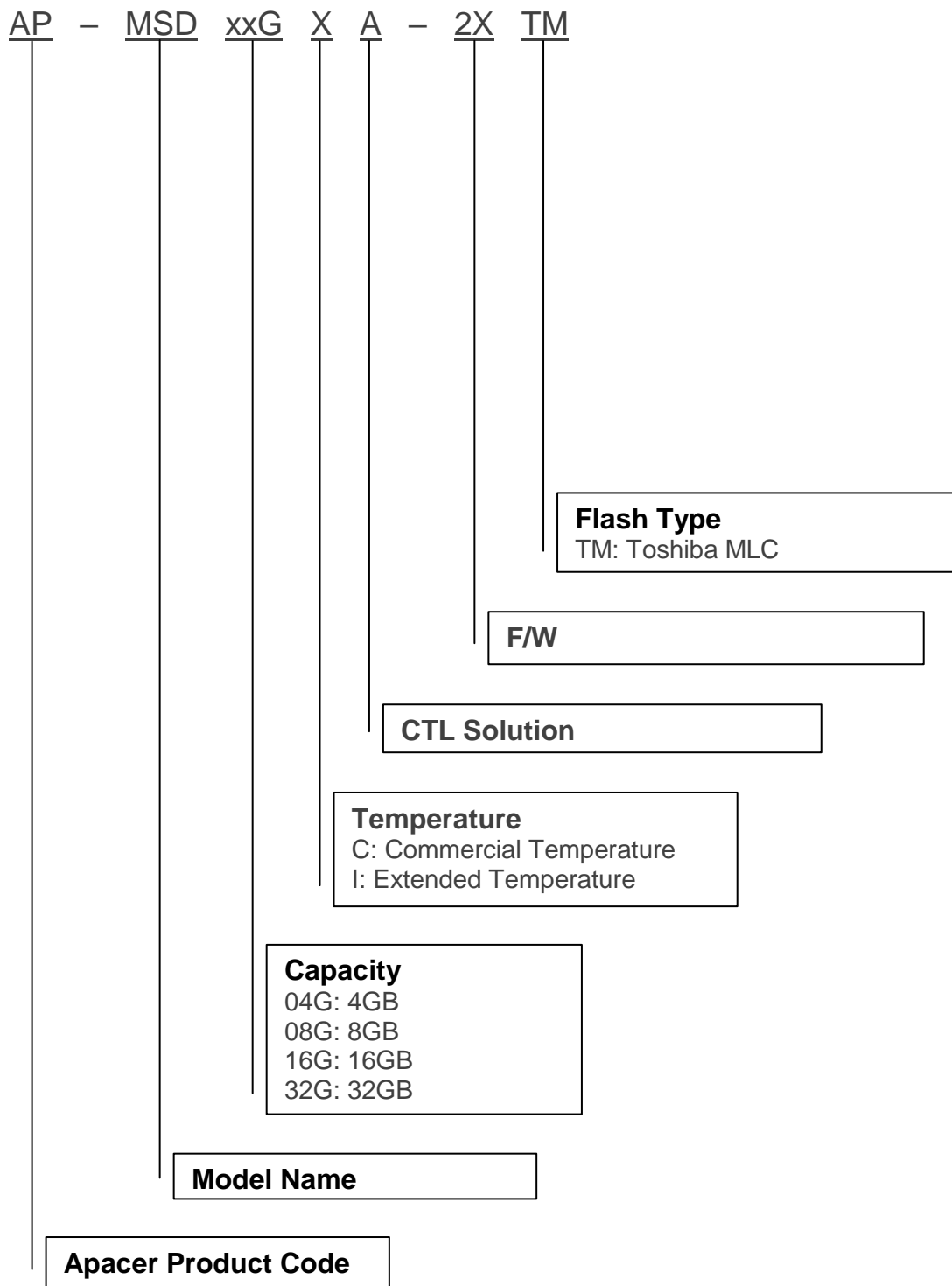


Figure 5-1: SD Memory Card State Diagram (data transfer mode)

Extracted from the SD Specifications Part 1 Physical Layer Simplified Specification Version 3.01.

6. Product Ordering Information

6.1 Product Code Designations



6.2 Valid Combinations

Capacity	Standard Temperature	Extended Temperature
4GB	AP-MSD04GCA-2HTM	AP-MSD04GIA-2HTM
8GB	AP-MSD08GCA-2HTM	AP-MSD08GIA-2HTM
16GB	AP-MSD16GCA-2HTM	AP-MSD16GIA-2HTM
32GB	AP-MSD32GCA-2FTM	AP-MSD32GIA-2FTM

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Revision History

Revision	Description	Date
1.0	Official release	3/17/2016
1.1	Revised product ordering information for 4GB-16GB due to FW change (82.105)	7/29/2016
1.2	Added Power Failure Management to Features and General Description	10/3/2016
1.3	Removed "The data written at the exact moment power off will be lost, and the max data loss is 16 sectors." from 1.2.5 Power Failure Management	10/7/2016
1.4	Modified the argument of Step 2: Read Mode – [0x10] Get SMART Command Information for S.M.A.R.T.	10/27/2016
1.5	- Updated 1. General Description - Added 1.2.6 SLC-Lite Technology	3/31/2017
1.6	Removed write protect support	7/31/2017
1.7	- Added Read Disturb Management to Flash Management on Features page - Added 1.2.5. Read Disturb Management - Updated performance and power consumption	9/26/2017
1.8	- Changed "Features" to "Specifications Overview" - Modified performance figures at Performance on Specifications Overview page	4/27/2018
1.9	Revised the capacity range given in Table 2-3 from 32-256GB to 4-32GB	5/18/2018

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