RoHS Compliant

Micro SDHC Card

SPI Mode Appendix

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Version 1.0

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SPI Bus Timing Diagram

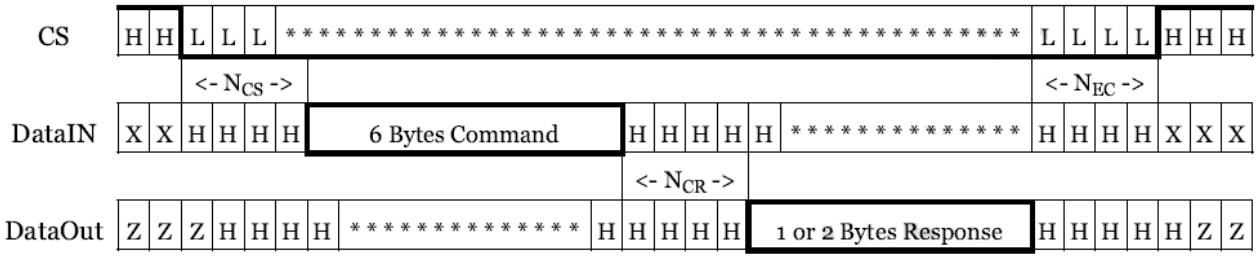
Before looking at the diagrams, please keep in mind that all timing diagrams are following the schematics and the abbreviations below.

H	Signal is high (logical “1”)
L	Signal is low (logical “0”)
X	Don’t’ care/ignore
Z	High impedance state (->=1)
*	Repeater
Busy	Busy token
Command	Command token
Response	Response token
Data block	Data token

Command & Response

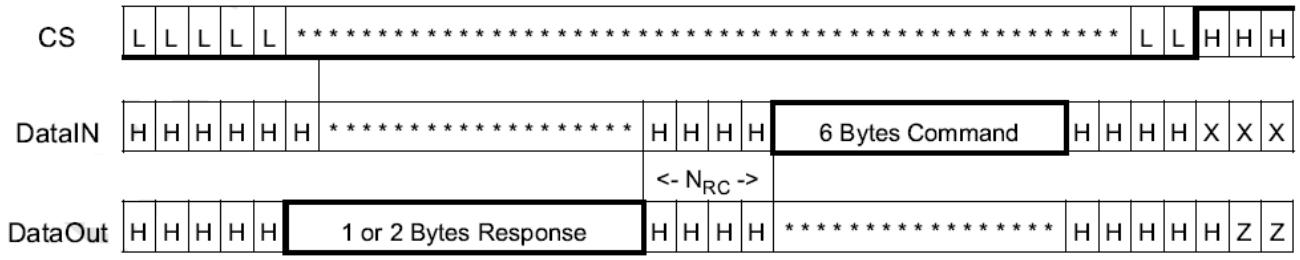
Host Command to Card Response – Card is ready

The following timing diagram describes the basic command response (no data) SPI transaction.



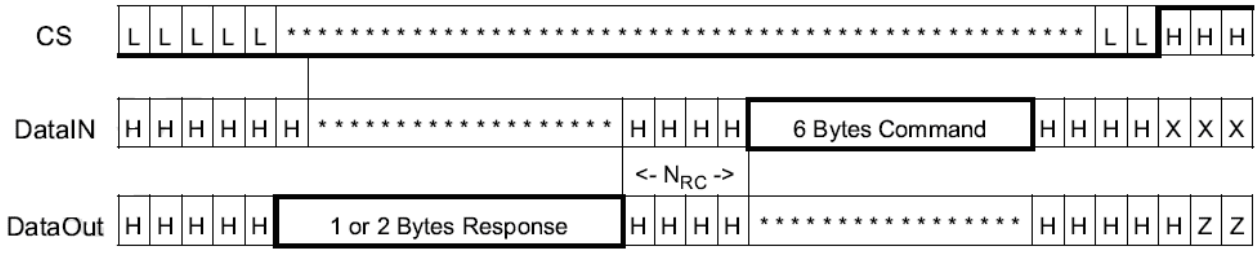
Host Command to Card Response – Card is busy

The following timing diagram describes the command-response transaction with the R1b response (for example, SET_WRITE_PROT and ERASE). When the card is signaling busy, the host may de-select it (by raising the CS) at any time. The card will release the DataOut line one clock after the CS goes high. To check if the card is still busy, it needs to be re-selected by asserting (set to low) the CS signal. The card will resume busy signal (pulling DataOut low) one clock after the falling edge of CS.



Card Response to Host Command

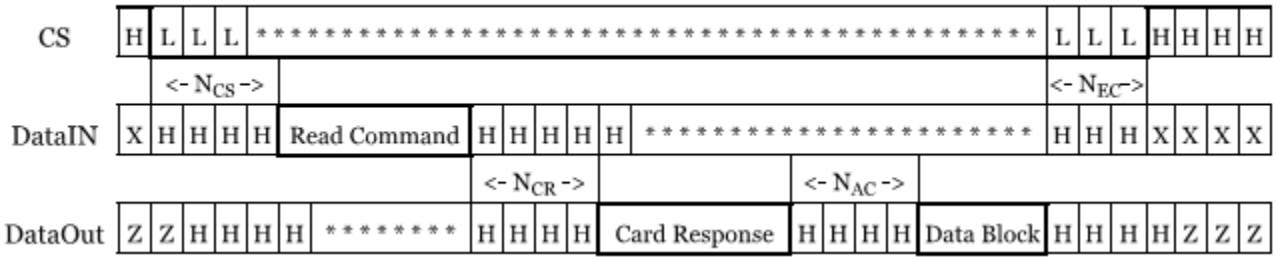
The following diagram describes timing between card response to new host command.



Data Read

Timing of Single Block Read Operation

The following timing diagram describes all single-block read operations with the exception of SEND_CSD and SEND_CID commands.



Stop Transmission Timing of Multiple Block Read Operation

The following table describes Stop Transmission operation in case of Multiple Block Read.

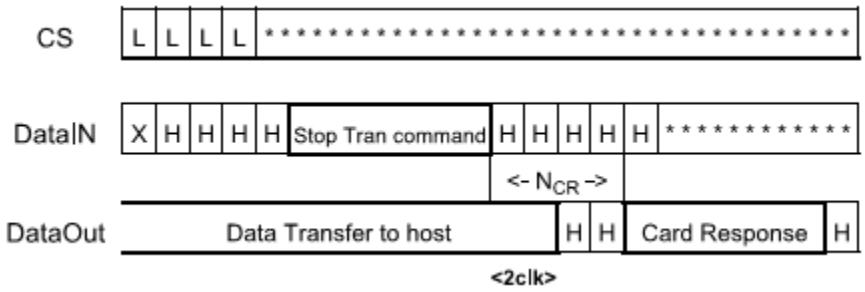
Clock cycle between read data blocks are defined by NAC (not shown in the following diagram).

To avoid conflict between CMD12 response and next data block, timing of CMD12 should be controlled as follows.

1. SPI host should issue CMD12 at the timing that end bit of CMD12 and end bit of data block is overlapped.

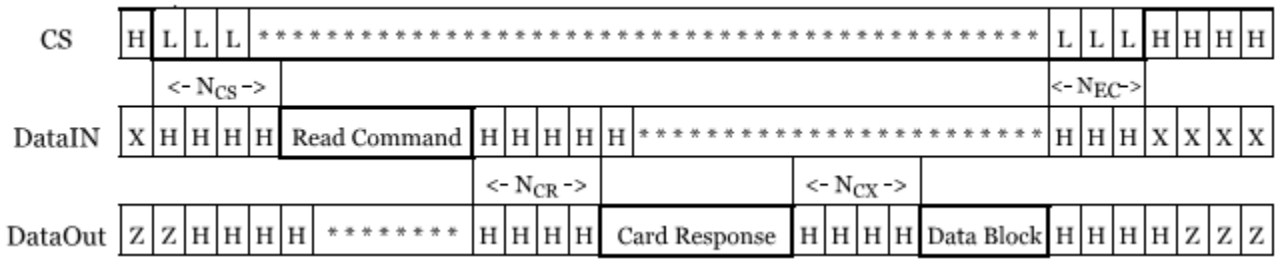
2. If 1. is not possible, SPI host should wait to receive a token (Start Block Token or Data Error Token), and then issue CMD12 after one clock from the token.

After the last block is read in case of 2., the host receives Data Error Token by out of range error. However, the data block before Data Error Token can be considered as valid if it is received successfully.



Reading the CSD or CID Register

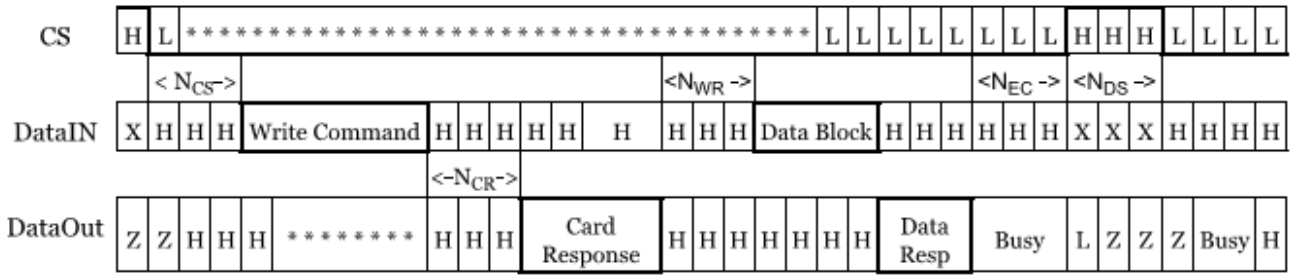
The following timing diagram describes the SEND_CSD and SEND_CID command bus transactions. The timeout values for the response and the data block are N_{CR} and N_{CX} respectively. (Since the NAC is still unknown).



Data Write

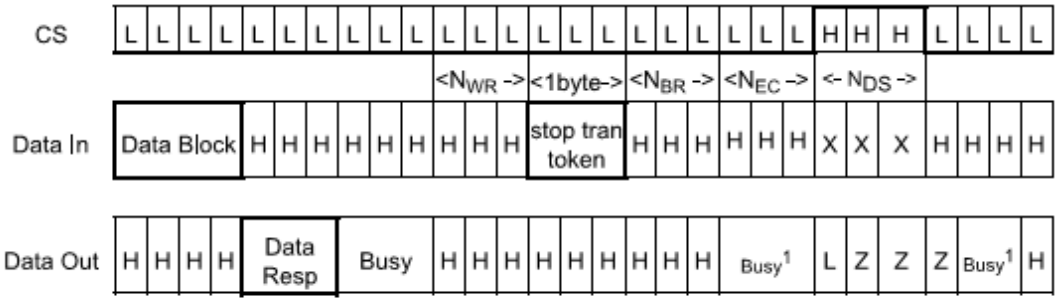
Timing of Multiple Block Write Operation

The host may de-select a card (by raising the CS) at any time during the card busy period (refer to the given timing diagram). The card will release the DataOut line one clock after the CS goes high. To check if the card is still busy, it needs to be re-selected by asserting (set to low) the CS signal. The card will resume busy signal (pulling DataOut low) one clock after the falling edge of CS.



Stop Transmission Timing of Multiple Block Write Operation

The following figure describes stop transmission operation in multiple block write transfer. Error occurrence after the last data response token is indicated in the response of the next command.



(1) The Busy may appear within N_{BR} clocks after the Stop Tran Token. If there is no Busy signal, the host may continue to the next command.

Timing Values

All timing values are defined in the following table. The host shall keep the clock running for at least N_{CR} clock cycles after receiving the card response. This restriction applies to both command and data response tokens.

Parameter	Min.	Max.	Unit
N_{CS}	0	-	8 clock cycles
N_{CR}	1	8	8 clock cycles
N_{RC}	1	-	8 clock cycles
N_{AC}	1	spec. in the CSD	8 clock cycles
N_{WR}	1	-	8 clock cycles
N_{EC}	0	-	8 clock cycles
N_{DS}	0	-	8 clock cycles
N_{BR}	0	1	8 clock cycles
N_{CX}	0	8	8 clock cycles

Notes for N_{AC}: the maximum read access time for a standard capacity SD memory card shall be calculated by host as follows

N_{AC} (max) = 100 ((TAAC*fpp)+(100*NSAC));

fpp is the interface clock rate and TAAC & NSAC are given in the CSD (Chapter 5.3).

n the case of a high capacity SD memory card, a fixed value (100 ms) shall be used for the maximum read access time. Details of read, write and erase timeout are described in section 4.6.2 of SD card Physical Layer Specifications (ver. 3.00).

SPI Electrical Interface

The electrical interface is identical to SD mode with the exception of the programmable card output drivers option, which is not supported in SPI mode.

SPI Bus Operation Conditions

Bus operating conditions are identical to SD mode.

Bus Timing

Bus timing is identical to SD mode. The timing of the CS signal is the same as any other card input.

Revision History

Revision	Description	Date
1.0	Official release	03/08/2013

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