

**RoHS Recast Compliant**

## **Industrial microSD 6.1**

**CV110-MSD Product Specifications**

(Toshiba TLC BiCS3 64 Layers)

**June 4, 2021**

**Version 1.3**



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## Specifications Overview:

- **Fully Compatible with SD Card Association Specifications**
  - Physical Layer Specification Ver6.1
  - Security Specification Ver4.0
- **Capacity**
  - 32, 64, 128, 256 GB
- **Performance\***
  - Sequential read: Up to 85 MB/sec
  - Sequential write: Up to 32 MB/sec
  - Random read (4K): Up to 1,500 IOPS
  - Random write (4K): Up to 600 IOPS
- **Flash Management**
  - Built-in advanced ECC algorithm
  - Global Wear Leveling
  - Flash bad-block management
  - Power Failure Management
  - Flash Translation Layer: Page Mapping
  - DataRAID™
  - S.M.A.R.T.
  - SMART Read Refresh™
- **NAND Flash Type:** Toshiba TLC BiCS3 64 Layers
- **SD-Protocol Compatible**
- **Supports SD SPI Mode**
- **Backward Compatible with 3.0 and 2.0**
- **Endurance (in Terabytes Written: TBW)**
  - 32 GB: 48 TBW
  - 64 GB: 94 TBW
  - 128 GB: 163 TBW
  - 256 GB: 342 TBW
- **Temperature Range**
  - Operating:
    - Standard: -25°C to 85°C
    - Wide: -40°C to 85°C
  - Storage: -40°C to 85°C
- **Operating Voltage: 2.7V ~ 3.6V**
- **Power Consumption\***
  - Operating: 95 mA
  - Standby: 160 µA
- **Bus Speed Mode:** Supports Class 10 with U1 and UHS-I\*\*
  - SDR12: SDR up to 25MHz 1.8V signaling
  - SDR25: SDR up to 50MHz 1.8V signaling
  - SDR50: 1.8V signaling, frequency up to 100MHz, up to 50 MB/sec
  - SDR104: 1.8V signaling, frequency up to 208MHz, up to 104MB/sec
  - DDR50: 1.8V signaling, frequency up to 50MHz, sampled on both clock edges, up to 50 MB/sec
- **Physical Dimensions**
  - 15mm (L) x 11mm (W) x 1mm (H)
- **Supports Video Speed Class**
  - V10: 32 GB
  - V30: 64-256 GB
- **RoHS Recast Compliant**

\*Performance values presented here are typical and measured based on USB 3.0 card reader. The results may vary depending on settings and platforms.

\*\*Timing in 1.8V signaling is different from that of 3.3V signaling. Operation mode selection command is compliant with SD 3.0, referring to SDA's Part 1, Physical Layer Specification, Ver 3.01 (Section 3.9).

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# 1. General Descriptions

Apacer microSD CV110-MSD is compatible with the microSD card version 6.1. The command list supports [Physical Layer Specification Ver6.10 Final] definitions. Card Capacity of Non-secure Area, Secure Area Supports [Part 3 Security Specification Ver4.00 Final] Specifications.

The microSD 6.1 card comes with 8-pin interface. It can alternate communication protocols between the microSD mode and SPI mode. It performs data error detection and correction with very low power consumption. It supports capacity up to 256GB with exFAT SDXC.

Apacer microSD CV110-MSD Secure Digital 4.0 with high performance, good reliability and wide compatibility is nowadays one of the most popular cards well adapted for hand-held applications with customized firmware techniques in semi-industrial/medical markets already.

## 1.1 Functional Block

The microSD contains a card controller and a memory core for the microSD standard interface.

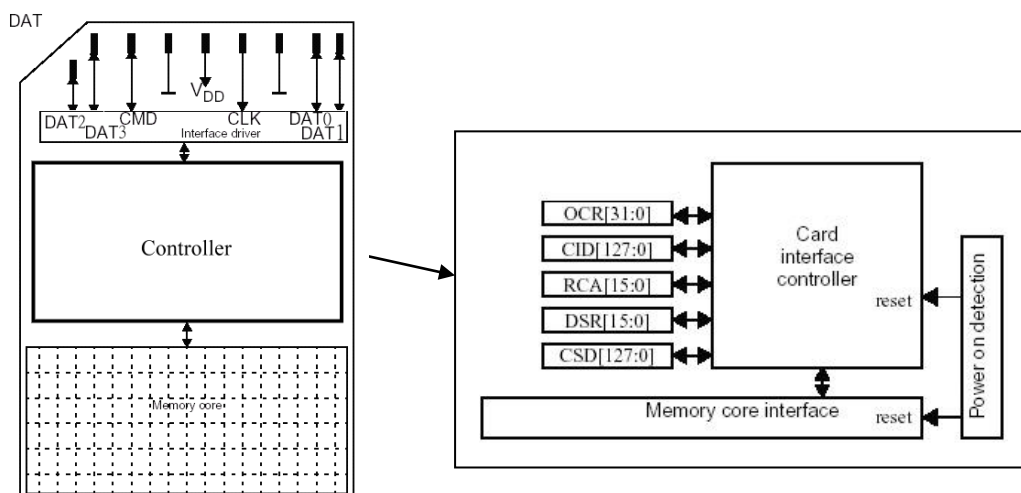


Figure 1-1 Functional Block Diagram

## 1.2 Flash Management

### 1.2.1 Bad Block Management

The microSD controller contains logical/physical flash block mapping and bad block management system. It will manage all flash block include user data space and spare block.

The microSD also contains a sophisticated defect and error management system. It does a read after write under margin conditions to verify that the data is written correctly (except in the case of write pre-erased sectors). In case that a bit is found to be defective, the microSD replaces this bad bit with a spare bit within the sector header. If necessary, the microSD will even replace the entire sector with a spare sector. This is completely transparent to the master (host device) and does not consume any user data space.

### 1.2.2 Powerful ECC Algorithms

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, the microSD card applies the advanced ECC Algorithm, which can detect and correct errors occur during read process, ensure data been read correctly, as well as protect data from corruption.

### 1.2.3 S.M.A.R.T.

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is a special function that allows a memory device to automatically monitor its health. Apacer provides a program named SmartInfo Tool to observe Apacer's SD and microSD cards. Note that this tool can only support Apacer's industrial SD and microSD cards. This tool will display firmware version, endurance life ratio, good block ratio, and so forth.

### 1.2.4 Global Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some area get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Global Wear Leveling technique is applied to extend the lifespan of NAND Flash by evenly distributing writes and erase cycles across the media.

Apacer provides Global Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing Global Wear Leveling algorithm, the life expectancy of the NAND Flash is greatly improved.

### 1.2.5 Power Failure Management

Power Failure Management plays a crucial role when power supply becomes unstable. Power disruption may occur when users are storing data into the SSD, leading to instability in the drive. However, with Power Failure Management, a firmware protection mechanism will be activated to scan pages and blocks once power is resumed. Valid data will be transferred to new blocks for merging and the mapping table will be rebuilt. Therefore, data reliability can be reinforced, preventing damage to data stored in the NAND Flash.

### 1.2.6 DataRAID™

Apacer's DataRAID algorithm applies an additional level of protection and error-checking. Using this algorithm, a certain amount of space is given over to aggregating and resaving the existing parity data used for error checking. So, in the event that data becomes corrupted, the parity data can be compared to the existing uncorrupted data and the content of the corrupted data can be rebuilt.

## 1.2.7 SMART Read Refresh™

Apacer's SMART Read Refresh plays a proactive role in avoiding read disturb errors from occurring to ensure health status of all blocks of NAND flash. Developed for read-intensive applications in particular, SMART Read Refresh is employed to make sure that during read operations, when the read operation threshold is reached, the data is refreshed by re-writing it to a different block for subsequent use.

## 1.2.8 Flash Translation Layer – Page Mapping

Page mapping is an advanced flash management technology whose essence lies in the ability to gather data, distribute the data into flash pages automatically, and then schedule the data to be evenly written. Page-level mapping uses one page as the unit of mapping. The most important characteristic is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different sizes of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. Thus, page mapping is adopted to increase random access speed and improve microSD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

## 2. Product Specifications

### 2.1 Card Architecture

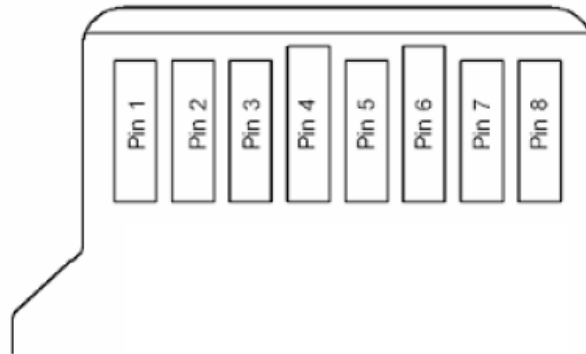


Figure 2-1 Card Architecture

### 2.2 Pin Assignment

Table 2-1 Pin Descriptions

Pin	microSD Mode		SPI Mode	
	Name	Description	Name	Description
1	DAT2	Data line[bit 2]	Reserved	
2	CD/DAT3	Card Detect/Data line [bit 3]	CS	Chip select
3	CMD	Command/Response	DI	Data in
4	VDD	Supply voltage	VDD	Supply voltage
5	CLK	Clock	SCLK	Clock
6	VSS	Supply voltage ground	VSS	Supply voltage ground
7	DAT0	Data line[bit 0]	DO	Data out
8	DAT1	Data line[bit 1]	Reserved	

## 2.3 Capacity

The following table shows the specific capacity for the microSD 6.1 card.

**Table 2-2** Capacity Specifications

Capacity	Total bytes*
32 GB	31,033,655,296
64 GB	62,243,471,360
128 GB	124,755,378,176
256 GB	249,443,647,488

Note: Total bytes are viewed under Windows operating system and were measured by microSD format too.

## 2.4 Performance

Performances of the microSD 6.1 card are shown in the table below.

**Table 2-3** Performance Specifications

Capacity	32 GB	64 GB	128 GB	256 GB
<b>Sequential Read* (MB/s)</b>	85	85	80	85
<b>Sequential Write* (MB/s)</b>	20	27	32	32
<b>Random Read IOPS** (4K)</b>	1,400	1,500	1,500	1,500
<b>Random Write IOPS** (4K)</b>	500	600	600	600

Note:

Results may differ from various flash configurations or host system setting.

\*Sequential performance is based on CrystalDiskMark 5.2.1 with file size 1,000MB.

\*\*Random performance measured using IOMeter with Queue Depth 32.

\*\*\*Performance results are measured based on USB 3.0 card reader.

## 2.5 Electrical

**Table 2-4** Operating Voltages

Symbol	Parameter	Min.	Max.	Unit
V <sub>DD</sub>	Power Supply Voltage	2.7	3.6	V

**Table 2-5** Power Consumption

Capacity	32 GB	64 GB	128 GB	256 GB
<b>Operating (mA)</b>	70	75	90	95
<b>Standby (µA)</b>	85	95	120	160

Note:

\*All values are typical and may vary depending on flash configurations or host system settings.

\*\*Active power is an average power measurement performed using CrystalDiskMark with 128KB sequential read/write transfers.

\*\*\*Power is measured based on USB 3.0 card reader.

## 2.6 Endurance

The endurance of a storage device is predicted by TeraBytes Written based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

**Table 2-6** Endurance Specifications

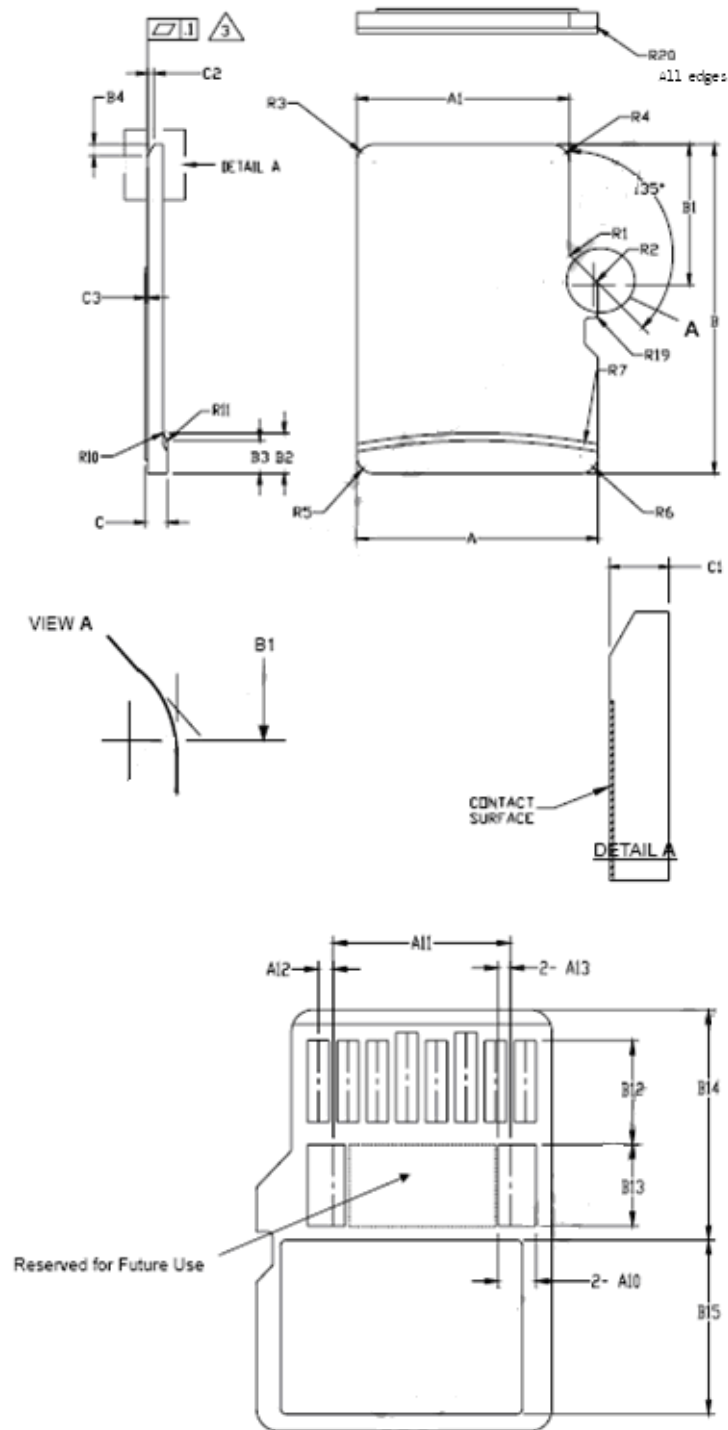
Capacity	TeraBytes Written
32 GB	48
64 GB	94
128 GB	163
256 GB	342

Note:

- This estimation complies with Apacer internal workload.
- Flash vendor guaranteed 3D NAND TLC P/E cycle: 3K
- WAF may vary from capacity, flash configurations and writing behavior on each platform.
- 1 Terabyte = 1,024GB
- DWPD (Drive Write Per Day) is calculated based on the number of times that user can overwrite the entire capacity of an SSD per day of its lifetime during the warranty period. (3D NAND TLC warranty: 2 years)


### 3. Physical Characteristics

#### 3.1 Physical Dimensions



SYMBOL	COMMON DIMENSIONS			NOTE
	MIN	NOM	MAX	
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.80	-	-	
A10	1.35	1.40	1.45	
A11	6.50	6.60	6.70	
A12	0.50	0.55	0.60	
A13	0.40	0.45	0.50	
B	14.90	15.00	15.10	
B1	6.30	6.40	6.50	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	5.50	-	-	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	-	-	9.00	
B10	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
B12	3.60	3.70	3.80	
B13	2.80	2.90	3.00	
B14	8.20	-	-	
B15	-	-	6.20	
C	0.90	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	
D1	1.00	-	-	
D2	1.00	-	-	
D3	1.00	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.70	0.80	0.90	
R6	0.70	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	
R20	0.02	-	0.15	

Notes:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3.  COPLANARITY IS ADDITIVE TO C1 MAX THICKNESS.

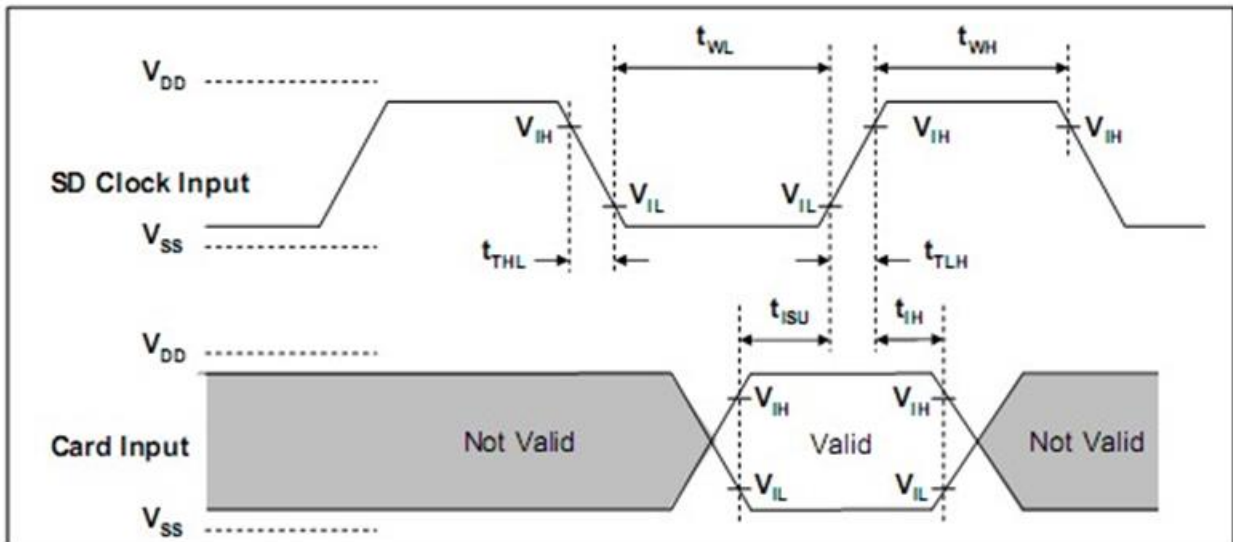
### 3.2 Durability Specifications

**Table 3-1** Durability Specifications

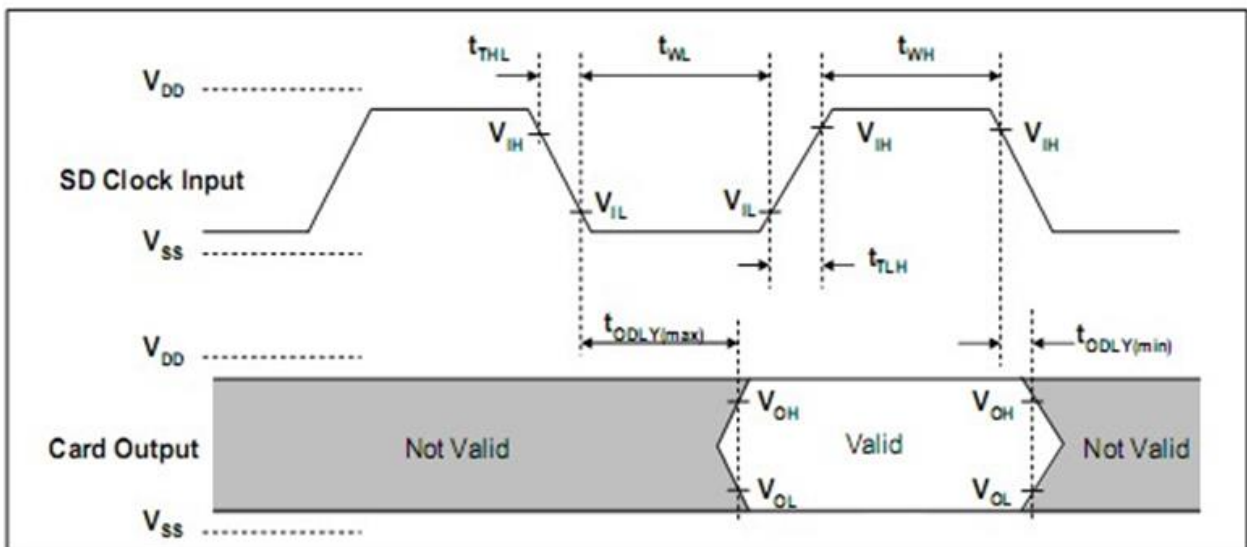
Item	Specifications
Temperature	-25°C to 85°C (Operating) -40°C to 85°C (Wide)
	-40°C to 85°C (Storage)
Shock	1,500G, 0.5ms
Vibration	20Hz~80Hz/1.52mm (frequency/displacement) 80Hz~2000Hz/20G (frequency/displacement) X, Y, Z axis/60mins each
Drop	150cm free fall, 6 face of each
Bending	≥ 10N, hold 1min/5times
Torque	0.1N-m or 2.5deg, hold 5min/5times
Salt Spray	Concentration: 3% NaCl at 35°C (storage for 24 hours)
Waterproof	JIS IPX7 compliance Water temperature 25°C Water depth: the lowest point of unit is locating 1000mm below surface (storage for 30 mins)
X-Ray Exposure	0.1 Gy of medium-energy radiation (70 KeV to 140 KeV, cumulative dose per year) to both sides of the card (storage for 30 mins)
Durability	10,000 times mating cycle
ESD	Pass

## 4. AC Characteristics

### 4.1 microSD Interface Timing (Default)



Card input Timing (Default Speed Card)

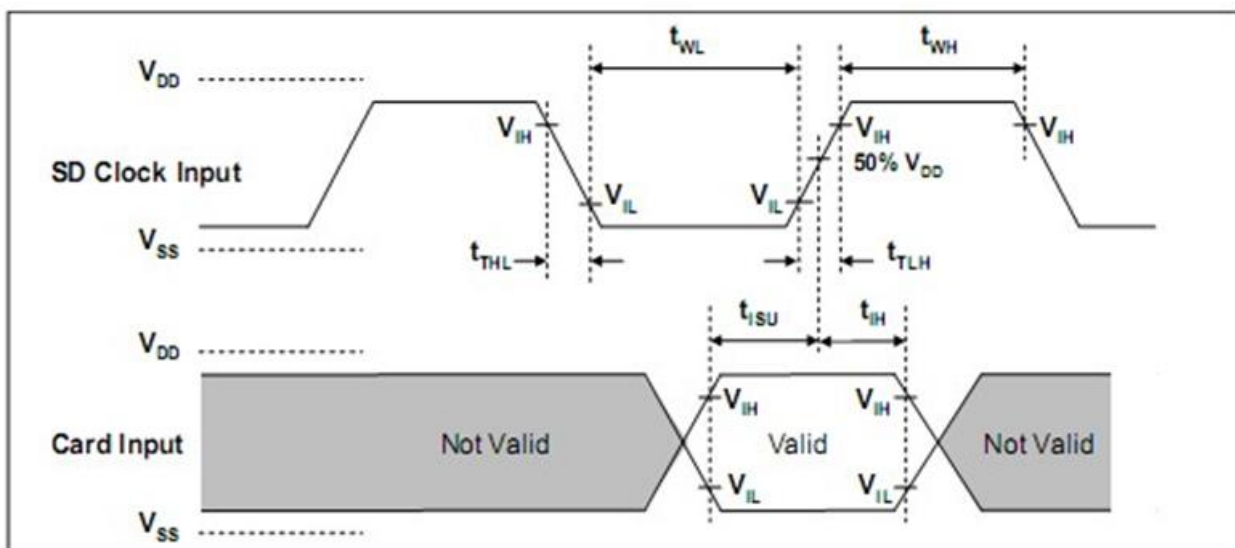


Card Output Timing (Default Speed Mode)

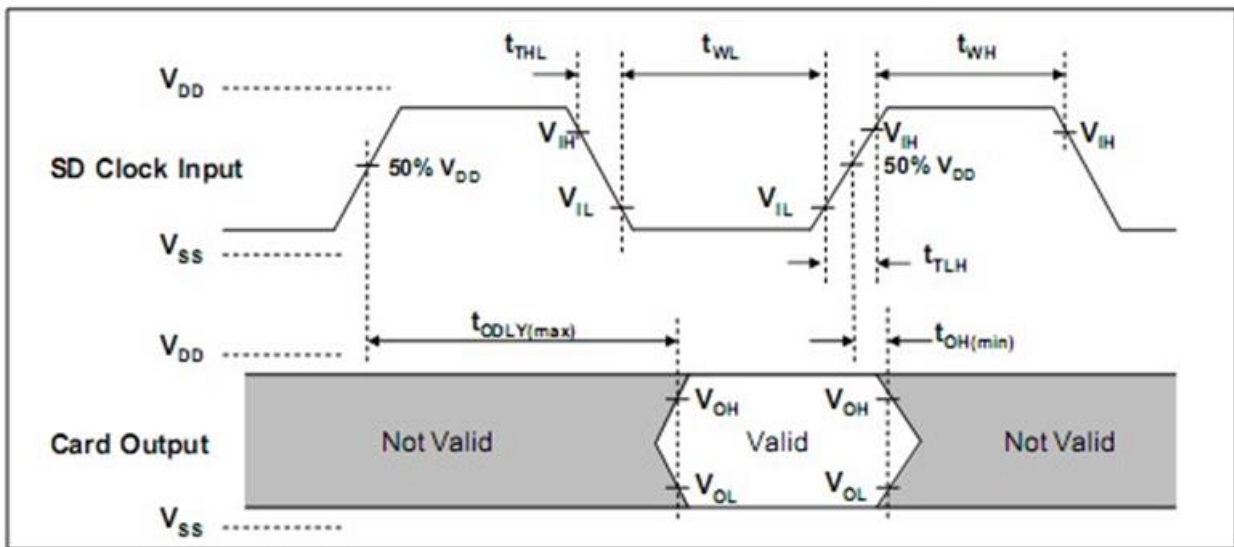
SYMBOL	PARAMETER	MIN	MAX	UNIT	REMARK
<b>Clock CLK (All values are referred to min(V<sub>IH</sub>) and max(V<sub>IL</sub>))</b>					
f <sub>PP</sub>	Clock frequency data transfer	0	25	MHz	C <sub>card</sub> ≤ 10 pF (1 card)
f <sub>OD</sub>	Clock frequency identification	0 <sup>(1)</sup> /100	400	KHz	C <sub>card</sub> ≤ 10 pF (1 card)
t <sub>WL</sub>	Clock low time	10	-	ns	C <sub>card</sub> ≤ 10 pF (1 card)
t <sub>WH</sub>	Clock high time	10	-	ns	C <sub>card</sub> ≤ 10 pF (1 card)
t <sub>TLH</sub>	Clock rise time	-	10	ns	C <sub>card</sub> ≤ 10 pF (1 card)
t <sub>THL</sub>	Clock fall time	-	10	ns	C <sub>card</sub> ≤ 10 pF (1 card)
<b>Inputs CMD, DAT (Referenced to CLK)</b>					
t <sub>ISU</sub>	Input setup time	5	-	ns	C <sub>card</sub> ≤ 10 pF (1 card)
t <sub>IH</sub>	Input hold time	5	-	ns	C <sub>card</sub> ≤ 10 pF (1 card)
<b>Outputs CMD, DAT (Referenced to CLK)</b>					
t <sub>ODLY</sub>	Output delay time during data transfer mode	0	14	ns	C <sub>L</sub> ≤ 40 pF (1 card)
t <sub>OH</sub>	Output hold time	0	50	ns	C <sub>L</sub> ≤ 40 pF (1 card)

(1)0Hz means to stop the clock. The given minimum frequency range is for cases that require the clock to be continued.

## 4.2 microSD Interface Timing (High Speed Mode)



**Card Input Timing (High Speed Card)**



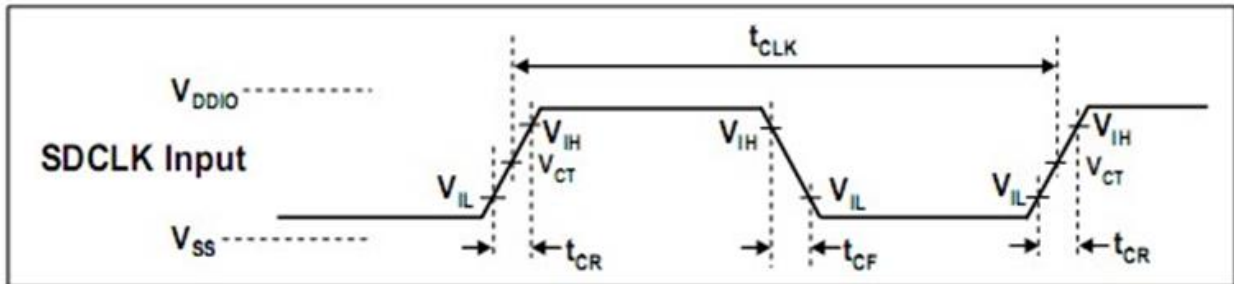
**Card Output Timing (High Speed Mode)**

SYMBOL	PARAMETER	MIN	MAX	UNIT	REMARK
<b>Clock CLK (All values are referred to min(V<sub>IH</sub>) and max(V<sub>IL</sub>))</b>					
f <sub>PP</sub>	Clock frequency data transfer	0	50	MHz	C <sub>card</sub> ≤ 10 pF (1 card)
t <sub>WL</sub>	Clock low time	7	-	ns	C <sub>card</sub> ≤ 10 pF (1 card)
t <sub>WH</sub>	Clock high time	7	-	ns	C <sub>card</sub> ≤ 10 pF (1 card)
t <sub>TLH</sub>	Clock rise time	-	3	ns	C <sub>card</sub> ≤ 10 pF (1 card)
t <sub>THL</sub>	Clock fall time	-	3	ns	C <sub>card</sub> ≤ 10 pF (1 card)
<b>Inputs CMD, DAT (Referenced to CLK)</b>					
t <sub>ISU</sub>	Input setup time	6	-	ns	C <sub>card</sub> ≤ 10 pF (1 card)
t <sub>IH</sub>	Input hold time	2	-	ns	C <sub>card</sub> ≤ 10 pF (1 card)
<b>Outputs CMD, DAT (Referenced to CLK)</b>					
t <sub>ODLY</sub>	Output delay time during data transfer made	-	14	ns	CL ≤ 40 pF (1 card)
t <sub>OH</sub>	Output hold time	2.5	-	ns	CL ≥ 15 pF (1 card)
CL	Total system capacitance for each line*	-	40	pF	1 card

\*In order to satisfy severe timing, host shall run on only one card

### 4.3 microSD Interface Timing (SDR12, SDR25, SDR50 and SDR104 Modes)

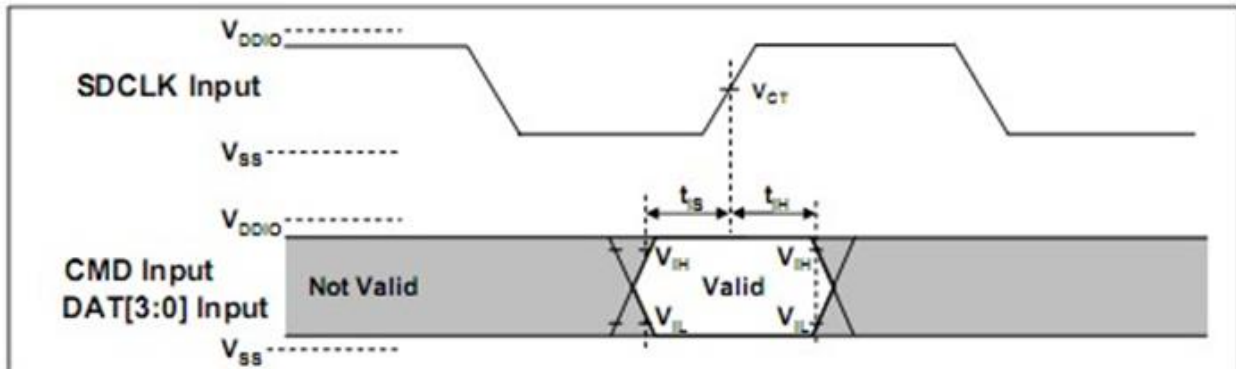
#### 4.3.1 Clock Timing



**Clock Signal Timing**

SYMBOL	MIN	MAX	UNIT	REMARK
$t_{CLK}$	4.8	-	ns	208MHz (Max.), Between rising edge, $V_{CT} = 0.975V$
$t_{CR}, t_{CF}$	-	$0.2 * t_{CLK}$	ns	$t_{CR}, t_{CF} < 2.00ns$ (max.) at 208MHz, $C_{CARD}=10pF$ $t_{CR}, t_{CF} < 2.00ns$ (max.) at 100MHz, $C_{CARD}=10pF$ The absolute maximum value of $t_{CR}, t_{CF}$ is 10ns regardless of clock frequency.
Clock Duty	30	70	%	

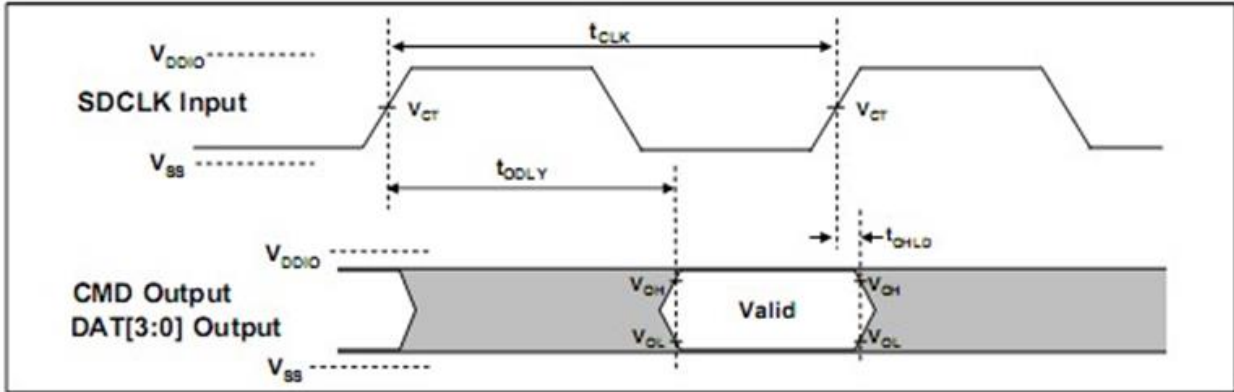
#### 4.3.2 Card Input Timing



**Card Input Timing**

SYMBOL	MIN	MAX	UNIT	SDR104 MODE
$t_{IS}$	1.40	-	ns	$C_{CARD} = 10pF, V_{CT} = 0.975V$
$t_{IH}$	0.80	-	ns	$C_{CARD} = 5pF, V_{CT} = 0.975V$
SYMBOL	MIN	MAX	UNIT	SDR12, SDR25 and SDR50 MODES
$t_{IS}$	3.00	-	ns	$C_{CARD} = 10pF, V_{CT} = 0.975V$
$t_{IH}$	0.80	-	ns	$C_{CARD} = 5pF, V_{CT} = 0.975V$

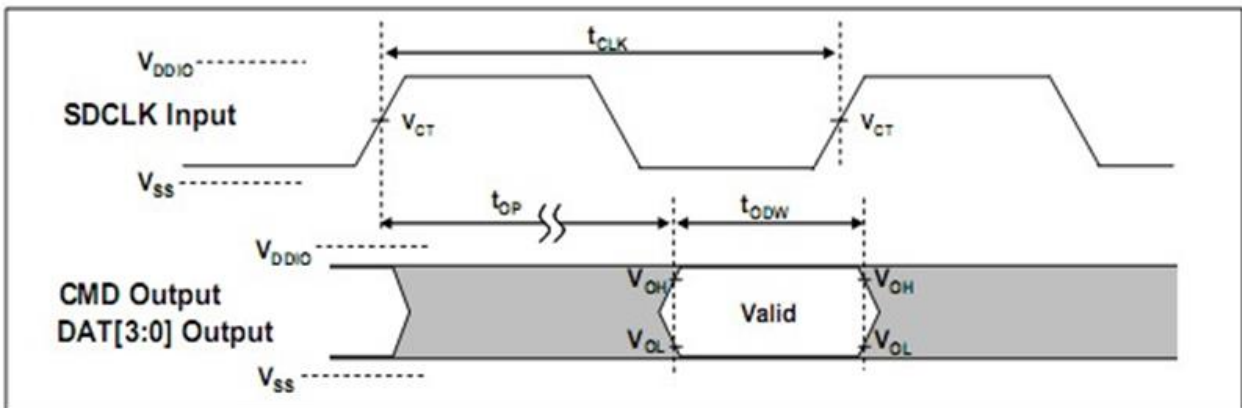
### 4.3.3 Card Output Timing of Fixed Data Window (SDR12, SDR25 and SDR50)



Output Timing of Fixed Date Window<sup>+</sup>

SYMBOL	MIN	MAX	UNIT	REMARK
$t_{ODLY}$	-	7.5	ns	$t_{CLK} \geq 10.0ns$ , $CL=30pF$ , using driver Type B, for SDR50.
$t_{ODLY}$		14	ns	$t_{CLK} \geq 20.0ns$ , $CL=40pF$ , using driver Type B, for SDR25 and SDR12.
$t_{OH}$	1.5	-	ns	Hold time at the $t_{ODLY}$ (min.). $CL=15pF$

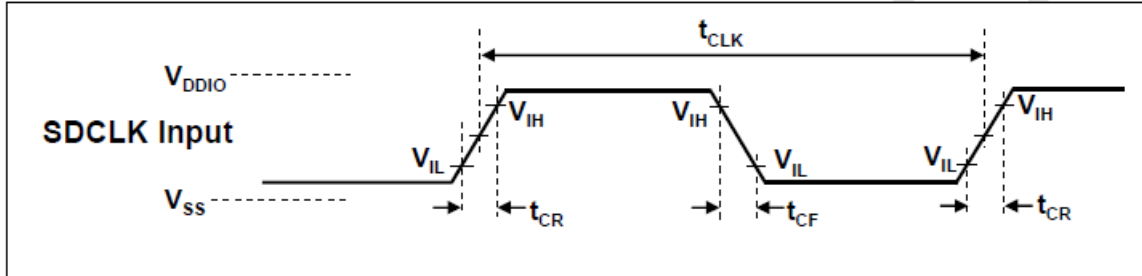
### 4.3.4 Output Timing of Variable Window (SDR104)



Output Timing of Variable Data Window<sup>+</sup>

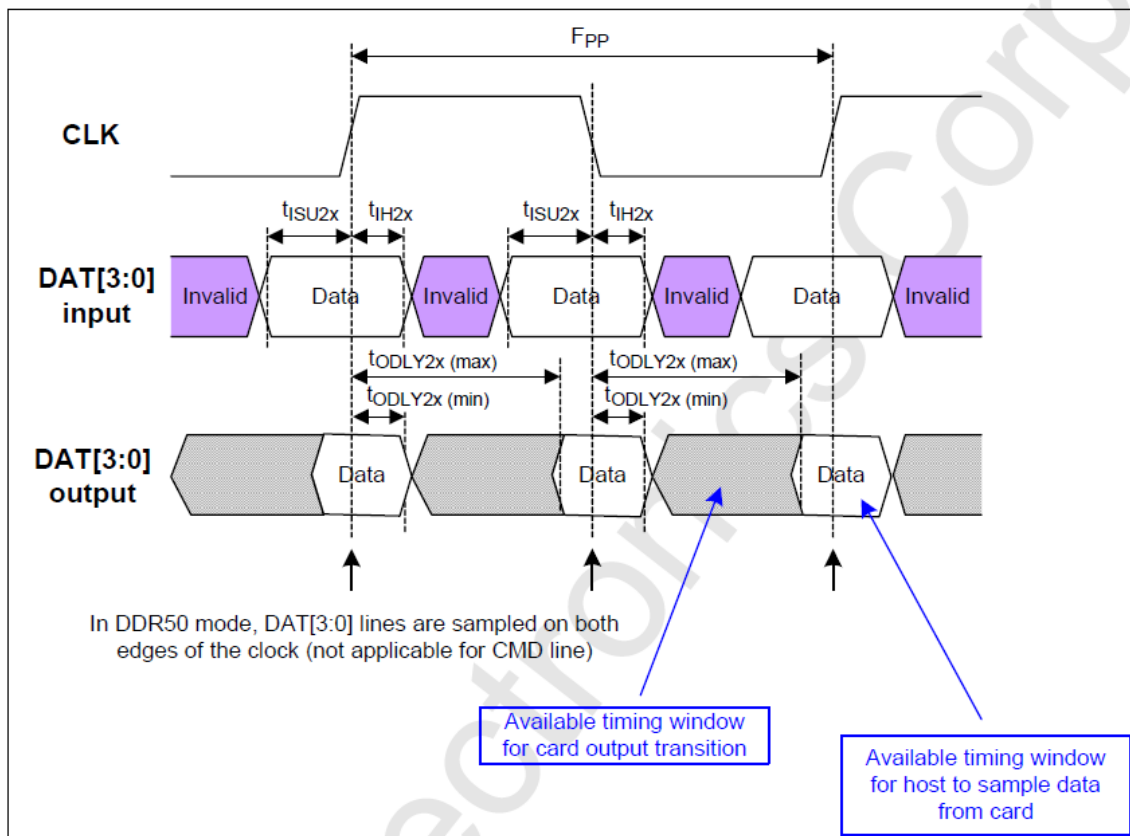
SYMBOL	MIN	MAX	UNIT	REMARK
$t_{OP}$	-	2	UI	Card Output Phase
$\Delta t_{OP}$	-350	+1550	ps	Delay variation due to temperature change after tuning
$t_{ODW}$	0.60	-	UI	$t_{ODW} = 2.88ns$ at 208MHz

### 4.3.5 SD Interface Timing (DDR50 Mode)



**Clock Signal Timing**

SYMBOL	MIN	MAX	UNIT	REMARK
$t_{CLK}$	20	-	ns	50MHz (Max.), Between rising edge
$t_{CR}, t_{CF}$	-	$0.2 \cdot t_{CLK}$	ns	$t_{CR}, t_{CF} < 4.00\text{ns (max.)}$ at 50MHz, CCARD=10pF
Clock Duty	45	55	%	



**Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode**

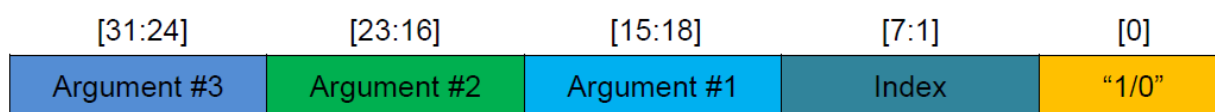
### 4.3.6 Bus Timings – Parameters Values (DDR50 Mode)

Symbol	Parameters	Min	Max	Unit	Remark
<b>Input CMD</b> (referenced to CLK rising edge)					
t <sub>ISU</sub>	Input set-up time	6	-	ns	C <sub>card</sub> ≤ 10 pF (1 card)
t <sub>IH</sub>	Input hold time	0.8	-	ns	C <sub>card</sub> ≤ 10 pF (1 card)
<b>Output CMD</b> (referenced to CLK rising edge)					
t <sub>ODLY</sub>	Output Delay time during Data Transfer Mode	-	13.7	ns	C <sub>L</sub> ≤ 30 pF (1 card)
T <sub>OH</sub>	Output Hold time	1.5	-	ns	C <sub>L</sub> ≥ 15 pF (1 card)
<b>Inputs DAT</b> (referenced to CLK rising and falling edges)					
t <sub>ISU2x</sub>	Input set-up time	3	-	ns	C <sub>card</sub> ≤ 10 pF (1 card)
t <sub>IH2x</sub>	Input hold time	0.8	-	ns	C <sub>card</sub> ≤ 10 pF (1 card)
<b>Outputs DAT</b> (referenced to CLK rising and falling edges)					
t <sub>ODLY2x</sub>	Output Delay time during Data Transfer Mode	-	7.0	ns	C <sub>L</sub> ≤ 25 pF (1 card)
T <sub>OH2x</sub>	Output Hold time	1.5	-	ns	C <sub>L</sub> ≥ 15 pF (1 card)

## 5. S.M.A.R.T.

### 5.1 Direct Host Access to SMART Data via SD General Command (CMD56)

CMD 56 is structured as a 32-bit argument. The implementation of the general purpose functions will arrange the CMD56 argument into the following format:



- Bit [0]: Indicates Read Mode when bit is set to [1] or Write Mode when bit is cleared [0]. Depending on the function, either Read Mode or Write Mode can be used.
- Bit [7:1]: Indicates the index of the function to be executed:
  - Read Mode: Index = 0x10 Get SMART Command Information
  - Write Mode: Index = 0x08 Pre-Load SMART Command Information
- Bit [15:8]: Function argument #1 (1-byte)
- Bit [23:16]: Function argument #2 (1-byte)
- Bit [31:24]: Function argument #3 (1-byte)

### 5.2 Process for Retrieving SMART Data

Retrieving SMART data requires the following two commands executed in sequence and in accordance with the SD Association standard flowchart for CMD56 (see below).

#### Step 1: Write Mode – [0x08] Pre-Load SMART Command Information

Sequence	Command	Argument	Expected Data
Pre-Load SMART Command Information	CMD56	[0] "0" (Write Mode) [1:7] "0001 000" (Index = 0x08) [8:511] All '0' (Reserved)	No expected data

**Step 2: Read Mode – [0x10] Get SMART Command Information**

Sequence	Command	Argument	Expected Data
Get SMART Command Information	CMD56		1 sector (512 bytes) of response data
		[0] "1" (Read Mode) [1:7] "0010 000" (Index = 0x10) [8:31] All '0' (Reserved)	byte[0-8] Flash ID byte[9-10] IC Version byte[11-12] FW Version byte[13] Reserved byte[14] CE Number byte[15] Reserved byte[16-17] Bad Block Replace Maximum byte[18] Reserved byte[32-63] Bad Block count per Die byte[64-65] Good Block Rate(%) byte[66-79] Reserved byte[80-83] Total Erase Count byte[84-95] Reserved byte[96-97] Endurance (Remain Life) (%) byte[98-99] Average Erase Count – L* byte[100-101] Minimum Erase Count – L* byte[102-103] Maximum Erase Count – L* byte[104-105] Average Erase Count – H* byte[106-107] Minimum Erase Count – H* byte[108-109] Maximum Erase Count – H* byte[110-111] Reserved byte[112-115] Power Up Count byte[116-127] Reserved byte[128-129] Abnormal Power Off Count byte[130-159] Reserved byte[160-161] Total Refresh Count byte[176-183] Product "Marker" byte[184-215] Bad Block count per Die byte[216-511] Reserved

\*Please refer to technical note for High/Low byte definition.

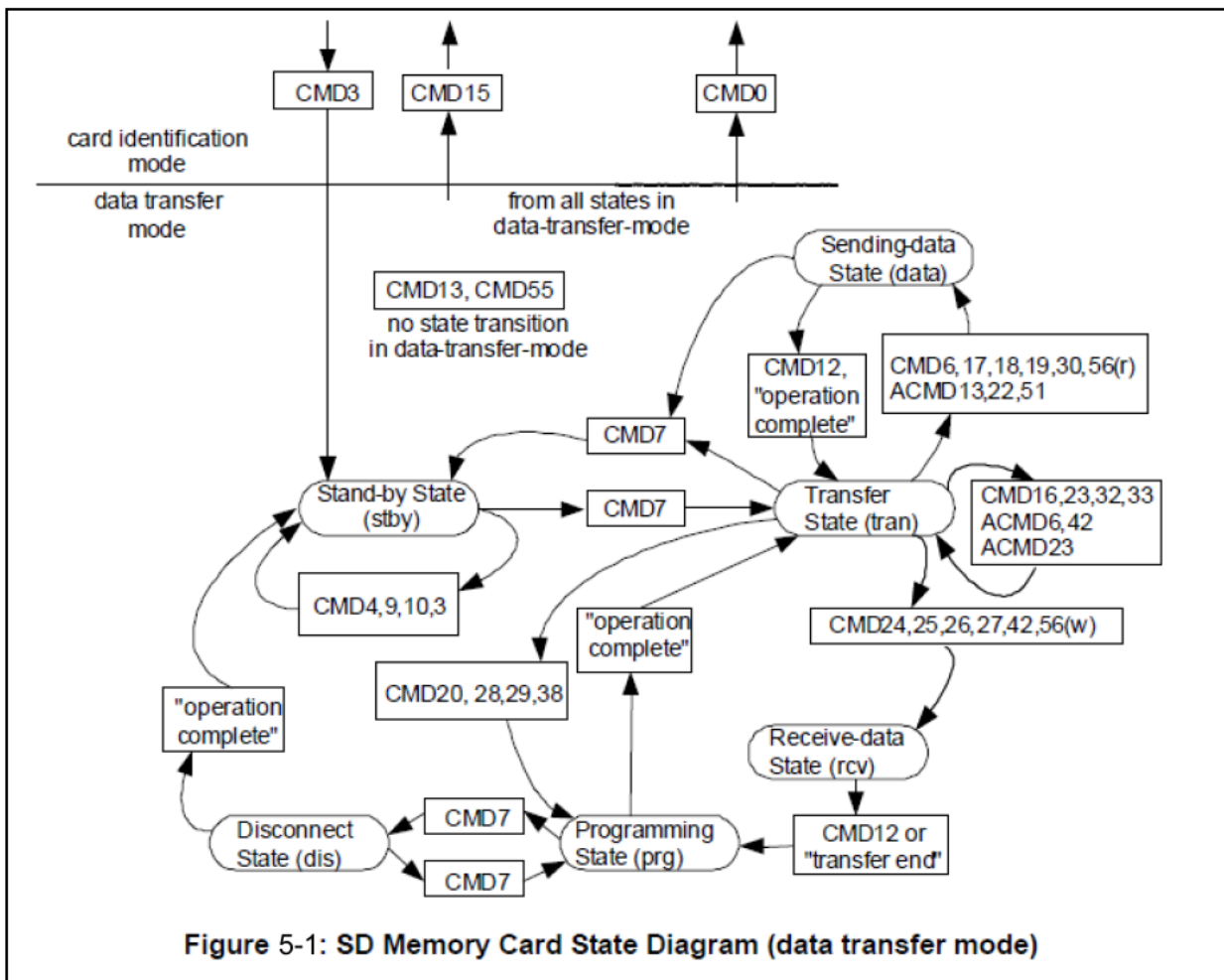


Figure 5-1: SD Memory Card State Diagram (data transfer mode)

Extracted from the SD Specifications Part 1 Physical Layer Simplified Specification Version 3.01.

## 6. Product Ordering Information

### 6.1 Product Code Designations

Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	A	K	6	.	1	1	X	X	X	A	.	X	X	X	1	0

<b>Code 1-3 (Product Line &amp; form factor)</b>	CV110-MSD
<b>Code 5-6 (Model/Solution)</b>	CV110
<b>Code 7-8 (Product Capacity)</b>	2F: 32GB 2G: 64GB 2H: 128GB 2J: 256GB
<b>Code 9 (Flash Type &amp; Product Temp)</b>	G: 3D TLC Standard Temperature H: 3D TLC Wide Temperature
<b>Code 10 (Product Spec)</b>	microSD Card
<b>Code 12-14 (Version Number)</b>	Random number generated by system
<b>Code 15-16 (Firmware Version)</b>	10: Firmware page mode

## 6.2 Valid Combinations

Capacity	Standard Temperature	Wide Temperature
32GB	AK6.112FGA.00110	AK6.112FHA.00110
64GB	AK6.112GGA.00110	AK6.112GHA.00110
128GB	AK6.112HGA.00110	AK6.112HHA.00110
256GB	AK6.112JGA.00110	AK6.112JHA.00110

**Note:** Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

## Revision History

Revision	Description	Date
1.0	Official release	10/3/2019
1.1	Updated supported bus mode to Class 10 with U3 and UHS-I at Bus Speed Mode on Specifications Overview	3/31/2020
1.2	Changed support for U3 to U1 at Bus Speed Mode on Specifications Overview page	4/8/2021
1.3	<ul style="list-style-type: none"><li>- Updated Performance and Power Consumption on Specifications Overview page</li><li>- Updated Tables 2-2, 2-3 and 2-5</li><li>- Updated 6. Product Ordering Information due to FW change</li></ul>	6/4/2021

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