

RoHS Recast Compliant

Industrial Secure Digital Card

R1 Product Specifications

January 19, 2016

Version 1.1



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FEATURES:

- **Fully Compatible with SD Card Specifications 3.0, 2.0 and 1.1**
 - SD Memory Card Specifications, Part 1, Physical Layer Specification, Version 2.00
 - SD Memory Card Specifications, Part 2, File System Specification, Version 2.00
 - SD Memory Card Specifications, Part 3, Security Specification, Version 2.00
- **Capacity**
 - 1, 2, 4, 8, 16 GB
- **Performance***
 - Sustained Read: Up to 43 MB/sec
 - Sustained Write: Up to 41 MB/sec
- **SD-Protocol Compatible**
- **Supports SD SPI Mode**
- **NAND Flash Type: SLC**
- **Dimensions: 32mm(L) x 24mm(W) x 2.1mm(H)**
- **Flash Management**
 - Flash bad-block management
 - Built-in advanced ECC algorithms
 - S.M.A.R.T.
 - Power management
 - Wear-leveling algorithms
- **Temperature Range**
 - Operating: -40°C to 85°C
 - Storage: -40°C to 85°C
- **Operating Voltage: 2.7V ~ 3.6V**
- **Power Consumption***
 - Operating: 120 mA
 - Standby: 260 μ A
- **RoHS Recast Compliant (2011/65/EU)**

*Performance values presented here are typical and may vary depending on settings and platforms.

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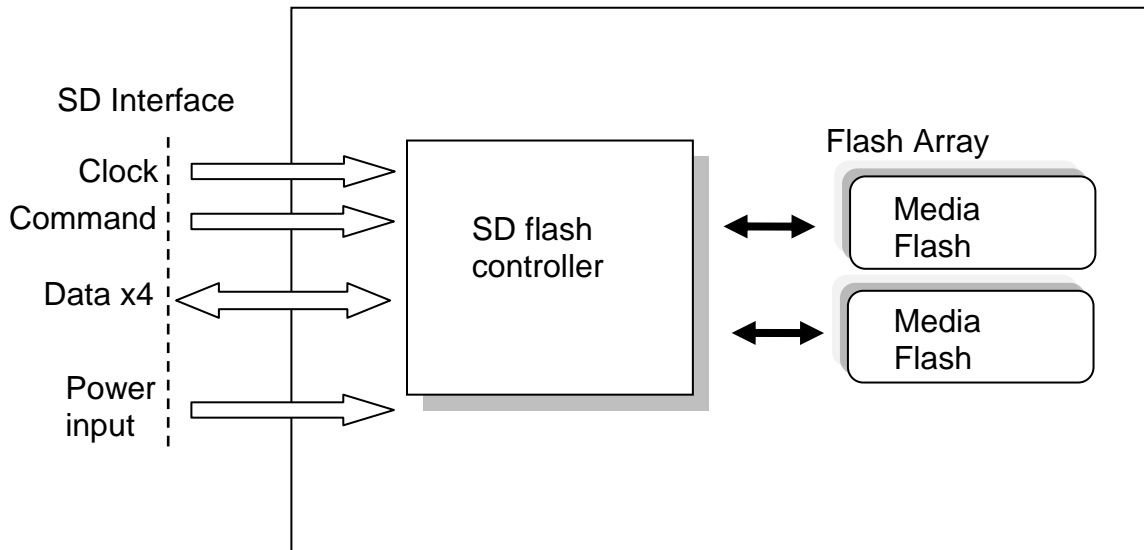
1. General Description

As the demand of reliable and high-performance data storage in a small form factor increases, Apacer's SD card is designed specifically for rigorous applications by offering maximum endurance, reliability, and agility, where extreme traceability, enhanced data integrity, and exceptionally velocity are required.

Regarding compatibility, this industrial SD card is compatible with SD Memory Card Specifications, Physical Layer specification, File System Specification and Part 3 Security Specification. Furthermore, the SD card is compatible with SD protocol. With built in ECC, wear-leveling and bad block management, this industrial SD card serves as an ideal portable storage solution.

1.1 Product Function Block

The SD contains a flash controller and flash media with SD standard interface.



1.2 Flash Management

The embedded SD device contains a high level, intelligent subsystem that provides many capabilities including:

- Bad block management
- ECC algorithms
- S.M.A.R.T
- Power management
- Global wear-leveling algorithms

1.2.1 Bad Block Management

The SD controller contains logic/physical flash block mapping and bad block management system. It will manage all flash block include user data space and spare block.

The SD also contains a sophisticated defect and error management system. It does a read after write under margin conditions to verify that the data is written correctly (except in the case of write pre-erased sectors). In case that a bit is found to be defective, the SD replaces this bad bit with a spare bit within the sector header. If necessary, the SD will even replace the entire sector with a spare sector. This is completely transparent to the master (host device) and does not consume any user data space.

1.2.2 ECC Algorithms

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, this SD card applies the BCH ECC Algorithm, which can detect and correct errors occur during read process, ensure data been read correctly, as well as protect data from corruption.

1.2.3 S.M.A.R.T

S.M.A.R.T. (SMART), an acronym stands for Self-Monitoring, Analysis and Reporting Technology, is an open standard allowing an individual disk drive in the ATA/IDE or SCSI interface to automatically monitor its own health and report potential problems in order to prevent data loss. This failure warning technology provides predictions from unscheduled downtime by observing and storing critical drive performance and calibration parameters. Ideally, this should allow taking hands-on actions to keep from impending drive failure.

Failures are divided into two categories: those that can be predicted and those that cannot. Predictable failures occur gradually over time, and the decline in performance can be detected; on the other hand, unpredictable failures happen very sudden without any warning. These failures may be caused by power surges or related to electronic components. The purpose of the SMART implementation is to predict near-term failures of each individual disk drive and generate a warning to prevent unfortunate loss.

1.2.4 Power Management

A power saving feature of the SD is automatic entrance and exit from sleep mode. Upon completion of an operation, the SD will enter the sleep mode to conserve power if no further commands are received within X seconds, where X is programmable by software. The master does not have to take any action for this to occur. The SD is in sleep mode except when the host is accessing it, thus conserving power.

Any command issued by the master to the SD will cause it to exit sleep mode and response to the master.

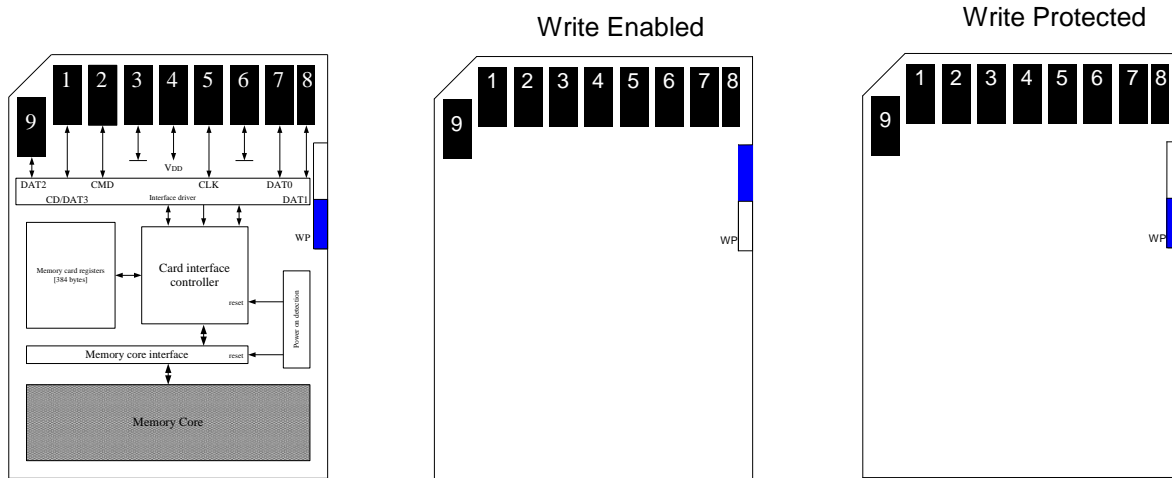
1.2.5 Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some area get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling technique is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

Apacer provides wear leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND Flash is greatly improved.

2. Electrical Characteristics

2.1 Card Architecture



2.2 Pin Assignment

Pin	SD Mode		SPI Mode	
	Name	Description	Name	Description
1	CD/DAT3	Card detect/Data line[Bit 3]	CS	Chip select
2	CMD	Command/Response	DI	Data in
3	VSS1	Supply voltage ground	VSS	Supply voltage ground
4	VDD	Supply voltage	VDD	Supply voltage
5	CLK	Clock	SCLK	Clock
6	VSS2	Supply voltage ground	VSS2	Supply voltage ground
7	DAT0	Data line[Bit 0]	DO	Data out
8	DAT1	Data line[Bit 1]	Reserved	
9	DAT2	Data line[Bit 2]	Reserved	

2.3 Capacity Specifications

The following table shows the specific capacity for the SD card.

Capacity	Total Bytes
1 GB	969,605,120
2 GB	1,938,489,344
4 GB	3,875,504,128
8 GB	7,751,073,792
16 GB	15,510,503,424

Note: The statistics may vary depending on file systems of various OS. User data bytes do not indicate total useable bytes. LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

2.4 Performance Specifications

Performances of the SD card are shown in the table below.

Modes \ Capacity	1 GB	2 GB	4 GB	8 GB	16 GB
Read (MB/s)	23	23	43	43	43
Write (MB/s)	15	18	35	39	41

Note: results may vary depending on settings and platforms.

2.5 DC Power Supply

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Power Supply Voltage	2.7	3.3	3.6	V

2.6 Power Consumption

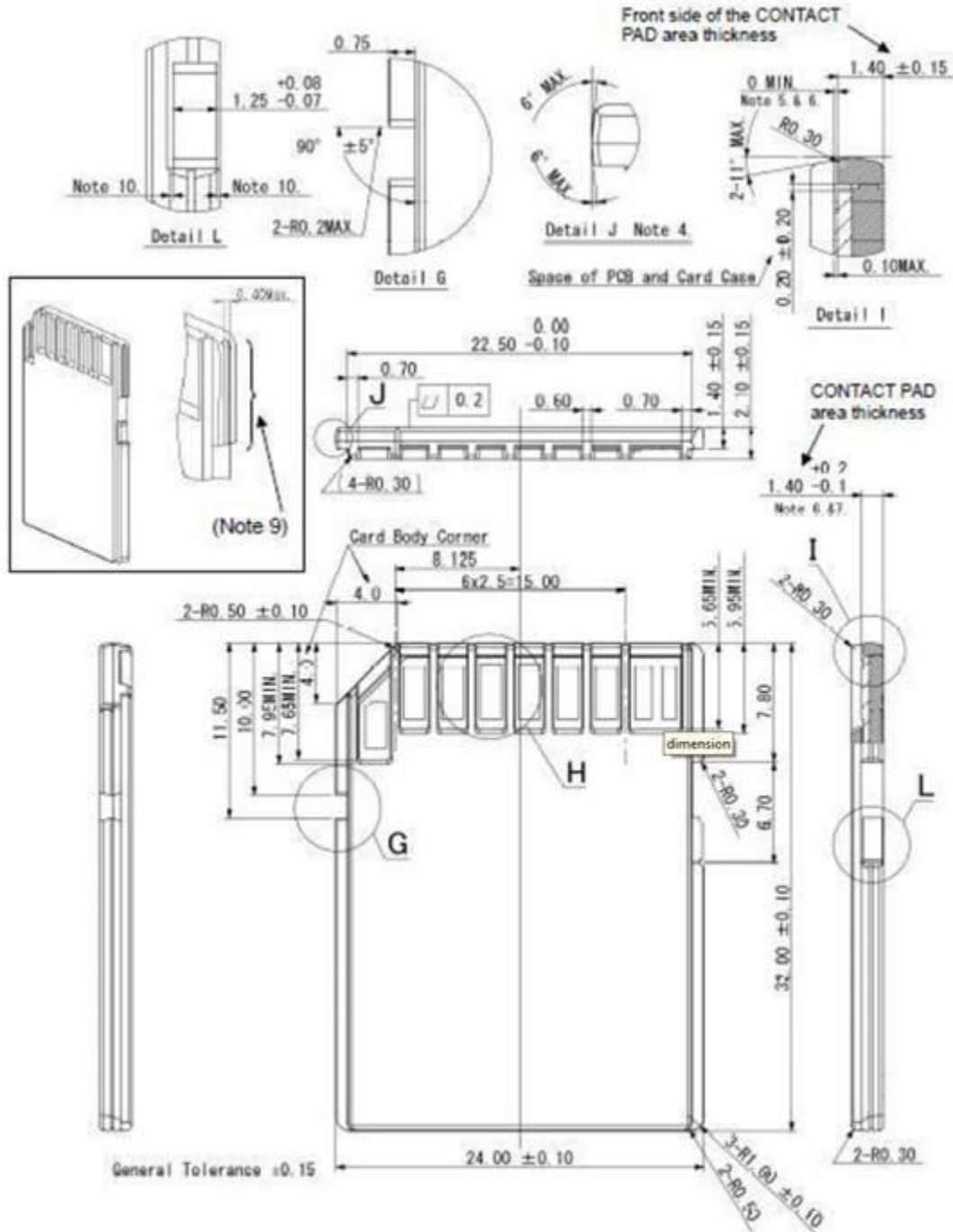
Modes \ Capacity	1 GB	2 GB	4 GB	8 GB	16 GB
Operating (mA)	75	80	120	115	120
Standby (μA)	150	160	240	245	260

Note: results may vary depending on settings and platforms.

3. Physical Characteristics

3.1 Physical Dimensions

Dimensions: 32 mm (L) x 24 mm (W) x 2.1 mm (H)

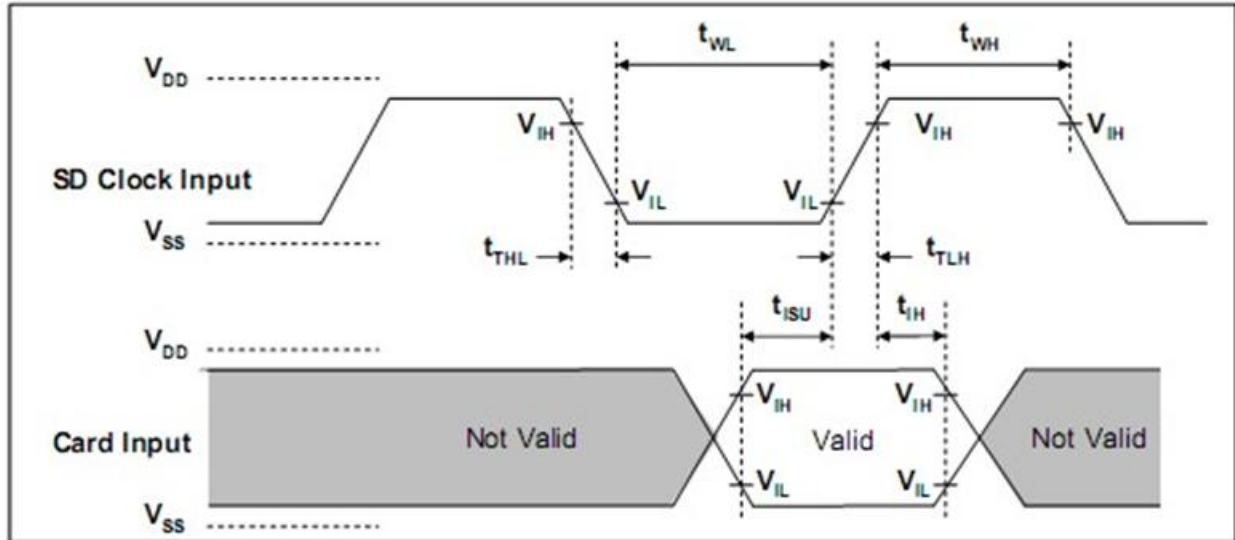


3.2 Durability Specifications

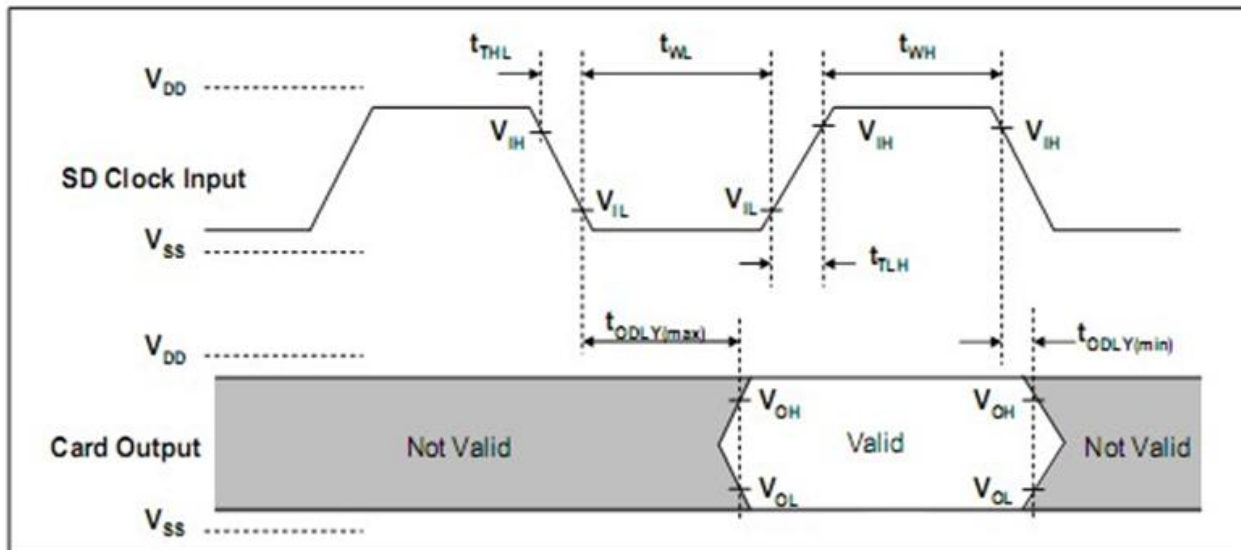
Item	Specifications
Temperature	-40°C to 85°C (Operating)
	-40°C to 85°C (Storage)
Shock	1,500G, 0.5ms
Vibration	20Hz~80Hz/1.52mm (frequency/displacement) 80Hz~2000Hz/20G (frequency/displacement) X, Y, Z axis/60mins each
Drop	1.5m free fall, 6 surfaces of each
Bending	≥ 10N, hold 1min/5times
Torque	0.15N-m or 2.5deg, hold 30 seconds/ 5 times
Salt spray	Concentration: 3% NaCl at 35°C (storage for 24 hours)
Waterproof	JIS IPX7 compliance, Water temperature 25°C Water depth: the lowest point of unit is locating 1000mm below surface (storage for 30 mins)
X-Ray Exposure	0.1 Gy of medium-energy radiation (70 KeV to 140 KeV, cumulative dose per year) to both sides of the card ;storage for 30 mins)
Switch cycle	0.4~0.5N, 1000 times
Durability	10,000 times mating cycle
ESD	Contact: +/-4KV each item 25 times Air: +/-8KV 10 times

4. AC Characteristics

4.1 SD Interface Timing (Default)



Card input Timing (Default Speed Card)

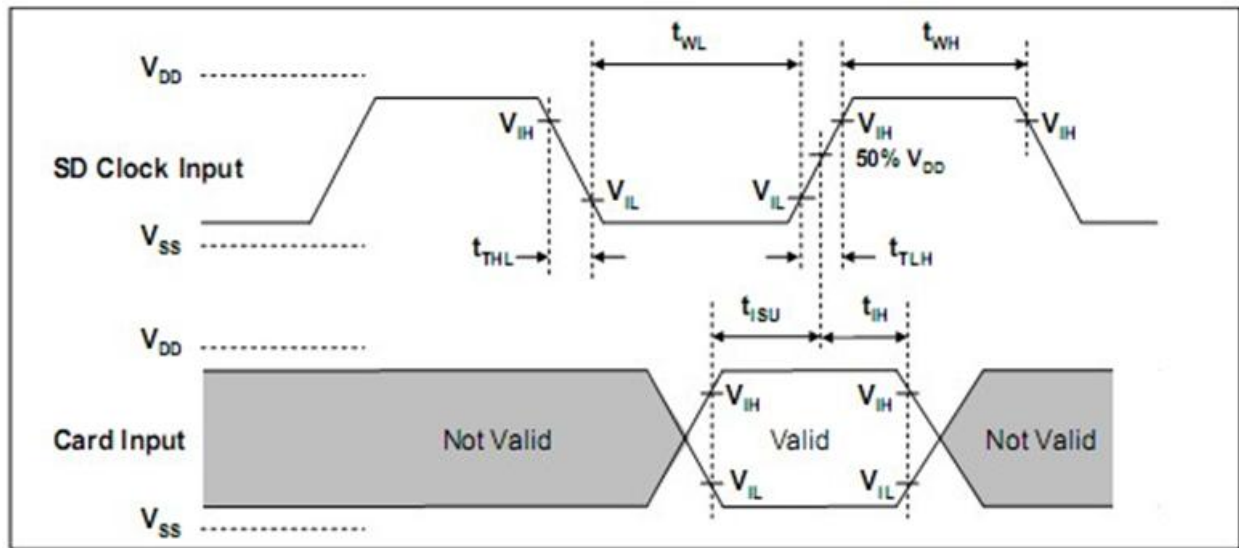


Card Output Timing (Default Speed Mode)

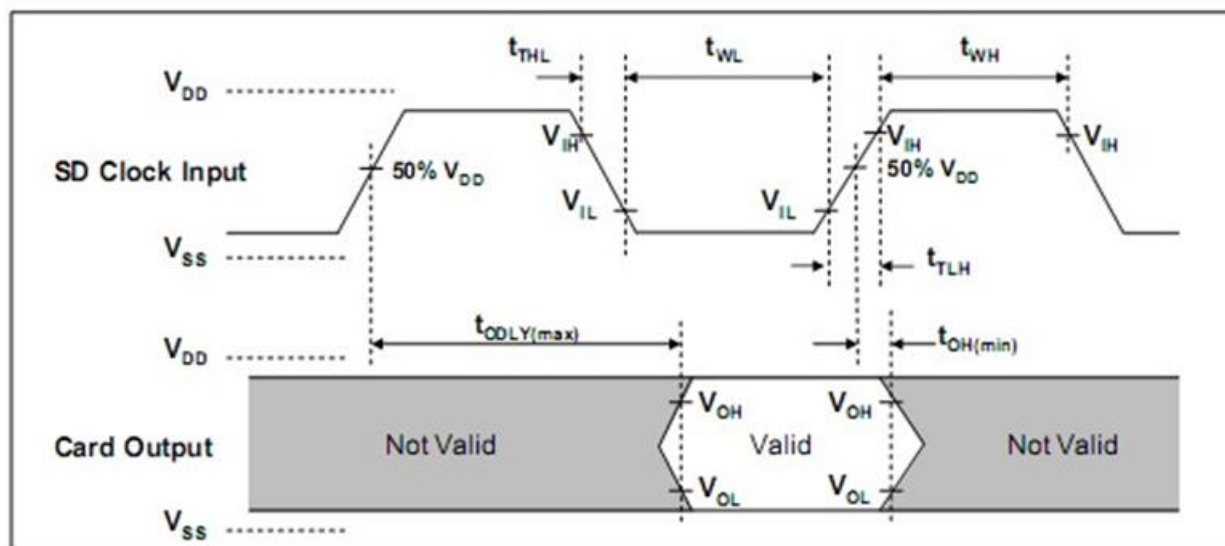
SYMBOL	PARAMETER	MIN	MAX	UNIT	REMARK
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
f _{PP}	Clock frequency data transfer	0	25	MHz	C _{card} ≤ 10 pF (1 card)
f _{OD}	Clock frequency identification	0 ⁽¹⁾ /100	400	KHz	C _{card} ≤ 10 pF (1 card)
t _{WL}	Clock low time	10	-	ns	C _{card} ≤ 10 pF (1 card)
t _{WH}	Clock high time	10	-	ns	C _{card} ≤ 10 pF (1 card)
t _{TLH}	Clock rise time	-	10	ns	C _{card} ≤ 10 pF (1 card)
t _{THL}	Clock fall time	-	10	ns	C _{card} ≤ 10 pF (1 card)
Inputs CMD, DAT (Referenced to CLK)					
t _{ISU}	Input setup time	5	-	ns	C _{card} ≤ 10 pF (1 card)
t _{IH}	Input hold time	5	-	ns	C _{card} ≤ 10 pF (1 card)
Outputs CMD, DAT (Referenced to CLK)					
t _{ODLY}	Output delay time during data transfer mode	0	14	ns	C _L ≤ 40 pF (1 card)
t _{OH}	Output hold time	0	50	ns	C _L ≤ 40 pF (1 card)

(1)0Hz means to stop the clock. The given minimum frequency range is for cases that require the clock to be continued.

4.2 SD Interface Timing (High Speed Mode)



Card Input Timing (High Speed Card)



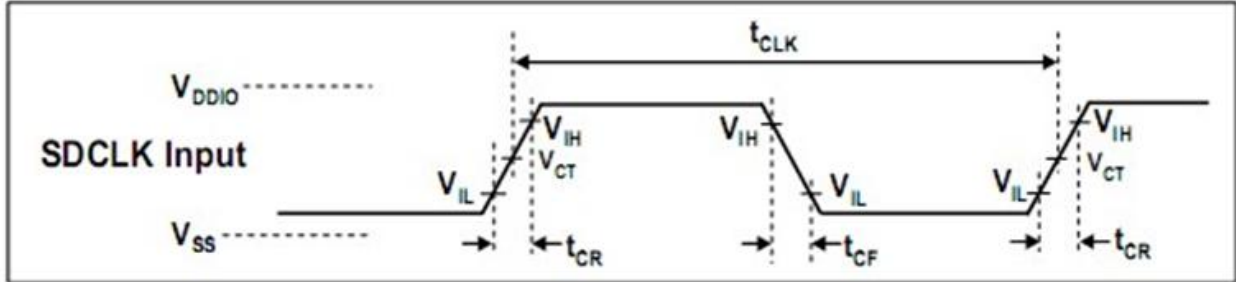
Card Output Timing (High Speed Mode)

SYMBOL	PARAMETER	MIN	MAX	UNIT	REMARK
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
f_{PP}	Clock frequency data transfer	0	50	MHz	$C_{card} \leq 10$ pF (1 card)
t_{WL}	Clock low time	7	-	ns	$C_{card} \leq 10$ pF (1 card)
t_{WH}	Clock high time	7	-	ns	$C_{card} \leq 10$ pF (1 card)
t_{TLH}	Clock rise time	-	3	ns	$C_{card} \leq 10$ pF (1 card)
t_{THL}	Clock fall time	-	3	ns	$C_{card} \leq 10$ pF (1 card)
Inputs CMD, DAT (Referenced to CLK)					
t_{ISU}	Input setup time	6	-	ns	$C_{card} \leq 10$ pF (1 card)
t_{TH}	Input hold time	2	-	ns	$C_{card} \leq 10$ pF (1 card)
Outputs CMD, DAT (Referenced to CLK)					
t_{ODLY}	Output delay time during data transfer made	-	14	ns	$CL \leq 40$ pF (1 card)
t_{OH}	Output hold time	2.5	-	ns	$CL \geq 15$ pF (1 card)
C_L	Total system capacitance for each line*	-	40	pF	1 card

*In order to satisfy severe timing, host shall run on only one card

4.3 SD Interface Timing (SDR12, SDR25, SDR50 and SDR104 Modes) Input

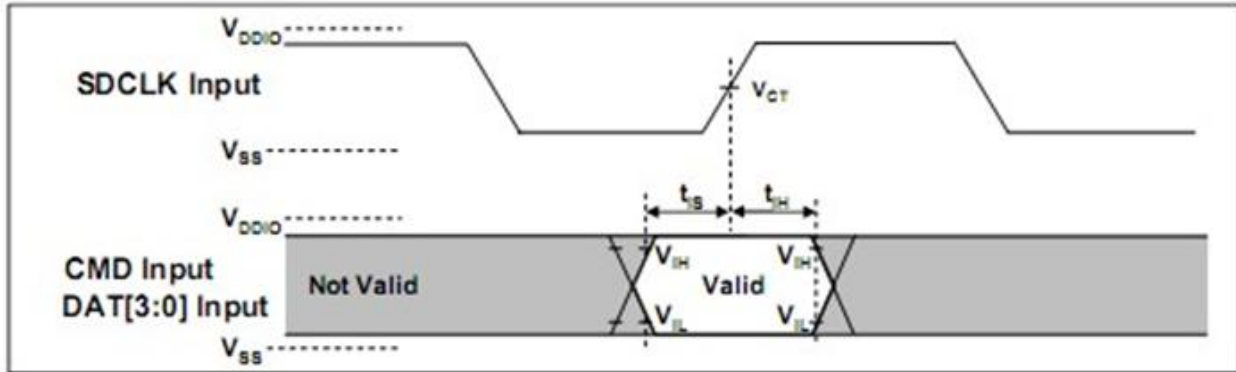
4.3.1 Clock Timing



Clock Signal Timing

SYMBOL	MIN	MAX	UNIT	REMARK
t_{CLK}	4.8	-	ns	208MHz (Max.), Between rising edge, $V_{CT} = 0.975V$
t_{CR}, t_{CF}	-	$0.2 * t_{CLK}$	ns	$t_{CR}, t_{CF} < 2.00ns$ (max.) at 208MHz, $C_{CARD}=10pF$ $t_{CR}, t_{CF} < 2.00ns$ (max.) at 100MHz, $C_{CARD}=10pF$ The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	

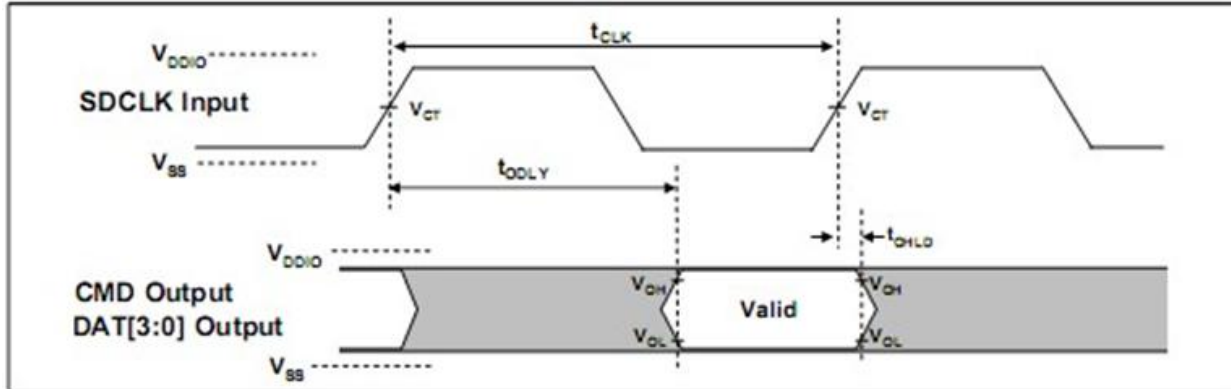
4.3.2 Card Input Timing



Card Input Timing

SYMBOL	MIN	MAX	UNIT	SDR104 MODE
t_{IS}	1.40	-	ns	$C_{CARD} = 10pF, V_{CT} = 0.975V$
t_{IH}	0.80	-	ns	$C_{CARD} = 5pF, V_{CT} = 0.975V$
SYMBOL	MIN	MAX	UNIT	SDR12, SDR25 and SDR50 MODES
t_{IS}	3.00	-	ns	$C_{CARD} = 10pF, V_{CT} = 0.975V$
t_{IH}	0.80	-	ns	$C_{CARD} = 5pF, V_{CT} = 0.975V$

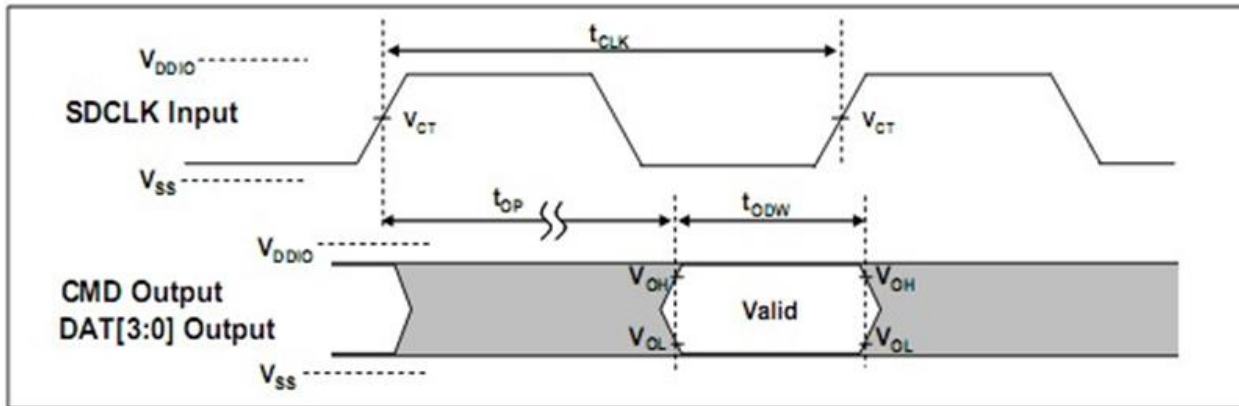
4.3.3 Card Output Timing of Fixed Data Window (SDR12, SDR25 and SDR50)



Output Timing of Fixed Date Window

SYMBOL	MIN	MAX	UNIT	REMARK
t_{ODLY}	-	7.5	ns	$t_{CLK} \geq 10.0ns$, $CL=30pF$, using driver Type B, for SDR50.
t_{ODLY}	-	14	ns	$t_{CLK} \geq 20.0ns$, $CL=40pF$, using driver Type B, for SDR25 and SDR12.
t_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.). $CL=15pF$

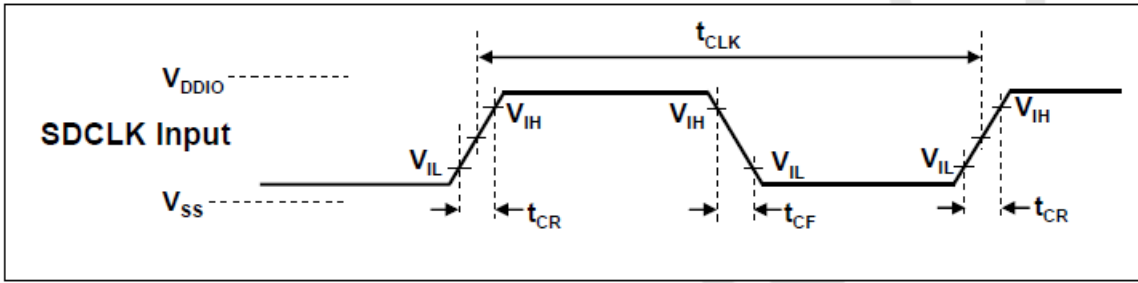
4.3.4 Output Timing of Variable Window (SDR104)



Output Timing of Variable Data Window

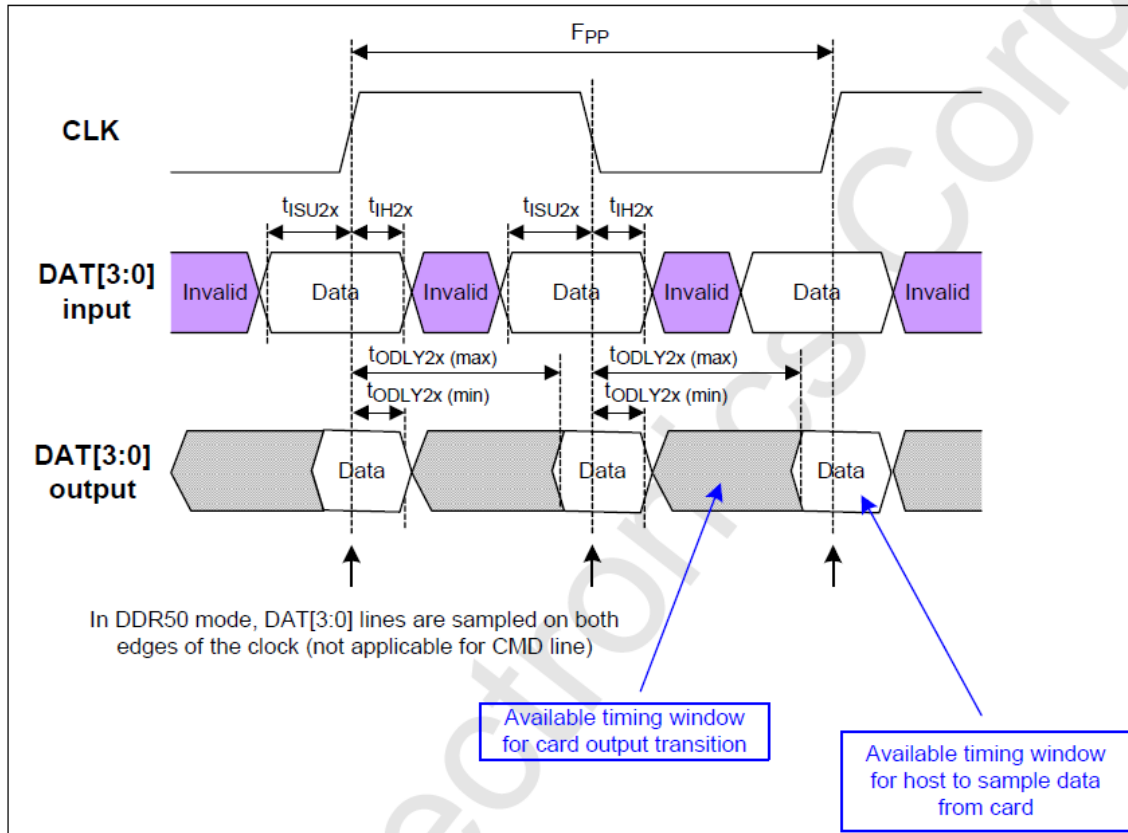
SYMBOL	MIN	MAX	UNIT	REMARK
t_{OP}	-	2	UI	Card Output Phase
Δt_{OP}	-350	+1550	ps	Delay variation due to temperature change after tuning
t_{ODW}	0.60	-	UI	$t_{ODW} = 2.88ns$ at 208MHz

4.3.5 SD Interface Timing (DDR50 Mode)



Clock Signal Timing

SYMBOL	MIN	MAX	UNIT	REMARK
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	$0.2 * t_{CLK}$	ns	$t_{CR}, t_{CF} < 4.00ns$ (max.) at 50MHz, CCARD=10pF
Clock Duty	45	55	%	



Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

4.3.6 Bus Timings – Parameters Values (DDR50 Mode)

Symbol	Parameters	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
t _{ISU}	Input set-up time	6	-	ns	C _{card} ≤ 10 pF (1 card)
t _{IH}	Input hold time	0.8	-	ns	C _{card} ≤ 10 pF (1 card)
Output CMD (referenced to CLK rising edge)					
t _{ODLY}	Output Delay time during Data Transfer Mode	-	13.7	ns	C _L ≤ 30 pF (1 card)
T _{OH}	Output Hold time	1.5	-	ns	C _L ≥ 15 pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
t _{ISU2x}	Input set-up time	3	-	ns	C _{card} ≤ 10 pF (1 card)
t _{IH2x}	Input hold time	0.8	-	ns	C _{card} ≤ 10 pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
t _{ODLY2x}	Output Delay time during Data Transfer Mode	-	7.0	ns	C _L ≤ 25 pF (1 card)
T _{OH2x}	Output Hold time	1.5	-	ns	C _L ≥ 15 pF (1 card)

5. S.M.A.R.T.

5.1 SMART Getting Flow Chart

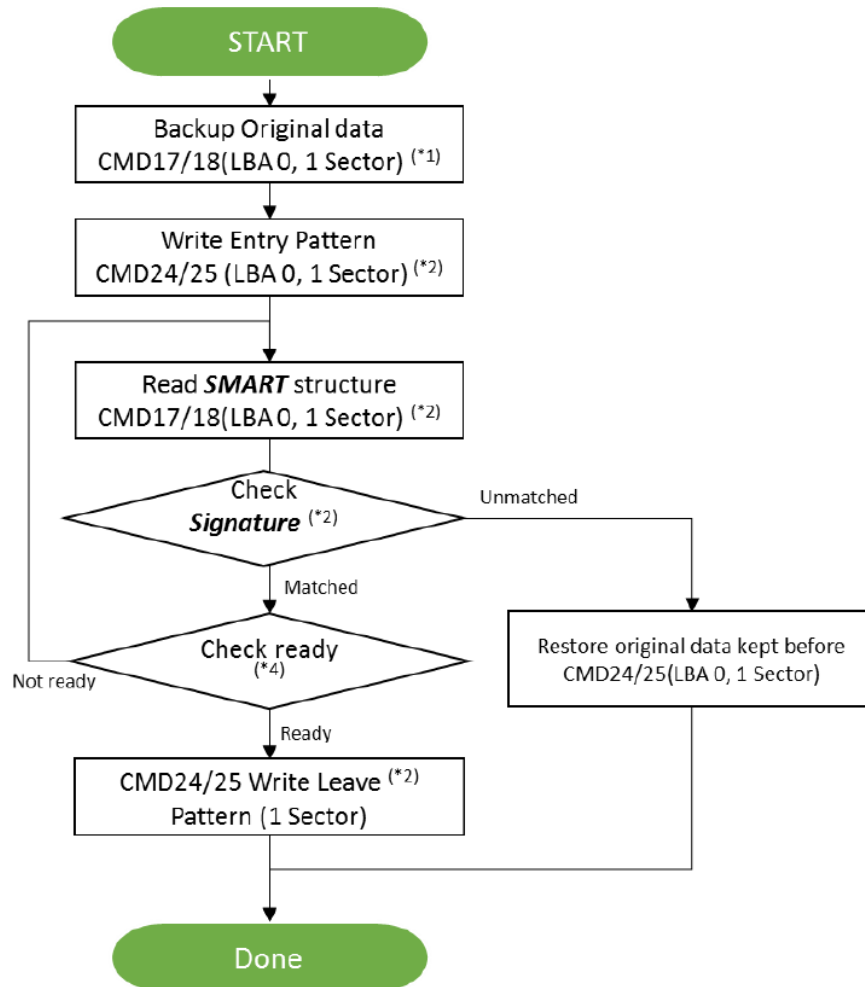


Figure 5-1 SMART Getting Flow Chart

(*1) Due to the SMART Read Flow is started by a **Write** command, the **backup-and-restore** activity is suggested to save the data in other storage media that aren't R1 products.

(*2) The **Arguments** of the SD CMD24/CMD25/CMD17/CMD18 (or the **LBA** of the SCSI Read/Write) should be **0**.

(*3) The first 3 bytes of the Read command returned data, called **Signature**, should be **53h, 49h** and **30h**. It confirms that the hardware accepted the SMART Entry Pattern for starting the SMART process.

(*4) After issuing Entry Pattern, the device starts to process preparing the SMART data. It may takes some time so that the AP should issue the Read Command repeatedly and check byte[73] of the returned data. **When byte[73] returned 1 it indicates that the data is busy and 0 for the data is ready**. Until byte[73] returned as ready, the others bytes in the returned data is available simultaneously.

5.2 The Entry Pattern and Leave Pattern

5.2.1 Entry Pattern (LBA: 0)

N	N+0	N+1	N+2	N+3	N+4	N+5	N+6	N+7
000	36h	39h	36h	36h	38h	33h	30h	33h
007 ⋮ 246	All Zero (240 Bytes)							
247	33h	30h	33h	38h	36h	36h	39h	36h
256	02h	39h	36h	36h	38h	33h	30h	33h
264 ⋮ 503	All Zero (240 Bytes)							
504	33h	30h	33h	38h	36h	36h	39h	36h

5.2.2 Leave Pattern (LBA: 0)

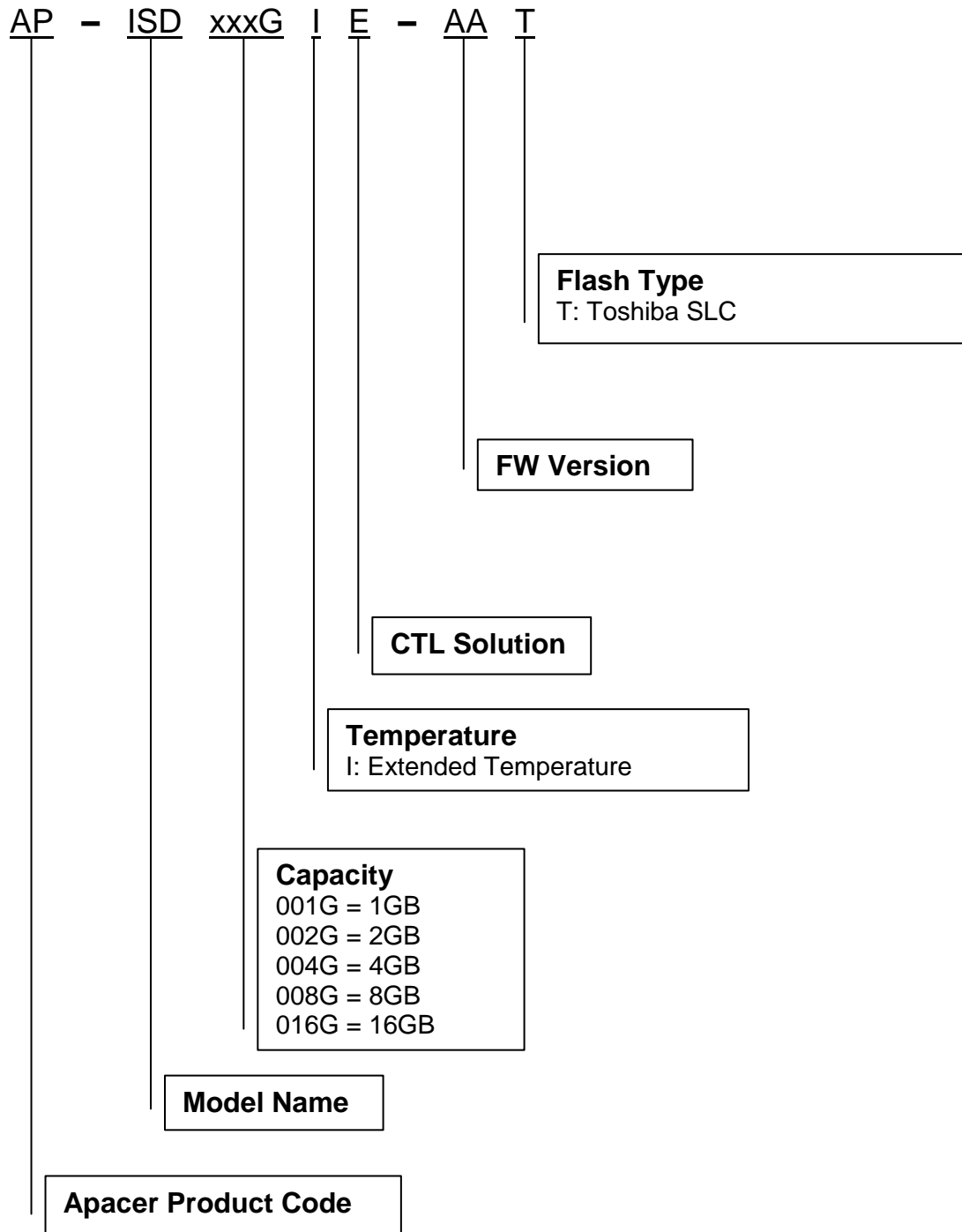
N	N+0	N+1	N+2	N+3	N+4	N+5	N+6	N+7
000	33h	30h	33h	38h	36h	36h	39h	36h
007 ⋮ 246	All Zero (240 Bytes)							
247	36h	39h	36h	36h	38h	33h	30h	33h
256	33h	30h	33h	38h	36h	36h	39h	36h
264 ⋮ 503	All Zero (240 Bytes)							
504	02h	39h	36h	36h	38h	33h	30h	33h

5.3 SMART Returned Table

Location	Digits	Name	Description
0-2	3	Signature	53h 49h 30h
3-18	16	Reserved	Reserved
19-34	16	Reserved	Reserved
35	1	Flash Type	0: SLC, 1: MLC
36-41	6	Flash ID	Flash ID Numbers
42-45	4	Flash PE Cycle	Flash P/E Cycle Times
46-49	4	Reserved	Reserved
50-51	2	Initial Bad Block Count	Physical number of bad blocks marked by factory
52-53	2	Later Bad VB	The number of bad blocks in virtual unit marked at run time
54-55	2	Spare Block Count	Spare Block Count
56	1	Reserved	Reserved
57-60	4	Total Erase Count	0 - 4294967295
61-64	4	Abnormal Shut Down Count	The number of abnormal unplug/power down times detected by the device
65-68	4	Power Cycle Count	The number of re-plug times
69-70	2	Reserved	Reserved
71	1	Total CE Count	NAND CE number of the device
72	1	VB Multiplier	The multiplier to convert Virtual Block Numbers to Physical Block Numbers
73	1	SMART Data Ready	Returns 1 for indicating preparing data; 0 for indicating that the data is ready
74-75	2	MP Version (High)	3 rd number of the MP Version in 16 bits
76-77	2	MP Version (Low)	4 th number of the MP Version in 16 bits
78-81	4	Total Virtual Blocks	The Total Physical Blocks / VB Multiplier
82-511	430	Reserved	Reserved

6. Product Ordering Information

6.1 Product Code Designations



6.2 Valid Combinations

Capacity	AP/N
1GB	AP-ISD001GIE-AAT
2GB	AP-ISD002GIE-AAT
4GB	AP-ISD004GIE-AAT
8GB	AP-ISD008GIE-AAT
16GB	AP-ISD016GIE-AAT

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Revision History

Revision	Description	Date
1.0	Official release	12/22/2015
1.1	- Added S.M.A.R.T. chapter - Revised product ordering information	1/19/2016

Global Presence

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China	Apacer Electronic (Shanghai) Co., Ltd Room D, 22/FL, No.2, Lane 600, JieyunPlaza, Tianshan RD, Shanghai, 200051, China Tel: 86-21-6228-9939 Fax: 86-21-6228-9936 sales@apacer.com.cn
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