Apacer

Industrial SD Card 3.0

H1-M Product Specifications

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Version 2.5

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Product Features

- Compliant with SD Memory Card Specifications
  - Part 1 Physical Layer Specification Ver3.0
  - Part 2 File System Specification Ver3.0
  - Part 3 Security Specification Ver3.0
- Capacity: 8, 16, 32, 64, 128 GB
- NAND flash type: MLC
- Operating voltage range: 2.7V~3.6V
- SD card form factor: 32mm (L) x 24mm (W) x 2.1mm (H)
- Temperature range
  - Operating: -25°C to 85°C (Standard) and -40°C to 85°C (Wide)
  - Storage: -40°C to 85°C
- Speed class: Class 10
- SD Card protocol compatible
- Supports SD and SPI modes
- Bus Speed Mode[1] (using 4 parallel data lines): UHS-I
  - SDR12: SDR up to 25MHz 1.8V signaling
  - SDR25: SDR up to 50MHz 1.8V signaling
  - SDR50: 1.8V signaling, frequency up to 100MHz, up to 50 MB/sec
  - SDR104: 1.8V signaling, frequency up to 208MHz, up to 104 MB/sec
  - DDR50: 1.8V signaling, frequency up to 50MHz, sampled on both clock edges, up to 50 MB/sec
- Flash management
  - Error Correction/Detection, Global Wear Leveling, Bad Block Management, Power Failure Management, S.M.A.R.T., Smart Read Refresh™
- Enhanced security
  - Mechanical Write Protect Switch
  - Built-in write protection features (permanent and temporary)
- High reliability
  - Specifically designed for the industrial market, ideal for read-intensive applications such as navigation, infotainment, POS/POI systems, medical devices, and general boot media use cases
  - Supports MTBF of more than 3,000,000 hours
  - Supports up to 3,000 P/E cycles
  - Supports up to 10,000 card insertions and removals
- RoHS Compliant

Note 1: Timing in 1.8V signaling is different from that of 3.3V signaling.

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1. General Description

Apacer Industrial H1-M SD card is designed specifically for rigorous applications. It offers maximum endurance, reliability, and agility, making it ideal for scenarios that require extreme traceability, enhanced data integrity, and exceptional speed.

This industrial SD card is compatible with SD Memory Card Specifications, including the Physical Layer, File System, and Security specifications. It can switch between SD mode and SPI mode communication protocols. In terms of flash management, the card incorporates various advanced capabilities to extend product endurance and increase data reliability, including built-in ECC, global wear leveling, bad block management, Power Failure Management, Smart Read Refresh, and S.M.A.R.T.

With enhanced reliability and wide compatibility, Apacer Industrial H1-M SD card is an ideal solution for hand-held applications, especially in semi-industrial and medical markets, thanks to its customized firmware techniques.

2. Functional Block

The SD contains a flash controller and flash media with SD standard interface.

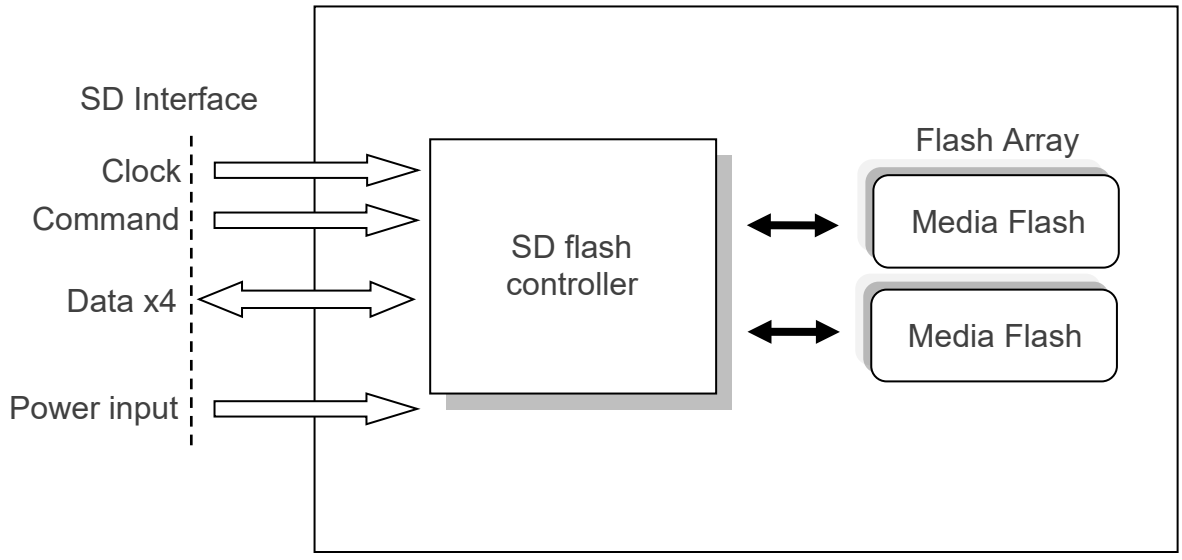


Figure 2-1 Functional Block Diagram

3. Electrical Interface Outlines

3.1 SD Card Pin Assignment

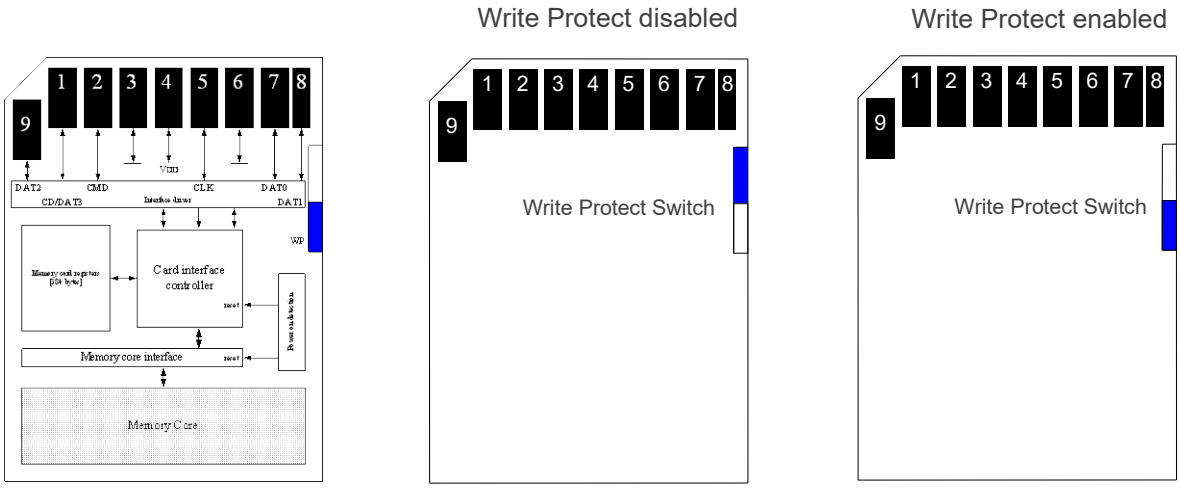


Figure 3-1 SD Card Pin Assignment

Table 3-1 SD Card Pin Assignment

Pin	SD Mode			SPI Mode		
	Name	Type[1]	Description	Name	Type	Description
1	CD/DAT3[2]	I/O/PP[3]	Card Detect/ Data Line [bit 3]	CS	I[3]	Chip Select (negative true)
2	CMD	PP	Command/Response	DI	I	Data In
3	VSS1	S	Supply voltage ground	VSS	S	Supply voltage ground
4	VDD	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	VSS2	S	Supply voltage ground	VSS2	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [bit 0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line [bit 1]	RSV		
9	DAT2	I/O/PP	Data Line [bit 2]	RSV		

Notes:
1. S: power supply, I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers.
2. The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used.
3. At power up, this line has a 50KOhm pull up enabled in the card. This resistor serves two functions: Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode, it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user during regular data transfer with SET_CLR_CARD_DETECT (ACMD42) command.

3.2 SD Card Bus Topology

The SD card supports two communication protocols: SD and SPI. The host system can choose either one of these modes. The card detects which mode is requested by the host when the reset command is received and expects all further communication to be in the same mode. The SD mode supports 4-bit high-performance data transfer, while the SPI mode offers only 1-bit data transfer, delivering lower performance than SD mode.

4. Product Specifications

4.1 Capacity

Table 4-1 Capacity Specifications

Capacity	Total bytes
8 GB	7,960,788,992
16 GB	15,997,075,456
32 GB	32,082,231,296
64 GB	64,156,073,984
128 GB	128,278,593,536

Note: The statistics may vary depending on file systems of various OS. User data bytes do not indicate total useable bytes. LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

4.2 Performance

Table 4-2 Performance Specifications

Capacity	Speed Class	Sequential (MB/s)	
		Read	Write
8 GB	C10	43	26
16 GB	C10	43	23
32 GB	C10	43	30
64 GB	C10	43	22
128 GB	C10	43	22

Notes:
- Results may differ from various flash configurations or host system setting.
- Sequential read/write is based on CrystalDiskMark 5.2.1 with file size 1,000MB.

4.3 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) indicates a device's reliability by representing the average time between one repair and the next failure. This metric is usually expressed in hours. A higher MTBF value signifies greater device reliability.

Table 4-3 Mean Time Between Failures

Analysis Method	MTBF (Hours)
Telcordia Technologies Special Report, SR-332, Issue 3 method	>3,000,000

4.4 Endurance

The endurance of a storage device is predicted by TeraBytes Written based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

Table 4-4 Endurance Specifications

Capacity	TeraBytes Written
8 GB	4
16 GB	9
32 GB	18
64 GB	37
128 GB	75

Notes:
- This estimation complies with Apacer internal workload.
- Flash vendor guaranteed MLC P/E cycles: 3K
- WAF may vary from capacity, flash configurations and writing behavior on each platform.
- 1 Terabyte = 1,024GB

4.5 Reliability and Durability

Table 4-5 Reliability and Durability

Parameter		Specification
Temperature	Operating	-25°C to 85°C (Standard); -40°C to 85°C (Wide)
	Storage	-40°C to 85°C
Shock		1,500G, 0.5ms
Vibration		20Hz~80Hz/1.52mm (frequency/displacement) 80Hz~2000Hz/20G (frequency/displacement) X, Y, Z axis/60mins each
Drop		150cm free fall, 6 face of each
Bending		≧10N, hold 1min/5times
Torque		0.15N-m or 2.5deg, hold 30 seconds/5times
Salt Spray		Concentration: 3% NaCl at 35°C (storage for 24 hours)
Waterproof		JIS IPX7 compliance. Water temperature: 25°C Water depth: the lowest point of unit is locating 1000mm below surface (storage for 30 mins)
X-Ray Exposure		0.1 Gy of medium-energy radiation (70 KeV to 140 KeV, cumulative dose per year) to both sides of the card (storage for 30 mins)
Switch cycle		0.4~0.5N, 1000 times
Durability		10,000 times mating cycle
ESD		Contact: +/-4KV each item 25 times Air: +/-8KV 10 times

5. Flash Management

5.1 Error Correction/Detection

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, the SD card applies the advanced ECC Algorithm, which can detect and correct errors occur during read process, ensure data been read correctly, as well as protect data from corruption.

5.2 Global Wear Leveling

NAND Flash devices can endure only a limited number of program/erase cycles, and flash media typically do not wear evenly. When certain areas are updated more frequently than others, the overall lifespan of the device can be significantly reduced. To address this, Global Wear Leveling is employed to extend the life of NAND Flash by evenly distributing program and erase cycles across the entire media.

Apacer's Global Wear Leveling algorithm efficiently balances flash usage throughout the full address space, preventing localized wear. By implementing this technology, the endurance and life expectancy of the NAND Flash are greatly enhanced.

5.3 Bad Block Management

The SD controller contains logical/physical flash block mapping and bad block management system. It will manage all flash block include user data space and spare block.

The SD also contains a sophisticated defect and error management system. It does a read after write under margin conditions to verify that the data is written correctly (except in the case of write pre-erased sectors). In case that a bit is found to be defective, the SD replaces this bad bit with a spare bit within the sector header. If necessary, the SD will even replace the entire sector with a spare sector. This is completely transparent to the master (host device) and does not consume any user data space.

5.4 Power Failure Management

Apacer industrial SD and microSD cards provide complete data protection mechanism during every abnormal power shutdown situation, such as power failure at programming data, updating system tables, erasing blocks, etc. Apacer Power-Loss Protection mechanism includes:

- Maintaining data correctness and increasing the reliability of the data stored in the NAND Flash memory.
- Protecting firmware table and the data written to flash from data loss in the event of power off.

5.6 S.M.A.R.T.

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is a special function that allows a memory device to automatically monitor its health. Apacer provides a program named SmartInfo Tool to observe Apacer's SD and microSD cards. Note that this tool can only support Apacer's industrial SD and microSD cards. This tool will display firmware version, endurance life ratio, good block ratio, and so forth.

5.7 Smart Read Refresh™

Apacer's Smart Read Refresh plays a proactive role in avoiding read disturb errors from occurring to ensure health status of all blocks of NAND flash. Developed for read-intensive applications in particular, Smart Read Refresh is employed to make sure that during read operations, when the read operation threshold is reached, the data is refreshed by re-writing it to a different block for subsequent use.

6. SD Card Comparison

Table 6-1 Comparing SDSC, SDHC, and SDXC

Item	SDSC	SDHC	SDXC
File System	FAT 12/16	FAT32	exFAT
Addressing Mode	Byte (1 byte unit)	Block (512 byte unit)	Block (512 byte unit)
HCS/CCS bits of ACMD41	Support	Support	Support
CMD8 (SEND_IF_COND)	Support	Support	Support
CMD16 (SET_BLOCKLEN)	Support	Support (Only CMD42)	Support (Only CMD42)
Partial Read	Support	Not Support	Not Support
Lock/Unlock Function	Mandatory	Mandatory	Mandatory
Write Protect Groups	Optional	Not Support	Not Support
Supply Voltage 2.7v – 3.6v (for operation)	Support	Support	Support
Total Bus Capacitance for each signal line	40pF	40pF	40pF
CSD Version (CSD_STRUCTURE Value)	1.0 (0x0)	2.0 (0x1)	2.0 (0x1)
Speed Class	Optional	Mandatory (Class 2 / 4 / 6 / 10)	Mandatory (Class 2 / 4 / 6 / 10)

Table 6-2 Comparing Speed Class Symbols

Item	C2 (Class 2)	C4 (Class 4)	C6 (Class 6)	C10 (Class 10)
Bus Mode	UHS-I/UHS-II			
SD Memory Card	SDSC, SDHC, SDXC			
Mark				
Min. Sequential Write Speed	2 MB/s	4 MB/s	6 MB/s	10 MB/s

Table 6-3 Comparing UHS Speed Grade Symbols

Item	U1 (UHS Speed Grade 1)	U3 (UHS Speed Grade 3)
Bus Mode	UHS-I /UHS-II	
SD Memory Card	SDHC, SDXC	
Mark		
Performance	10 MB/s minimum write speed	30 MB/s minimum write speed
Applications	Full higher potential of recording real-time broadcasts and capturing large-size HD videos.	Capable of recording 4K2K video.

Table 6-4 Comparing Video Speed Class Symbols

Item	V6 (Video Speed Class 6)	V10 (Video Speed Class 10)	V30 (Video Speed Class 30)	V60 (Video Speed Class 60)	V90 (Video Speed Class 90)
Bus Mode	High Speed/UHS-I/UHS-II		UHS-I/UHS-II	UHS-II	
SD Memory Card	SDHC, SDXC				
Mark					
Performance	6 MB/s minimum write speed	10 MB/s minimum write speed	30 MB/s minimum write speed	60 MB/s minimum write speed	90 MB/s minimum write speed
Applications	HD/FHD Video Recording	FHD Video Recording, HD Still Image, Continuous Shooting.		4K/2K Video Recording	8K/3D/360° Video Recording

Table 6-5 Comparing Application Performance Class Symbols

Item	A1 (Application Performance Class 1)	A2 (Application Performance Class 2)
Mark		
Min. Random Read	1500 IOPS	4000 IOPS
Min. Random Write	500 IOPS	2000 IOPS
Min. Sustained Sequential Write	10 MB/s	10 MB/s
Applications	Main target is uSD for Android mobile handset	

7. Electrical Specifications

7.1 Absolute Maximum Rating

Table 7-1 Absolute Maximum Rating

Parameter		Min.	Max.	Unit
Operating Temperature	Standard	-25	85	°C
	Wide	-40	85	°C
Storage Temperature		-40	85	°C

7.2 Power Requirement

Table 7-2 Power Requirement

Parameter	Symbol	Min.	Max.	Unit
Power Supply Voltage	V_{DD}	2.7	3.6	V

7.3 Power Consumption

Table 2-5 Power Consumption

Mode \ Capacity	8 GB	16 GB	32 GB	64 GB	128 GB	Unit
Operating (Max.)	75	75	110	135	145	mA
Standby	200	185	180	195	235	µA

Notes:
- All values are typical and may vary depending on flash configurations or host system settings.
- Based on USB 3.0 card reader, power consumption is measured using CrystalDiskMark 5.2.1 with file size 1,000MB.

7.4 DC Characteristics

7.4.1 Bus Operation Conditions for 3.3V Signaling

Table 7-4 Threshold Level for High Voltage Range

Parameter	Symbol	Min	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	V_{OH}	0.75*V_{DD}		V	I_{OH} = -2mA V_{DD} Min
Output Low Voltage	V_{OL}		0.125*V_{DD}	V	IOL = 2mA V_{DD} Min
Input High Voltage	V_{IH}	0.625*V_{DD}	V_{DD}+0.3	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3	0.25*V_{DD}	V	
Power Up Time			250	ms	From 0V to V_{DD} min

Table 7-5 Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max	Unit	Remark
Peak voltage on all lines		-0.3	V_{DD}+0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

Table 7-6 Threshold Level for 1.8V Signaling

Parameter	Symbol	Min	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Regulator Voltage	V_{DDIO}	1.7	1.95	V	Generated by V_{DD}
Output High Voltage	V_{OH}	1.4	-	V	I_{OH} = -2mA
Output Low Voltage	V_{OL}	-	0.45	V	I_{OL} = 2mA
Input High Voltage	V_{IH}	1.27	2.00	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3	0.58	V	

Table 7-7 Input Leakage Current for 1.8V Signaling

Parameter	Symbol	Min	Max	Unit	Remark
Input Leakage Current		-2	2	uA	DAT3 pull-up is disconnected.

7.4.2 Bus Signal Line Levels

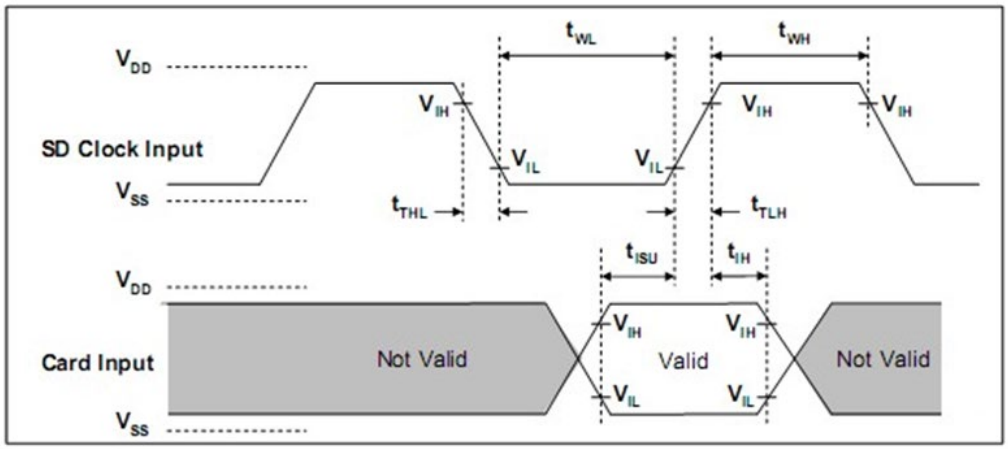
Total Bus Capacitance = C_{HOST} + C_{BUS} +NC_{CARD}

Table 7-8 Bus Signal Line Load

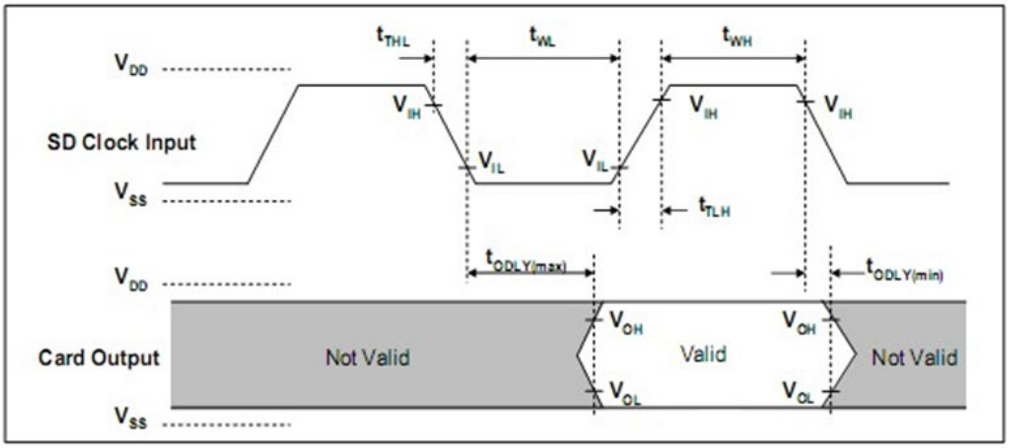
Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	kΩ	To prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1 card C_{HOST}+C_{BUS} shall not exceed 30pF
Card capacitance for each signal pin	C_{CARD}		10	pF	
Maximum signal line inductance			16	nH	
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	kΩ	May be used for card detection.
Capacity connected to power line	C_C		5	uF	To prevent inrush current

7.5 AC Characteristics

7.5.1 SD Interface Timing (Default)



Card input Timing (Default Speed Card)



Card Output Timing (Default Speed Mode)

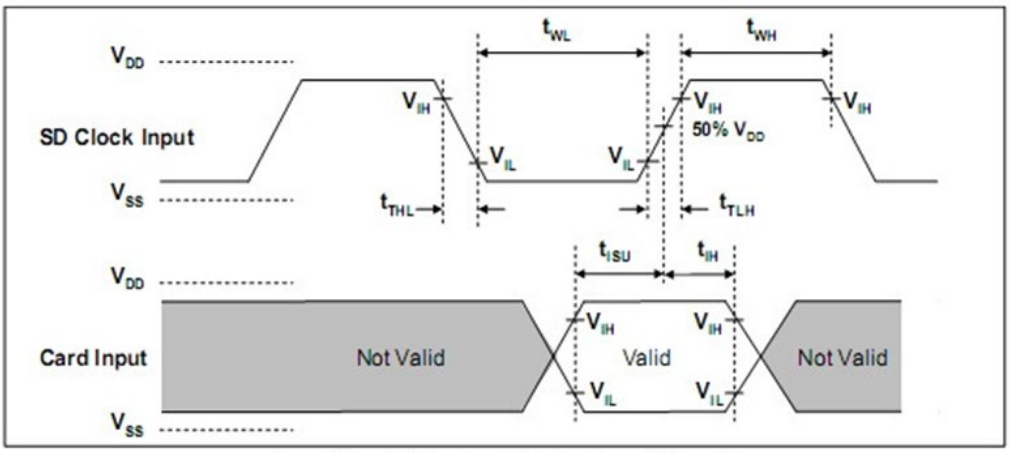
Table 7-9 SD Interface Timing (Default)

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	C_{card} ≤ 10 pF (1 card)
Clock frequency Identification Mode	f_{OD}	0[1]/100	400	kHz	C_{card} ≤ 10 pF (1 card)
Clock low time	t_{WL}	10		ns	C_{card} ≤ 10 pF (1 card)
Clock high time	t_{WH}	10		ns	C_{card} ≤ 10 pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{card} ≤ 10 pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{card} ≤ 10 pF (1 card)

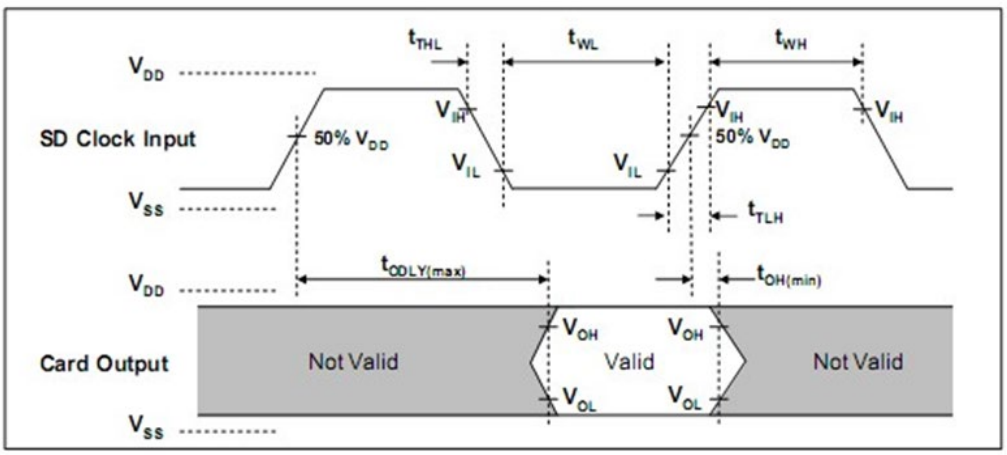
Inputs CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	5		ns	C_{card} ≤ 10 pF (1 card)
Input hold time	t_{IH}	5		ns	C_{card} ≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	C_L ≤ 40 pF (1 card)
Output Delay time during Identification Mode	t_{ODLY}	0	50	ns	C_L ≤ 40 pF (1 card)

Note 1: 0Hz means to stop the clock. The given minimum frequency range is for cases where continuous clock is required.

7.5.2 SD Interface Timing (High-Speed Mode)



Card Input Timing (High Speed Card)



Card Output Timing (High Speed Mode)

Table 7-10 SD Interface Timing (High-Speed Mode)

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	C_{card} ≤ 10 pF (1 card)
Clock low time	t_{WL}	7		ns	C_{card} ≤ 10 pF (1 card)
Clock high time	t_{WH}	7		ns	C_{card} ≤ 10 pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{card} ≤ 10 pF (1 card)
Clock fall time	t_{THL}		3	ns	C_{card} ≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	6		ns	C_{card} ≤ 10 pF (1 card)
Input hold time	t_{IH}	2		ns	C_{card}≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		14	ns	C_L ≤ 40 pF (1 card)
Output Hold Time	T_{OH}	2.5		ns	C_L ≤ 15 pF (1 card)
Total System capacitance of each line[1]	C_L		40	pF	C_L ≤ 15 pF (1 card)

Note 1: In order to satisfy severe timing, the host shall drive only one card.

7.5.3 SD Interface Timing (SDR12, SDR25, SDR50, and SDR104 Modes)

Input

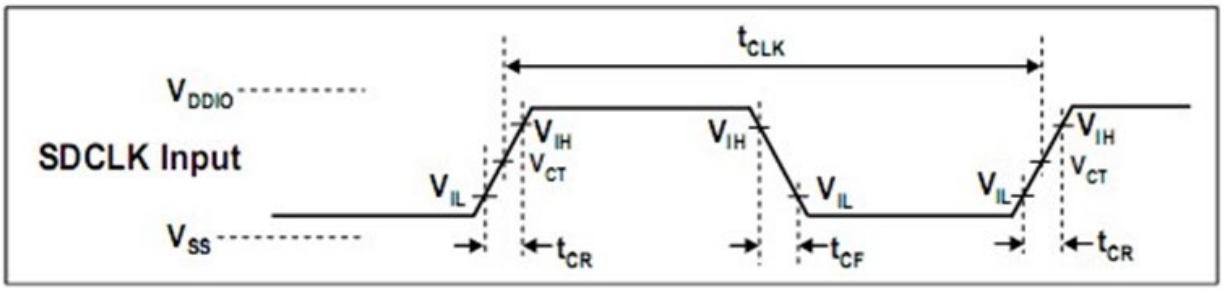


Table 7-11 Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	4.8	-	ns	208MHz (Max.), Between rising edge, V_{CT} = 0.975V
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 0.96ns (max.) at 208MHz, C_{CARD}=10pF t_{CR}, t_{CF} < 2.00ns (max.) at 100MHz, C_{CARD}=10pF The maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	

Input (SDR50 and SDR104 Modes)

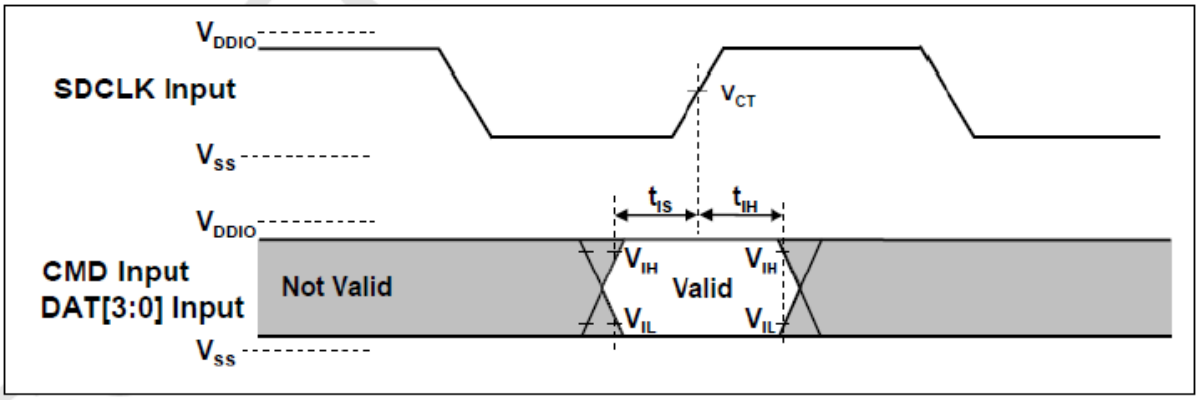


Table 7-12 Card Input Timing (SDR104 and SDR50 Modes)

Symbol	Min	Max	Unit	SDR104 Mode
t_{IS}	1.40	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5pF, V_{CT} = 0.975V
Symbol	**Min**	**Max**	**Unit**	**SDR50 Mode**
t_{IS}	3.00	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5pF, V_{CT} = 0.975V

Output (SDR12, SDR25, and SDR50 Modes)

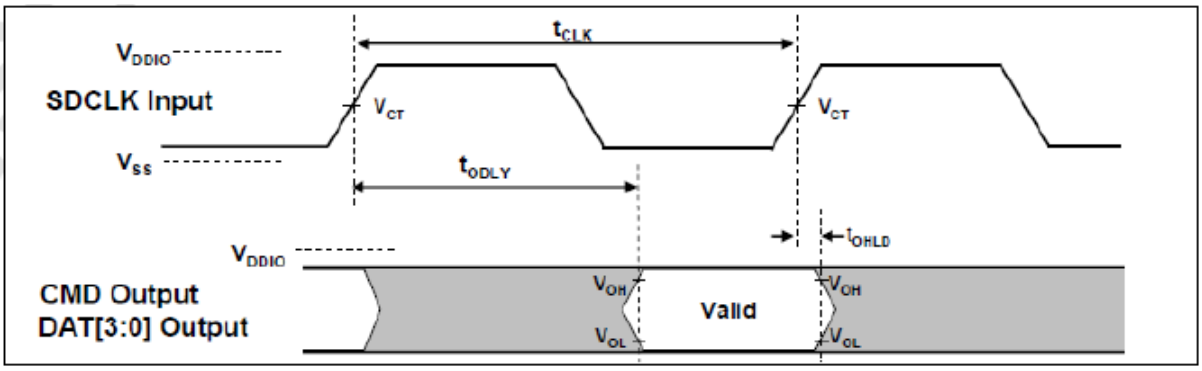


Table 7-13 Output Timing of Fixed Data Window (SDR12, SDR25, SDR50)

Symbol	Min	Max	Unit	Remark
t_{ODLY}	-	7.5	ns	t_{CLK} ≥10.0ns, C_L=30pF, using driver Type B, for SDR50.
t_{ODLY}	-	14	ns	t_{CLK} ≥20.0ns, C_L=40pF, using driver Type B, for SDR25 and SDR12
T_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.). C_L=15pF

Output (SDR104 Mode)

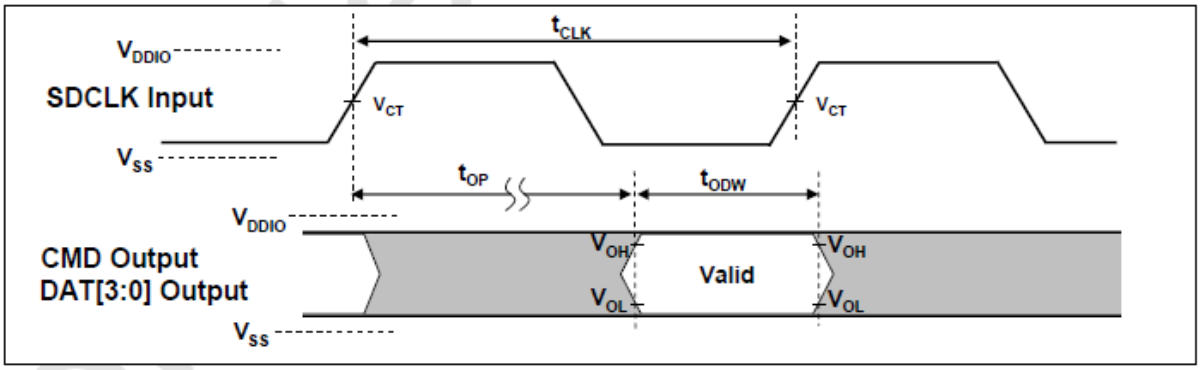


Table 7-14 Output Timing of Variable Window (SDR104)

Symbol	Min	Max	Unit	Remark
t_{OP}	0	2	UI	Card Output Phase
$\triangle t_{OP}$	-350	+1550	ps	Delay variable due to temperature change after tuning
t_{ODW}	0.60	-	UI	t_{ODW} = 2.88ns at 208MHz

7.5.4 SD Interface Timing (DDR50 Mode)

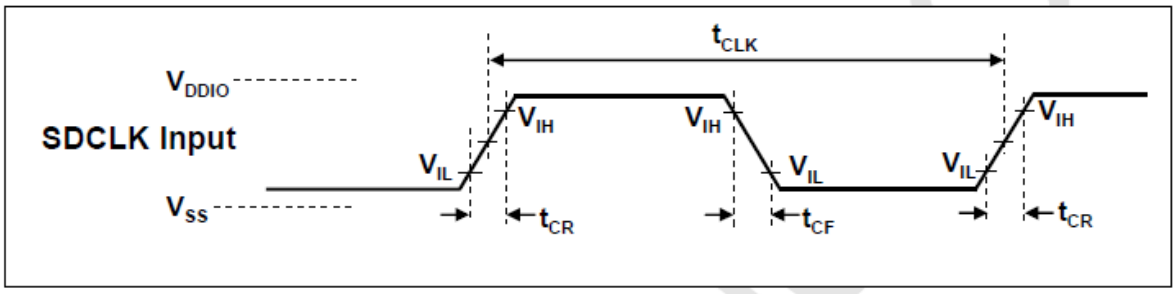
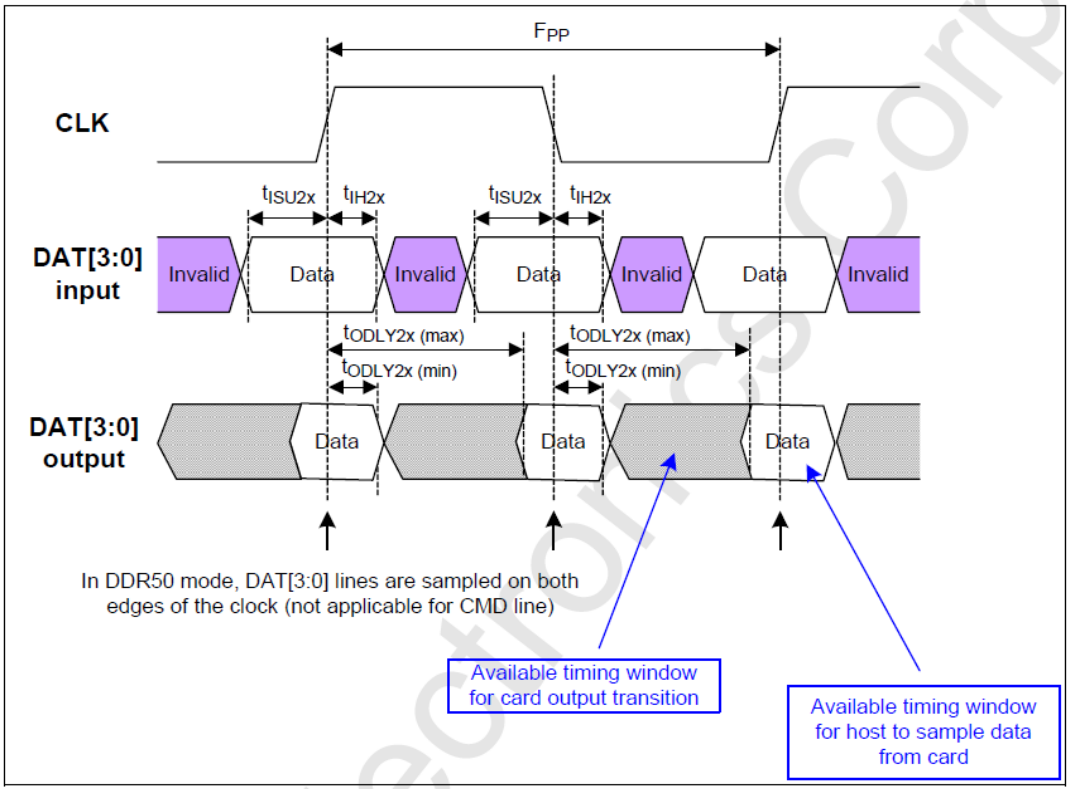


Table 7-15 Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	0.2*t_{CLK}	ns	t_{CR}, t_{CF} < 4.00ns (max.) at 50MHz, C_{CARD}=10pF
Clock Duty	45	55	%	



Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

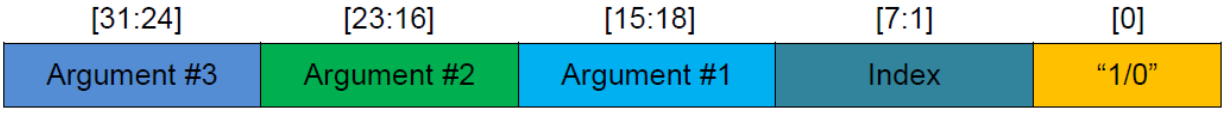
Table 7-16 Bus Timings – Parameters Values (DDR50 Mode)

Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input setup time	t_{ISU}	3	-	ns	$C_{card} \leq 10$ pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	$C_{card} \leq 10$ pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	13.7	ns	$C_L \leq 30$ pF (1 card)
Output Hold time	T_{OH}	1.5	-	ns	$C_L \geq 15$ pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input setup time	t_{ISU2x}	3	-	ns	$C_{card} \leq 10$ pF (1 card)
Input hold time	t_{IH2x}	0.8	-	ns	$C_{card} \leq 10$ pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7.0	ns	$C_L \leq 25$ pF (1 card)
Output Hold time	T_{OH2x}	1.5	-	ns	$C_L \geq 15$ pF (1 card)

8. S.M.A.R.T.

8.1 Direct Host Access to SMART Data via SD General Command (CMD56)

CMD 56 is structured as a 32-bit argument. The implementation of the general purpose functions will arrange the CMD56 argument into the following format:



- Bit [0]: Indicates Read Mode when bit is set to [1] or Write Mode when bit is cleared [0]. Depending on the function, either Read Mode or Write Mode can be used.
- Bit [7:1]: Indicates the index of the function to be executed:
  - Read Mode: Index = 0x10 Get SMART Command Information
  - Write Mode: Index = 0x08 Pre-Load SMART Command Information
- Bit [15:8]: Function argument #1 (1-byte)
- Bit [23:16]: Function argument #2 (1-byte)
- Bit [31:24]: Function argument #3 (1-byte)

8.2 Process for Retrieving SMART Data

Step 1:

Write Mode: [0x08] Pre-Load SMART Command Information

Sequence	Command	Argument	Expected Data
Pre-Load SMART Command Information	CMD56	[0] "0" (Write Mode) [1:7] "0001 000" (Index = 0x08) [8:511] All '0' (Reserved)	No expected data

Step 2:

Read Mode – [0x10] Get SMART Command Information

Sequence	Command	Argument	Expected Data
Get SMART Command Information	CMD56	[0] "1" (Read Mode) [1:7] "0010 000" (Index = 0x10) [8:31] All '0' (Reserved)	1 sector (512 bytes) of response data byte[0-8] Flash ID byte[9-10] IC Version byte[11-12] FW Version byte[13] Reserved byte[14] CE Number byte[15] Reserved byte[16-17] Bad Block Replace Maximum byte[18] Reserved byte[32-63] Bad Block count per Die byte[64-65] Good Block Rate(%) byte[66-79] Reserved byte[80-83] Total Erase Count byte[84-95] Reserved byte[96-97] Endurance (Remain Life) (%) byte[98-99] Average Erase Count – L* byte[100-101] Minimum Erase Count – L* byte[102-103] Maximum Erase Count – L* byte[104-105] Average Erase Count – H* byte[106-107] Minimum Erase Count – H* byte[108-109] Maximum Erase Count – H* byte[110-111] Reserved byte[112-115] Power Up Count byte[116-127] Reserved byte[128-129] Abnormal Power Off Count byte[130-159] Reserved byte[160-161] Total Refresh Count byte[176-183] Product "Marker" byte[184-215] Bad Block count per Die byte[216-511] Reserved

Notes:

- *Please refer to technical note for High/Low byte definition.
- Both steps are required to retrieve SMART data: Pre-Load SMART Command followed by Get SMART Command, and must be in accordance with the SD Association standard flowchart for CMD56 (see below).

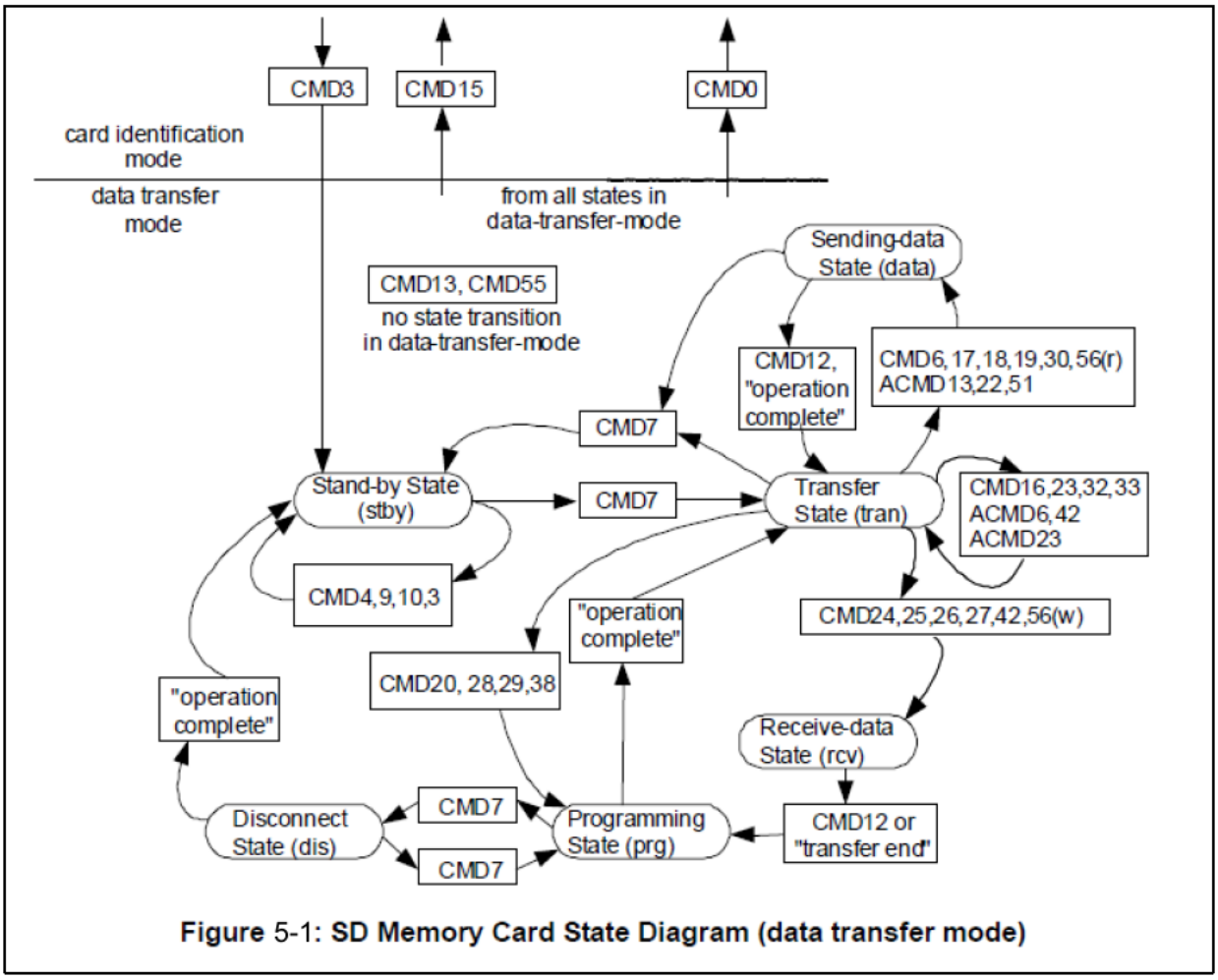


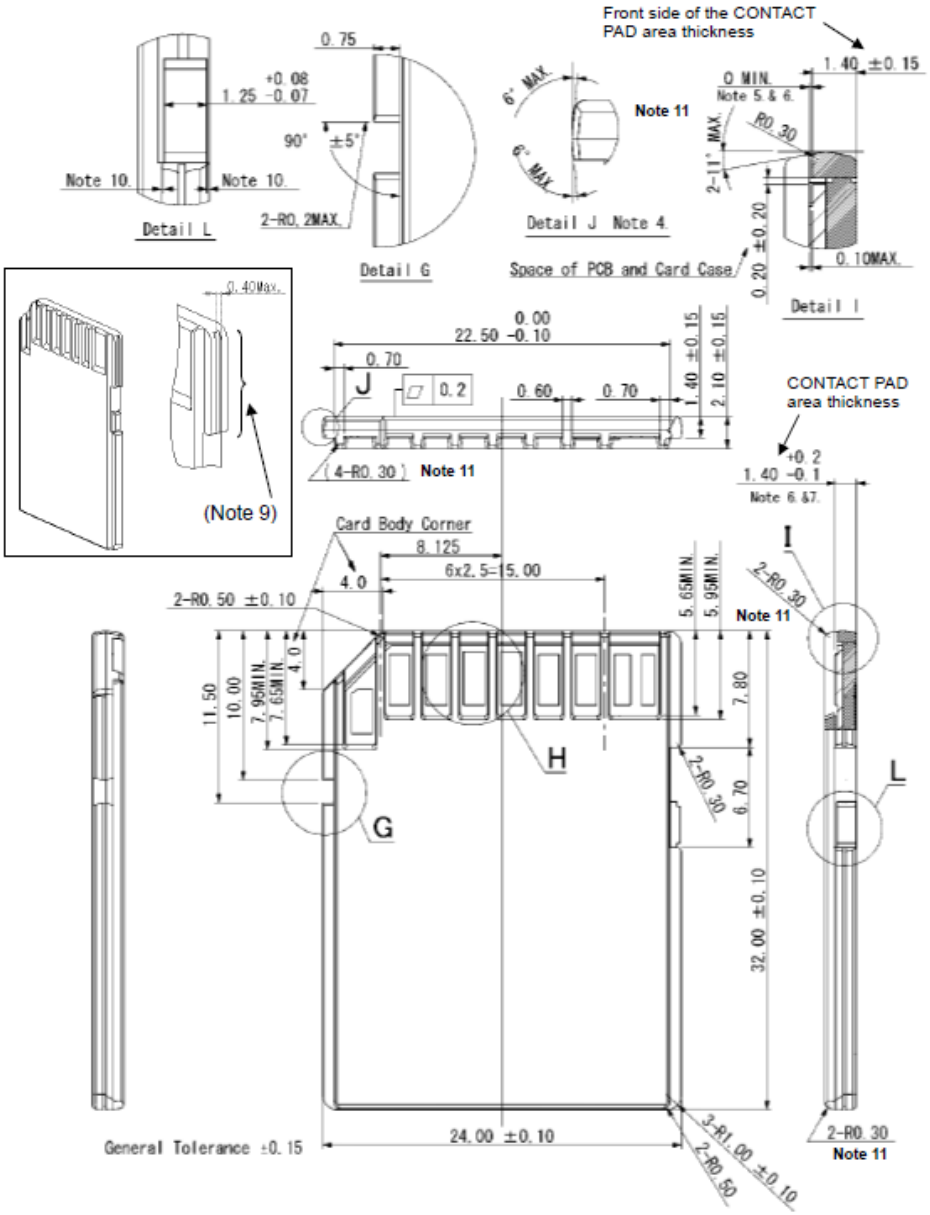
Figure 5-1: SD Memory Card State Diagram (data transfer mode)

Extracted from the SD Specifications Part 1 Physical Layer Simplified Specification Version 3.01.

9. Mechanical Dimensions

Table 9-1 Physical Information

Parameter	Unit	8 GB	16 GB	32 GB	64 GB	128GB
Length	mm	32.00 ± 0.10				
Width		24.00 ±0.10				
Height (Max.)		2.10 ± 0.15				



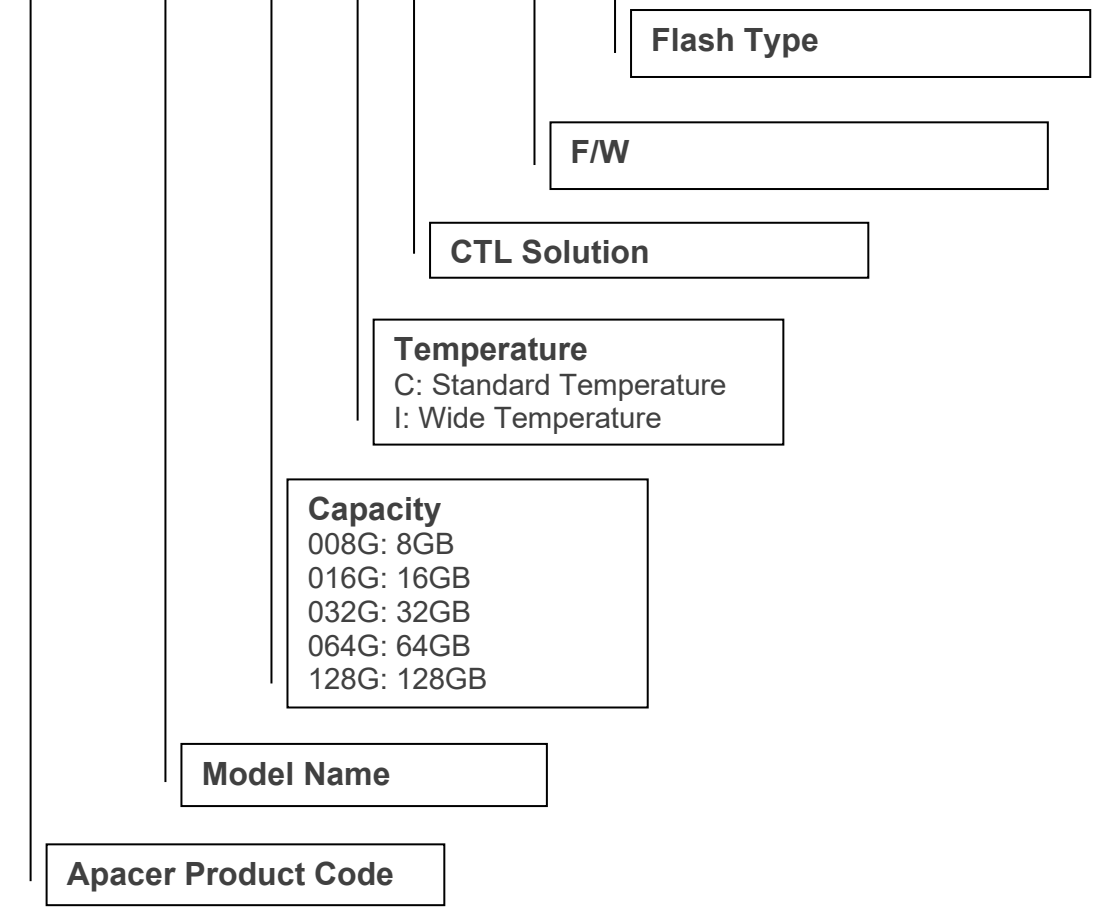
Note: For detailed mechanical specifications, please refer to *SD Specifications Part 1 Standard Size SD Card Mechanical Addendum*.

Figure 9-1 Mechanical Dimensions

10. Product Ordering Information

10.1 Product Code Designations

AP – ISD xxxG X A – 1X TM



10.2 Valid Combinations

The following table lists the available models of Apacer Industrial H1-M SD card series which are in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Capacity	Standard Temperature	Wide Temperature
8GB	AP-ISD008GCA-1HTM	AP-ISD008GIA-1HTM
16GB	AP-ISD016GCA-1HTM	AP-ISD016GIA-1HTM
32GB	AP-ISD032GCA-1HTM	AP-ISD032GIA-1HTM
64GB	AP-ISD064GCA-1FTM	AP-ISD064GIA-1FTM
128GB	AP-ISD128GCA-1FTM	AP-ISD128GIA-1FTM

Revision History

Revision	Description	Date
1.0	Official release	11/16/2015
1.1	Added CMD56 argument for SMART	12/16/2015
1.2	Added SMART section	12/23/2015
1.3	Added performance and power consumption for 4GB	2/2/2016
1.4	Revised performance and power consumption values	2/5/2016
1.5	Revised product ordering information for 4GB, 8GB, 16GB and 32GB due to FW update	3/15/2016
1.6	Revised capacity specifications	4/19/2016
1.7	- Revised performance for 4GB-32GB due to FW change (82.105) - Revised product ordering information for 4GB-32GB	7/29/2016
1.8	Added Power Failure Management to Features and General Description	10/27/2016
1.9	Modified the argument of Step 2: Read Mode – [0x10] Get SMART Command Information for S.M.A.R.T.	10/27/2016
2.0	- Changed Wear-leveling to Global Wear Leveling - Added Read Disturb Management to Flash Management on Features page	11/15/2017
2.1	- Renamed extended temperature to wide temperature - Added Endurance to Specifications Overview page and 2.7 Endurance - Renamed Power Failure Management to DataDefender at Flash Management on Specifications Overview page and 1.2.6 section and updated the technology description	12/20/2018
2.2	- Updated the first note at 2.7 Endurance - Renamed Read Disturb Management to SMART Read Refresh and updated its description at 1.2.5 section	5/20/2019
2.3	Updated power consumption for 32GB at 2.6 Power Consumption	11/26/2020
2.4	Removed 4GB support	10/1/2021
2.5	Replaced DataDefender with Power Failure Management support	11/5/2025

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