

## RoHS Recast Compliant Industrial Secure Digital Card H1 Product Specifications

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Version 1.4



**Apacer Technology Inc.**

1F, No.32, Zhongcheng Rd., Tucheng Dist., New Taipei City, Taiwan, R.O.C

Tel: +886-2-2267-8000 Fax: +886-2-2267-2261

[www.apacer.com](http://www.apacer.com)

## Specifications Overview:

- **Fully Compatible with SD Card Specifications 3.0, 2.0 and 1.1**
  - SD Memory Card Specifications, Part 1, Physical Layer Specification, Ver 3.00
  - SD Memory Card Specifications, Part 2, File System Specification, Ver 3.00
  - SD Memory Card Specifications, Part 3, Security Specification, Ver 3.00
- **Capacity**
  - 256, 512 MB
  - 1, 2 GB
- **Performance\***
  - Sequential read: Up to 23 MB/sec
  - Sequential write: Up to 19 MB/sec
- **Flash Management**
  - Built-in advanced ECC algorithm
  - Global Wear Leveling
  - Flash bad-block management
  - S.M.A.R.T.
  - Power Management
  - Power Failure Management
  - SMART Read Refresh™
- **NAND Flash Type: SLC**
- **Temperature Range**
  - Operating: -40°C to 85°C
  - Storage: -40°C to 85°C
- **Operating Voltage: 2.7V ~ 3.6V**
- **Power Consumption\***
  - Operating: 80 mA
  - Standby: 190 μA
- **SD-Protocol Compatible**
- **Supports SD SPI Mode**
- **Physical Dimensions:**  
32mm (L) x 24mm (W) x 2.1mm (H)
- **RoHS Recast Compliant (2011/65/EU)**

\*Varies from capacities. Performance values presented here are typical and may vary depending on settings and platforms.

## Table of Contents

<b>1. General Descriptions .....</b>	<b>3</b>
1.1. Product Functional Block .....	3
1.2 Flash Management .....	4
1.2.1 Bad Block Management.....	4
1.2.2 Powerful ECC Algorithms .....	4
1.2.3 Global Wear Leveling .....	4
1.2.4 S.M.A.R.T. ....	4
1.2.5 Power Management.....	4
1.2.6 SMART Read Refresh™.....	4
1.2.7 Power Failure Management.....	5
<b>2. Electrical Characteristics .....</b>	<b>6</b>
2.1 Card Architecture .....	6
2.2 Pin Assignment .....	6
2.3 Capacity Specifications .....	7
2.4 Performance Specifications .....	7
2.5 DC Power Supply.....	7
2.6 Power Consumption.....	7
<b>3. Physical Characteristics.....</b>	<b>8</b>
3.1 Physical Dimensions.....	8
3.2 Durability Specifications.....	9
<b>4. AC Characteristics .....</b>	<b>10</b>
4.1 SD Interface Timing (Default) .....	10
4.2 SD Interface Timing (High Speed Mode).....	11
4.3 SD Interface Timing (SDR12, SDR25, SDR50 and SDR104 Modes) Input.....	13
4.3.1 Clock Timing .....	13
4.3.2 Card Input Timing .....	13
4.3.3 Card Output Timing of Fixed Data Window (SDR12, SDR25 and SDR50) .....	14
4.3.4 Output Timing of Variable Window (SDR104) .....	14
4.3.5 SD Interface Timing (DDR50 Mode).....	15
4.3.6 Bus Timings – Parameters Values (DDR50 Mode).....	16
<b>5. Product Ordering Information.....</b>	<b>17</b>
5.1 Product Code Designations .....	17
5.2 Valid Combinations .....	18

# 1. General Descriptions

As the demand of reliable and high-performance data storage in a small form factor increases, Apacer's SD card is designed specifically for rigorous applications by offering maximum endurance, reliability, and agility, where extreme traceability, enhanced data integrity, and exceptionally velocity are required.

Regarding compatibility, this industrial SD card is compatible with SD Memory Card Specifications, Physical Layer specification, File System Specification and Part 3 Security Specification. Furthermore, the SD card is compatible with SD protocol. With built in ECC, wear-leveling and bad block management, this industrial SD card serves as an ideal portable storage solution.

## 1.1. Product Functional Block

The SD contains a flash controller and flash media with SD standard interface.

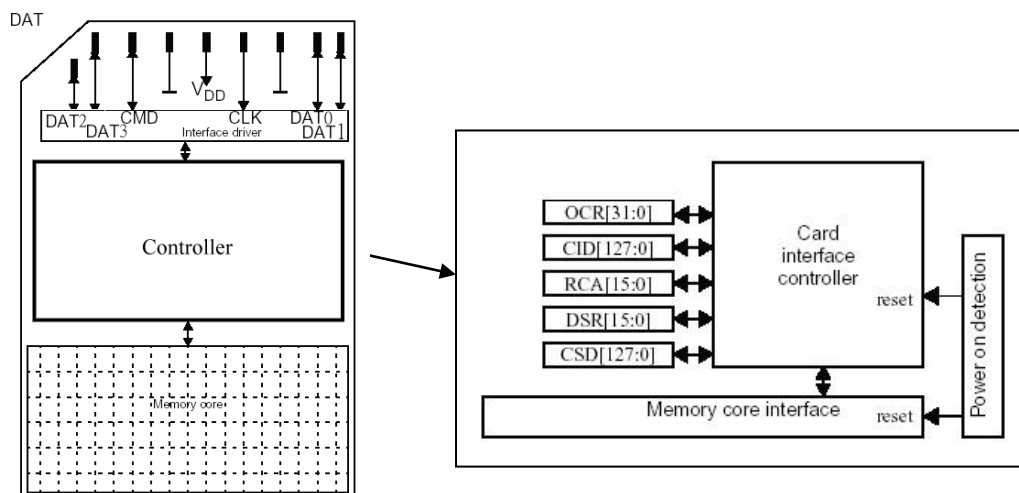


Figure 2-1 Block Diagram

## 1.2 Flash Management

### 1.2.1 Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. Apacer implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

### 1.2.2 Powerful ECC Algorithms

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, the SD card applies the BCH ECC Algorithm, which can detect and correct errors occur during read process, ensure data been read correctly, as well as protect data from corruption. The SD controller can detect and correct up to 43 bits error in 1K bytes.

### 1.2.3 Global Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some area get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Global Wear Leveling technique is applied to extend the lifespan of NAND Flash by evenly distributing writes and erase cycles across the media.

Apacer provides Global Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing Global Wear Leveling algorithm, the life expectancy of the NAND Flash is greatly improved.

### 1.2.4 S.M.A.R.T.

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is a special function that allows a memory device to automatically monitor its health. Apacer provides a program named SmartInfo Tool to observe Apacer’s SD and MicroSD cards. Note that this tool can only support Apacer’s industrial SD and MicroSD cards. This tool will display firmware version, endurance life ratio, good block ratio, and so forth.

### 1.2.5 Power Management

A power saving feature of the SD is automatic entrance and exit from sleep mode. Upon completion of an operation, the SD will enter the sleep mode to conserve power if no further commands are received within X seconds, where X is programmable by software. The master does not have to take any action for this to occur. The SD is in sleep mode except when the host is accessing it, thus conserving power.

Any command issued by the master to the SD will cause it to exit sleep mode and response to the master.

### 1.2.6 SMART Read Refresh™

Apacer’s SMART Read Refresh plays a proactive role in avoiding read disturb errors from occurring to ensure health status of all blocks of NAND flash. Developed for read-intensive applications in particular, SMART Read Refresh is employed to make sure that during read operations, when the read operation threshold is reached, the data is refreshed by re-writing it to a different block for subsequent use.

## 1.2.7 Power Failure Management

Apacer industrial SD and MicroSD cards provide complete data protection mechanism during every abnormal power shutdown situation, such as power failure at programming data, updating system tables, erasing blocks, etc. Apacer Power-Loss Protection mechanism includes:

- Maintaining data correctness and increasing the reliability of the data stored in the NAND Flash memory.
- Protecting F/W table and the data written to flash from data loss in the event of power off.

## 2. Electrical Characteristics

### 2.1 Card Architecture

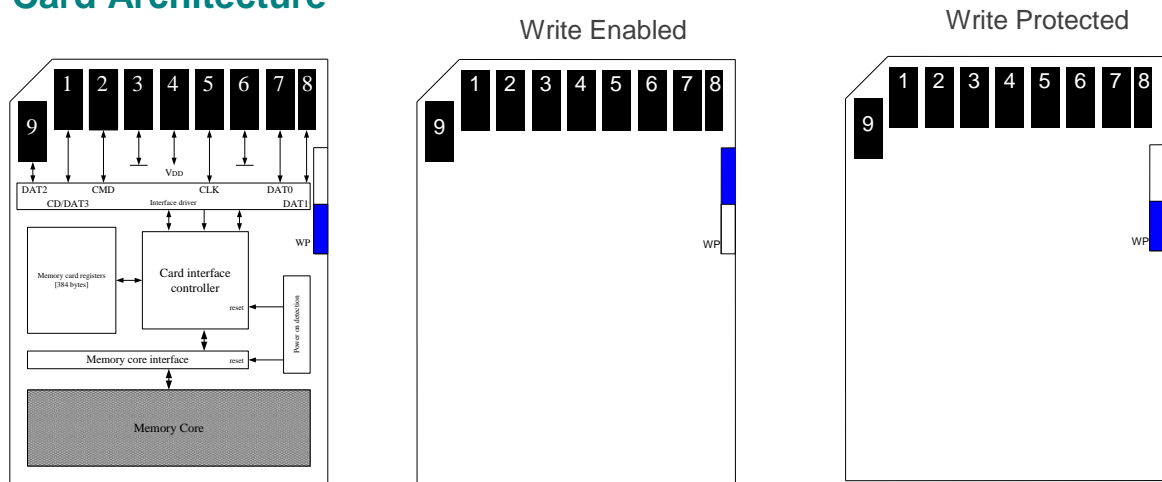


Figure 2-1 Card Architecture

### 2.2 Pin Assignment

Table 2-1 Pin Descriptions

Pin	SD Mode		SPI Mode	
	Name	Description	Name	Description
1	CD/DAT3	Card detect/Data line[Bit 3]	CS	Chip select
2	CMD	Command/Response	DI	Data in
3	VSS1	Supply voltage ground	VSS	Supply voltage ground
4	VDD	Supply voltage	VDD	Supply voltage
5	CLK	Clock	SCLK	Clock
6	VSS2	Supply voltage ground	VSS2	Supply voltage ground
7	DAT0	Data line[Bit 0]	DO	Data out
8	DAT1	Data line[Bit 1]	Reserved	
9	DAT2	Data line[Bit 2]	Reserved	

## 2.3 Capacity Specifications

The following table shows the specific capacity for the SD card.

**Table 2-2** Capacity Specifications

Capacity	Total bytes*
256 MB	248,643,584
512 MB	497,287,168
1 GB	996,868,096
2 GB	1,981,480,960

Note: The statistics may vary depending on file systems of various OS. User data bytes do not indicate total useable bytes. LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

## 2.4 Performance Specifications

Performances of the SD card are shown in the table below.

**Table 2-3** Performance Specifications

Capacity	256 MB	512 MB	1 GB	2 GB
<b>Sequential Read (MB/s)</b>	21	22	23	23
<b>Sequential Write (MB/s)</b>	8	16	19	19

Note:

Results may differ from various flash configurations or host system setting.

\*Sequential performance is based on CrystalDiskMark 5.2.1 with file size 1,000MB.

## 2.5 DC Power Supply

**Table 2-4** Operating Voltage

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Power Supply Voltage	2.7	3.3	3.6	V

## 2.6 Power Consumption

**Table 2-5** Power Consumption

Capacity	256 MB	512 MB	1 GB	2 GB
<b>Operating (mA)</b>	55	60	70	80
<b>Standby (µA)</b>	165	170	170	190

Note:

\*All values are typical and may vary depending on flash configurations or host system settings.

\*\*Active power is an average power measurement performed using CrystalDiskMark with 128KB sequential read/write transfers.



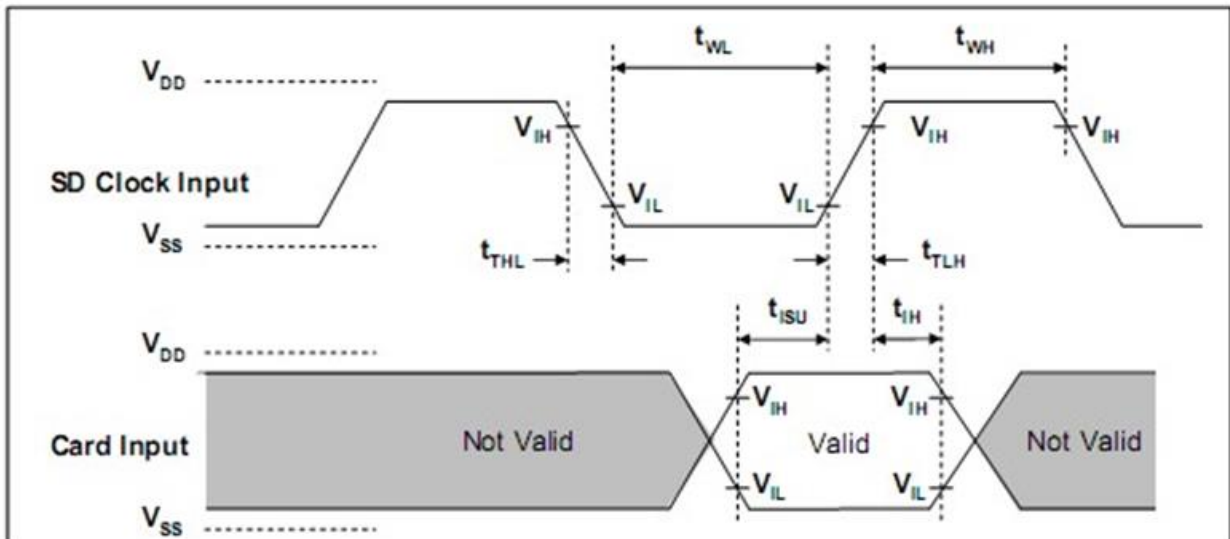
### 3.2 Durability Specifications

**Table 3-1** Durability Specifications

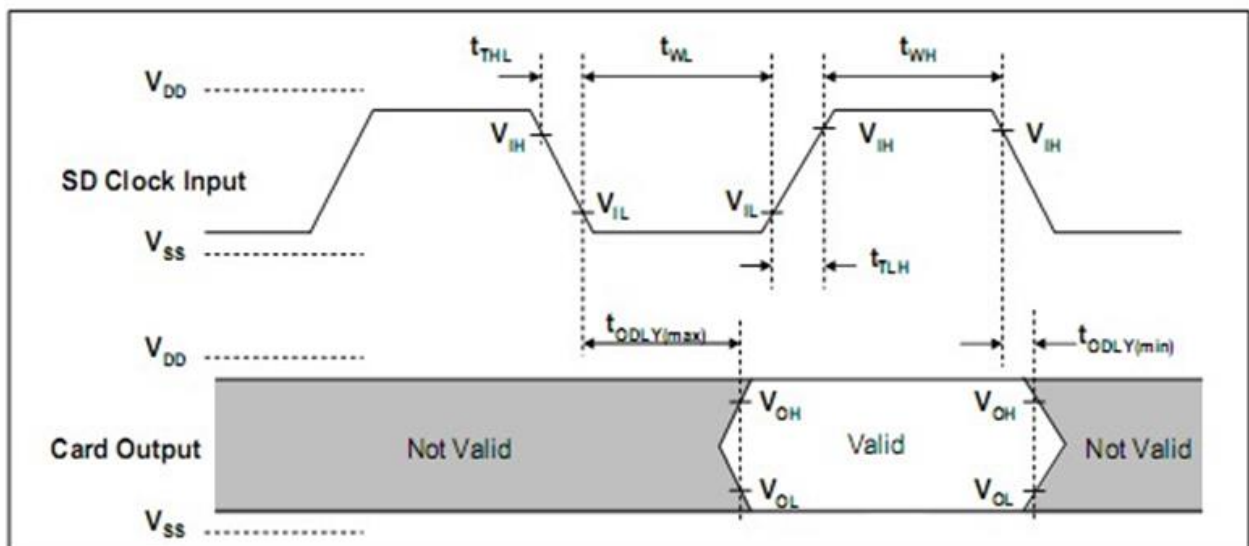
Item	Specifications
Temperature	-40°C to 85°C (Operating)
	-40°C to 85°C (Storage)
Shock	1,500G, 0.5ms
Vibration	20Hz~80Hz/1.52mm (frequency/displacement) 80Hz~2000Hz/20G (frequency/displacement) X, Y, Z axis/60mins each
Drop	1.5m free fall, 6 surfaces of each
Bending	≥ 10N, hold 1min/5times
Torque	0.15N-m or 2.5deg, hold 30 seconds/ 5 times
Salt spray	Concentration: 3% NaCl at 35°C (storage for 24 hours)
Waterproof	JIS IPX7 compliance, Water temperature 25°C Water depth: the lowest point of unit is locating 1000mm below surface (storage for 30 mins)
X-Ray Exposure	0.1 Gy of medium-energy radiation (70 KeV to 140 KeV, cumulative dose per year) to both sides of the card ;storage for 30 mins)
Switch Cycle	0.4~0.5N, 1000 times
Durability	10,000 times mating cycle
ESD	Contact: +/-4KV each item 25 times Air: +/-8KV 10 times

## 4. AC Characteristics

### 4.1 SD Interface Timing (Default)



Card input Timing (Default Speed Card)

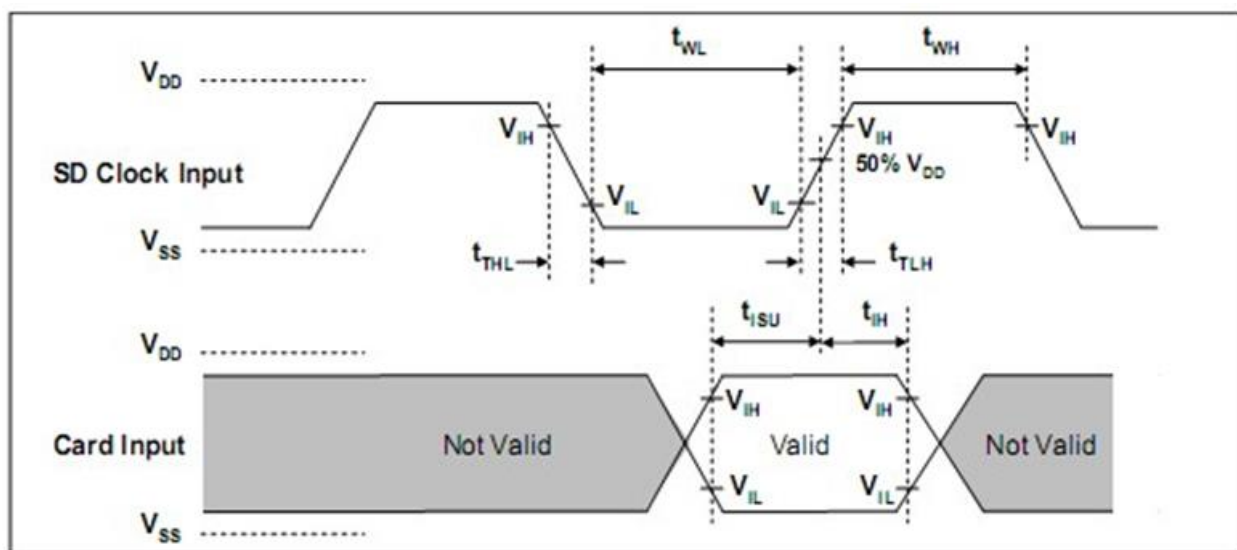


Card Output Timing (Default Speed Mode)

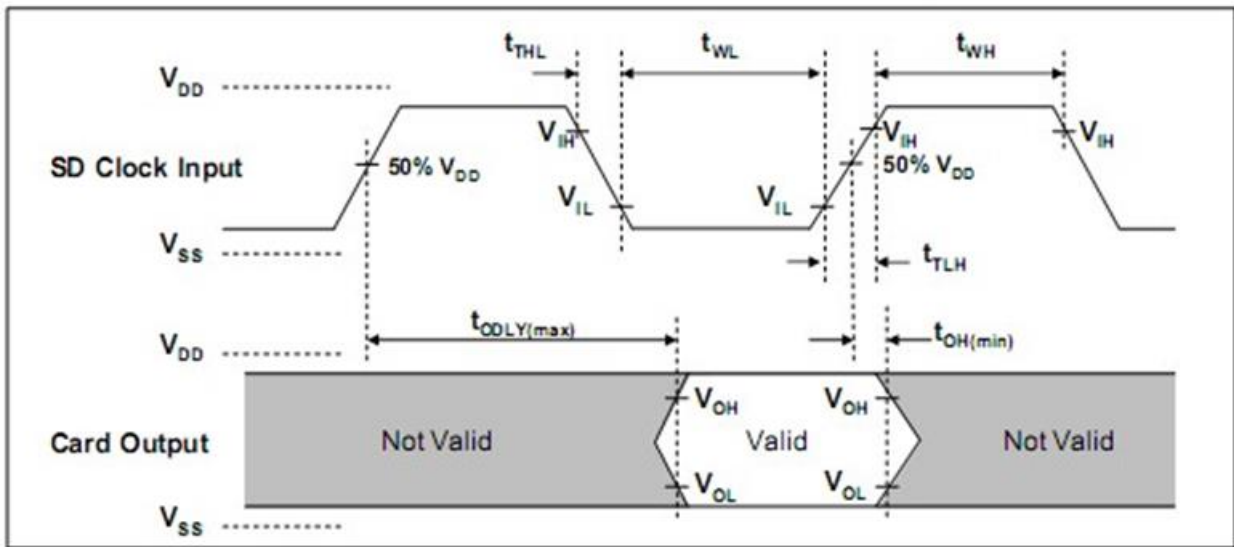
SYMBOL	PARAMETER	MIN	MAX	UNIT	REMARK
<b>Clock CLK (All values are referred to min(V<sub>IH</sub>) and max(V<sub>IL</sub>))</b>					
f <sub>PP</sub>	Clock frequency data transfer	0	25	MHz	C <sub>card</sub> ≤ 10 pF (1 card)
f <sub>OD</sub>	Clock frequency identification	0 <sup>(1)</sup> /100	400	KHz	C <sub>card</sub> ≤ 10 pF (1 card)
t <sub>WL</sub>	Clock low time	10	-	ns	C <sub>card</sub> ≤ 10 pF (1 card)
t <sub>WH</sub>	Clock high time	10	-	ns	C <sub>card</sub> ≤ 10 pF (1 card)
t <sub>TLH</sub>	Clock rise time	-	10	ns	C <sub>card</sub> ≤ 10 pF (1 card)
t <sub>THL</sub>	Clock fall time	-	10	ns	C <sub>card</sub> ≤ 10 pF (1 card)
<b>Inputs CMD, DAT (Referenced to CLK)</b>					
t <sub>ISU</sub>	Input setup time	5	-	ns	C <sub>card</sub> ≤ 10 pF (1 card)
t <sub>IH</sub>	Input hold time	5	-	ns	C <sub>card</sub> ≤ 10 pF (1 card)
<b>Outputs CMD, DAT (Referenced to CLK)</b>					
t <sub>ODLY</sub>	Output delay time during data transfer mode	0	14	ns	C <sub>L</sub> ≤ 40 pF (1 card)
t <sub>OH</sub>	Output hold time	0	50	ns	C <sub>L</sub> ≤ 40 pF (1 card)

(1)0Hz means to stop the clock. The given minimum frequency range is for cases that require the clock to be continued.

## 4.2 SD Interface Timing (High Speed Mode)



Card Input Timing (High Speed Card)



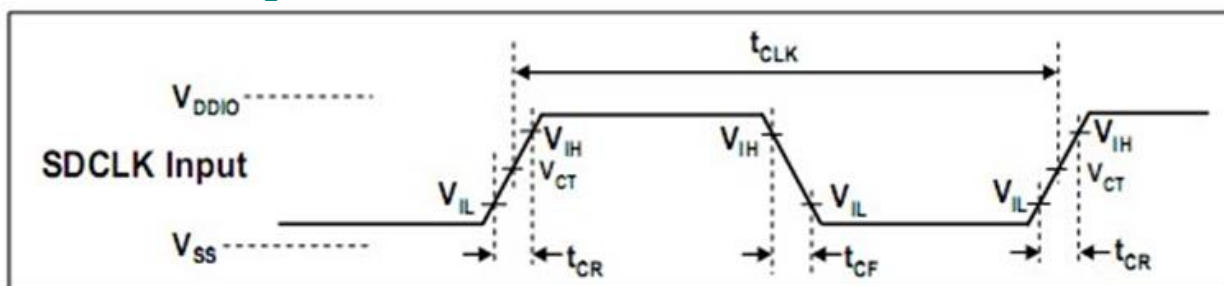
**Card Output Timing (High Speed Mode)**

SYMBOL	PARAMETER	MIN	MAX	UNIT	REMARK
<b>Clock CLK (All values are referred to min(<math>V_{IH}</math>) and max(<math>V_{IL}</math>))</b>					
$f_{PP}$	Clock frequency data transfer	0	50	MHz	$C_{card} \leq 10 \text{ pF}$ (1 card)
$t_{WL}$	Clock low time	7	-	ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
$t_{WH}$	Clock high time	7	-	ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
$t_{TLH}$	Clock rise time	-	3	ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
$t_{THL}$	Clock fall time	-	3	ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
<b>Inputs CMD, DAT (Referenced to CLK)</b>					
$t_{ISU}$	Input setup time	6	-	ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
$t_{IH}$	Input hold time	2	-	ns	$C_{card} \leq 10 \text{ pF}$ (1 card)
<b>Outputs CMD, DAT (Referenced to CLK)</b>					
$t_{ODLY}$	Output delay time during data transfer made	-	14	ns	$CL \leq 40 \text{ pF}$ (1 card)
$t_{OH}$	Output hold time	2.5	-	ns	$CL \geq 15 \text{ pF}$ (1 card)
CL	Total system capacitance for each line*	-	40	pF	1 card

\*In order to satisfy severe timing, host shall run on only one card

### 4.3 SD Interface Timing (SDR12, SDR25, SDR50 and SDR104 Modes) Input

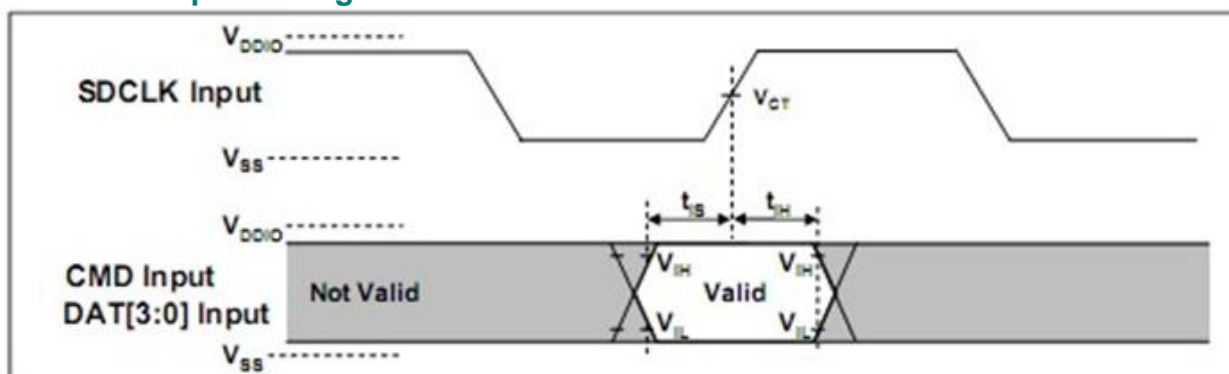
#### 4.3.1 Clock Timing



**Clock Signal Timing**

SYMBOL	MIN	MAX	UNIT	REMARK
$t_{CLK}$	4.8	-	ns	208MHz (Max.), Between rising edge, $V_{CT} = 0.975V$
$t_{CR}, t_{CF}$	-	$0.2 * t_{CLK}$	ns	$t_{CR}, t_{CF} < 2.00ns$ (max.) at 208MHz, $C_{CARD}=10pF$ $t_{CR}, t_{CF} < 2.00ns$ (max.) at 100MHz, $C_{CARD}=10pF$ The absolute maximum value of $t_{CR}, t_{CF}$ is 10ns regardless of clock frequency.
Clock Duty	30	70	%	

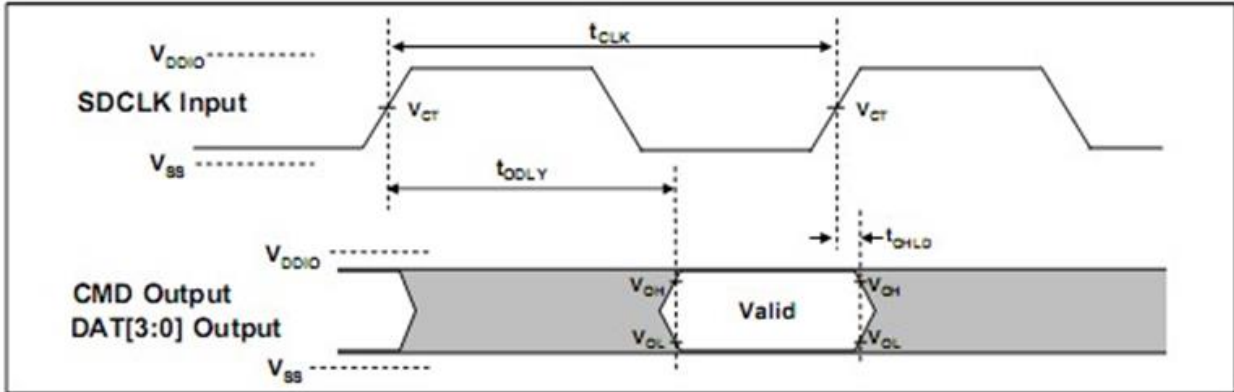
#### 4.3.2 Card Input Timing



**Card Input Timing**

SYMBOL	MIN	MAX	UNIT	SDR104 MODE
$t_{IS}$	1.40	-	ns	$C_{CARD} = 10pF, V_{CT} = 0.975V$
$t_{IH}$	0.80	-	ns	$C_{CARD} = 5pF, V_{CT} = 0.975V$
SYMBOL	MIN	MAX	UNIT	SDR12, SDR25 and SDR50 MODES
$t_{IS}$	3.00	-	ns	$C_{CARD} = 10pF, V_{CT} = 0.975V$
$t_{IH}$	0.80	-	ns	$C_{CARD} = 5pF, V_{CT} = 0.975V$

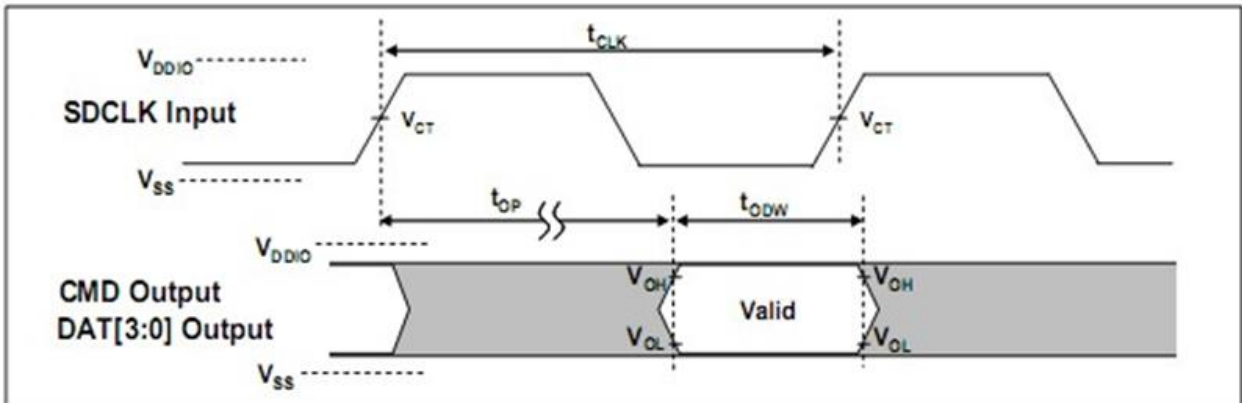
### 4.3.3 Card Output Timing of Fixed Data Window (SDR12, SDR25 and SDR50)



Output Timing of Fixed Date Window<sup>+</sup>

SYMBOL	MIN	MAX	UNIT	REMARK
$t_{ODLY}$	-	7.5	ns	$t_{CLK} \geq 10.0ns$ , $CL=30pF$ , using driver Type B, for SDR50.
$t_{ODLY}$		14	ns	$t_{CLK} \geq 20.0ns$ , $CL=40pF$ , using driver Type B, for SDR25 and SDR12.
$t_{OH}$	1.5	-	ns	Hold time at the $t_{ODLY}$ (min.). $CL=15pF$

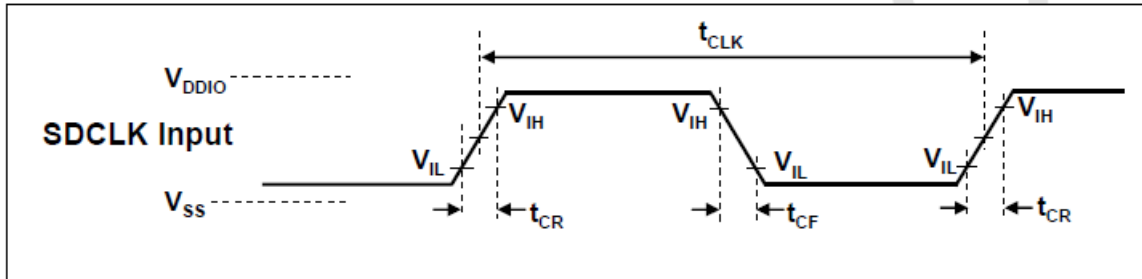
### 4.3.4 Output Timing of Variable Window (SDR104)



Output Timing of Variable Data Window<sup>+</sup>

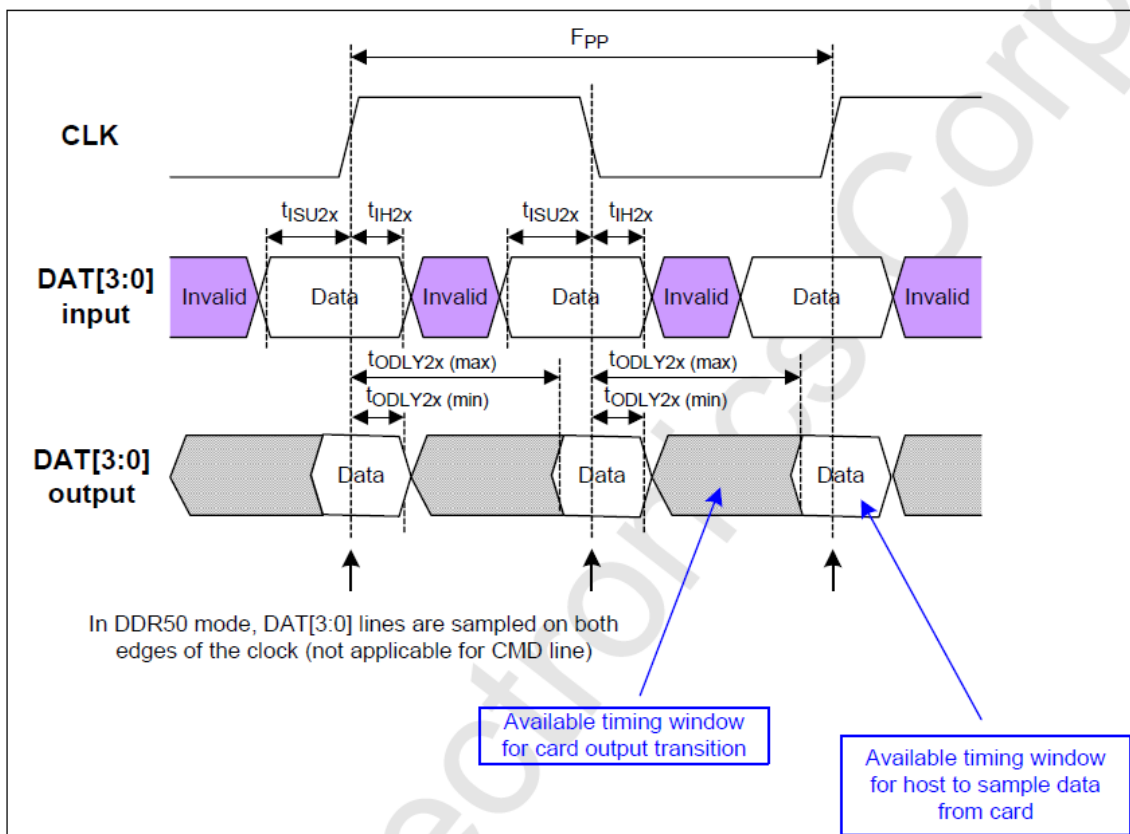
SYMBOL	MIN	MAX	UNIT	REMARK
$t_{OP}$	-	2	UI	Card Output Phase
$\Delta t_{OP}$	-350	+1550	ps	Delay variation due to temperature change after tuning
$t_{ODW}$	0.60	-	UI	$t_{ODW} = 2.88ns$ at 208MHz

### 4.3.5 SD Interface Timing (DDR50 Mode)



**Clock Signal Timing**

SYMBOL	MIN	MAX	UNIT	REMARK
$t_{CLK}$	20	-	ns	50MHz (Max.), Between rising edge
$t_{CR}, t_{CF}$	-	$0.2 * t_{CLK}$	ns	$t_{CR}, t_{CF} < 4.00ns$ (max.) at 50MHz, CCARD=10pF
Clock Duty	45	55	%	



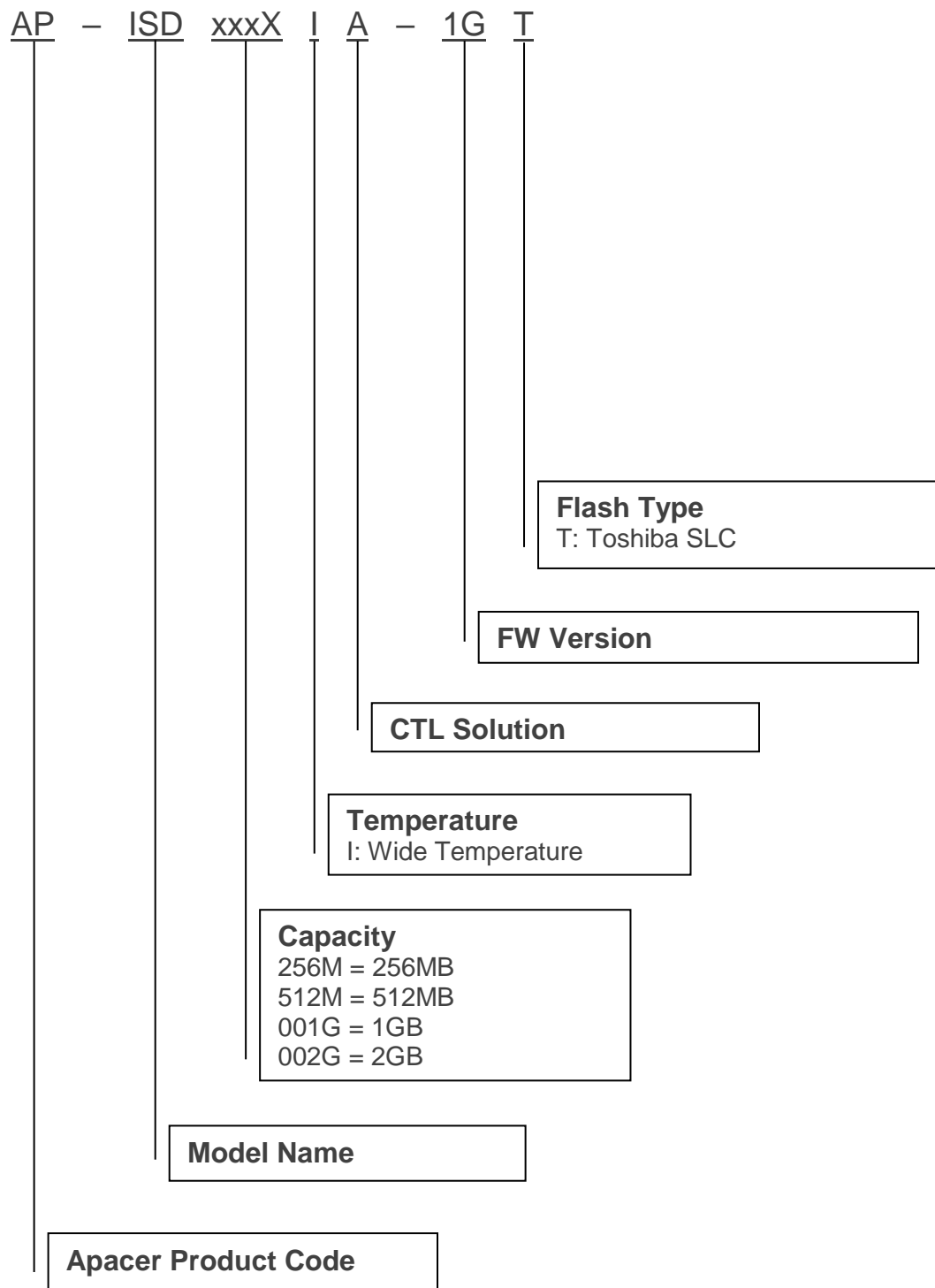
**Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode**

### 4.3.6 Bus Timings – Parameters Values (DDR50 Mode)

Symbol	Parameters	Min	Max	Unit	Remark
<b>Input CMD</b> (referenced to CLK rising edge)					
t <sub>ISU</sub>	Input set-up time	6	-	ns	C <sub>card</sub> ≤ 10 pF (1 card)
t <sub>IH</sub>	Input hold time	0.8	-	ns	C <sub>card</sub> ≤ 10 pF (1 card)
<b>Output CMD</b> (referenced to CLK rising edge)					
t <sub>ODLY</sub>	Output Delay time during Data Transfer Mode	-	13.7	ns	C <sub>L</sub> ≤ 30 pF (1 card)
T <sub>OH</sub>	Output Hold time	1.5	-	ns	C <sub>L</sub> ≥ 15 pF (1 card)
<b>Inputs DAT</b> (referenced to CLK rising and falling edges)					
t <sub>ISU2x</sub>	Input set-up time	3	-	ns	C <sub>card</sub> ≤ 10 pF (1 card)
t <sub>IH2x</sub>	Input hold time	0.8	-	ns	C <sub>card</sub> ≤ 10 pF (1 card)
<b>Outputs DAT</b> (referenced to CLK rising and falling edges)					
t <sub>ODLY2x</sub>	Output Delay time during Data Transfer Mode	-	7.0	ns	C <sub>L</sub> ≤ 25 pF (1 card)
T <sub>OH2x</sub>	Output Hold time	1.5	-	ns	C <sub>L</sub> ≥ 15 pF (1 card)

## 5. Product Ordering Information

### 5.1 Product Code Designations



## 5.2 Valid Combinations

Capacity	Part Number
256MB	AP-ISD256MIA-1GT
512MB	AP-ISD512MIA-1GT
1GB	AP-ISD001GIA-1GT
2GB	AP-ISD002GIA-1GT

**Note:** Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

## Revision History

Revision	Date	Description	Remark
1.0	4/28/2016	Official release	
1.1	5/3/2016	Revised durability specifications	
1.2	5/4/2016	Revised product ordering information	
1.3	10/3/2016	Added Power Failure Management to Features and General Description	
1.4	10/16/2020	Renamed extended temperature and Auto Read Refresh to wide temperature and SMART Read Refresh	

## Global Presence

### Taiwan (Headquarters)

#### Apacer Technology Inc.

1F., No.32, Zhongcheng Rd., Tucheng Dist.,  
New Taipei City 236, Taiwan R.O.C.

Tel: 886-2-2267-8000

Fax: 886-2-2267-2261

[amtsales@apacer.com](mailto:amtsales@apacer.com)

### U.S.A.

#### Apacer Memory America, Inc.

46732 Lakeview Blvd., Fremont, CA 94538

Tel: 1-408-518-8699

Fax: 1-510-249-9551

[sa@apacerus.com](mailto:sa@apacerus.com)

### Japan

#### Apacer Technology Corp.

6F, Daiyontamachi Bldg., 2-17-12, Shibaura, Minato-Ku,  
Tokyo, 108-0023, Japan

Tel: 81-3-5419-2668

Fax: 81-3-5419-0018

[jpservices@apacer.com](mailto:jpservices@apacer.com)

### Europe

#### Apacer Technology B.V.

Science Park Eindhoven 5051 5692 EB Son,  
The Netherlands

Tel: 31-40-267-0000

Fax: 31-40-290-0686

[sales@apacer.nl](mailto:sales@apacer.nl)

### China

#### Apacer Electronic (Shanghai) Co., Ltd

Room D, 22/FL, No.2, Lane 600, JieyunPlaza,  
Tianshan RD, Shanghai, 200051, China

Tel: 86-21-6228-9939

Fax: 86-21-6228-9936

[sales@apacer.com.cn](mailto:sales@apacer.com.cn)

### India

#### Apacer Technologies Pvt Ltd,

1874, South End C Cross, 9<sup>th</sup> Block Jayanagar,  
Bangalore-560069, India

Tel: 91-80-4152-9061/62

Fax: 91-80-4170-0215

[sales\\_india@apacer.com](mailto:sales_india@apacer.com)