Apacer

Halogen-free & RoHS Recast Compliant

CompactFlash Series 6A-M

Industrial CF Product Specifications

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Version 1.8

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Apacer

Specifications Overview:

- **CompactFlash Association Specification Revision 6.0 Standard Interface**
  - ATA command set compatible
  - ATA transfer mode supports: PIO Mode 6 , Multiword DMA Mode 4 , Ultra DMA Mode 7 , PCMCIA UDMA Mode 7
- **Capacity**
  - 8, 16, 32, 64 GB
- **Performance**[1]
  - Sequential read: Up to 115 MB/sec
  - Sequential write: Up to 75 MB/sec
  - Random read 4K: up to 3,500 IOPS
  - Random write 4K: up to 231 IOPS
- **Flash Management**
  - Global Wear Leveling
  - Built-in hardware ECC
  - Supports S.M.A.R.T commands
  - Flash bad-block management
  - Power Failure Management
- **NAND Flash Type:** MLC
- **MTBF:** >1,000,000 hours
- **Endurance (in Terabytes Written: TBW)**
  - 8 GB: 22 TBW
  - 16 GB: 42 TBW
  - 32 GB: 87 TBW
  - 64 GB: 182 TBW
- **Temperature Range**
  - Operating:
    Standard: 0°C to 70°C
    Wide: -40°C to 85°C
  - Storage: -40°C to 100°C
- **Operating Voltage for Read and Write**
  - 3.3V
  - 5.0V
- **Power Consumption**[1]

  Operating Voltage: 3.3V
  - Active mode (Max.): 255 mA
  - Standby mode: 10 mA

  Operating Voltage: 5.0V
  - Active mode (Max.): 260 mA
  - Standby mode: 10 mA
- **Connector Type**
  - 50 pins female
- **Physical Dimensions**
  - 36.4mm x 42.8mm x 3.3mm
- **Write Protect by Hardware Switch**
- **Halogen Free**
- **RoHS Recast Compliant (Complies with 2011/65/EU Standard)**

Note:
1. Varies from capacities. The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings.

Table of Contents

1. General Description

Apacer's value-added Industrial CompactFlash Card offers high performance, high reliability and power-efficient storage. Regarding standard compliance, this CompactFlash Card complies with CompactFlash specification revision 6.0, supporting transfer modes up to Programmed Input Output (PIO) Mode 6, Multi-word Direct Memory Access (DMA) Mode 4, Ultra DMA Mode 7, and PCMCIA Ultra DMA Mode 7.

Apacer's value-added CFC provides complete PCMCIA – ATA functionality and compatibility. Apacer 's CompactFlash technology is designed for applications in Point of Sale (POS) terminals, telecom, IP-STB, medical instruments, surveillance systems, industrial PCs and handheld applications such as the new generation of Digital Single Lens Reflex (DSLR) cameras.

2. Functional Block

The CompactFlash Card (CFC) includes a controller and flash media, as well as the CompactFlash standard interface. Figure 2-1 shows the functional block diagram.

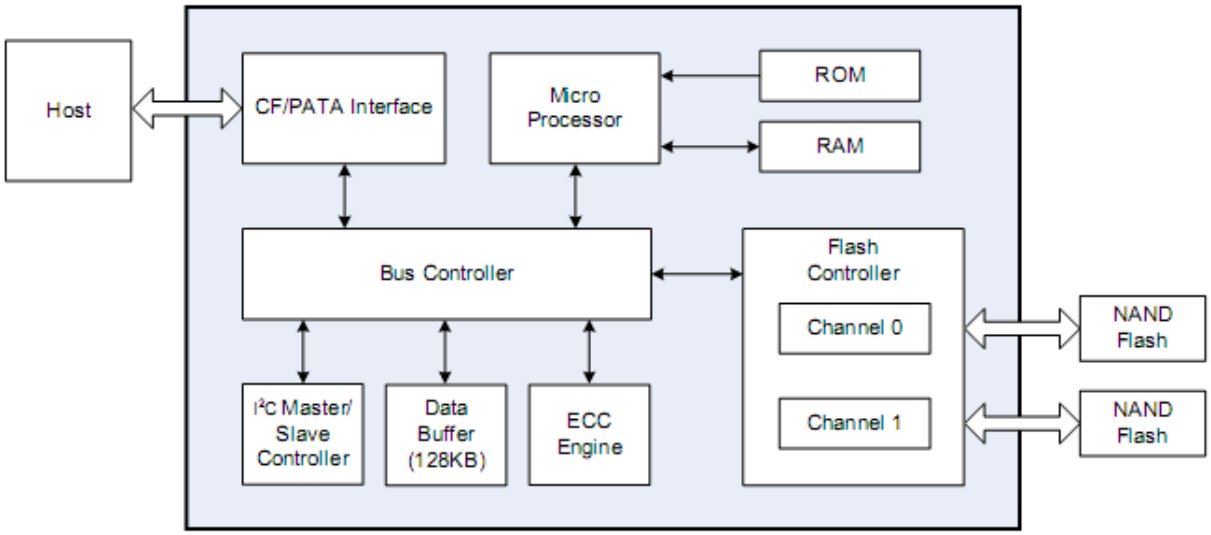


Figure 2-1 Functional Block Diagram

3. Pin Assignments

Table 3-1 lists the pin assignments with respective signal names for the 50-pin configuration. A "#" suffix indicates the active low signal. The pin type can be input, output or input/output.

Table 3-1 Pin Assignments

Pin No.	Memory card mode		I/O card mode		True IDE mode	
	Signal name	Pin I/O type	Signal name	Pin I/O type	Signal name	Pin I/O type
1	GND	-	GND	-	GND	-
2	D3	I/O	D3	I/O	D3	I/O
3	D4	I/O	D4	I/O	D4	I/O
4	D5	I/O	D5	I/O	D5	I/O
5	D6	I/O	D6	I/O	D6	I/O
6	D7	I/O	D7	I/O	D7	I/O
7	#CE1	I	#CE1	I	#CS0	I
8	A10	I	A10	I	A10[1]	I
9	#OE	I	#OE	I	#ATA SEL	I
10	A9	I	A9	I	A9[1]	I
11	A8	I	A8	I	A8[1]	I
12	A7	I	A7	I	A7[1]	I
13	VCC	-	VCC	-	VCC	-
14	A6	I	A6	I	A6[1]	I
15	A5	I	A5	I	A5[1]	I
16	A4	I	A4	I	A4[1]	I
17	A3	I	A3	I	A3[1]	I
18	A2	I	A2	I	A2	I
19	A1	I	A1	I	A1	I
20	A0	I	A0	I	A0	I
21	D0	I/O	D0	I/O	D0	I/O
22	D1	I/O	D1	I/O	D1	I/O
23	D2	I/O	D2	I/O	D2	I/O
24	WP	O	#IOIS16	O	#IOCS16	O
25	#CD2	O	#CD2	O	#CD2	O
26	#CD1	O	#CD1	O	#CD1	O
27	D11	I/O	D11	I/O	D11	I/O
28	D12	I/O	D12	I/O	D12	I/O
29	D13	I/O	D13	I/O	D13	I/O
30	D14	I/O	D14	I/O	D14	I/O
31	D15	I/O	D15	I/O	D15	I/O

Pin No.	Memory card mode		I/O card mode		True IDE mode	
	Signal name	Pin I/O type	Signal name	Pin I/O type	Signal name	Pin I/O type
32	#CE2	I	#CE2	I	#CS1	I
33	#VS1	O	#VS1	O	#VS1	O
34	#IORD	I	#IORD	I	#IORD	I
35	#IOWR	I	#IOWR	I	#IOWR	I
36	#WE	I	#WE	I	#WE	I
37	RDY/-BSY	O	#IREQ	O	INTRQ	O
38	VCC	-	VCC	-	VCC	-
39	#CSEL	I	#CSEL	I	#CSEL	I
40	#VS2	O	#VS2	O	#VS2	O
41	RESET	I	RESET	I	#RESET	I
42	#WAIT	O	#WAIT	O	IORDY	O
43	#INPACK	O	#INPACK	O	DMARQ[2]	O
44	#REG	I	#REG	I	DMACK[2]	I
45	BVD2	O	#SPKR	O	#DASP	I/O
46	BVD1	O	#STSCHG	O	#PDIAG	I/O
47	D8	I/O	D8	I/O	D8	I/O
48	D9	I/O	D9	I/O	D9	I/O
49	D10	I/O	D10	I/O	D10	I/O
50	GND	-	GND	-	GND	-

Notes:
1. The signal should be grounded by the host.
2. Connection required when UDMA is in use.

4. Product Specifications

4.1 Capacity

Capacity specifications of the Compact Flash Card series (CFC) are available as shown in Table 4-1. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

Table 4-1 Capacity Specifications

Capacity	Total bytes	Cylinders	Heads	Sectors	Total LBA
8 GB	8,195,604,480	15,880	16	63	16,007,040
16 GB	16,391,340,032	16,383	16	63	32,014,336
32 GB	32,019,316,736	16,383	16	63	62,537,728
64 GB	64,030,244,864	16,383	16	63	125,059,072

Notes:
- Display of total bytes varies from operating systems.
- Cylinders, heads or sectors are not applicable for these capacities. Only LBA addressing applies.
- 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.
- LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

4.2 Performance

Performance of the CF cards is listed below in Table 4-2.

Table 4-2 Performance Specifications

Capacity / Performance	8 GB	16 GB	32 GB	64 GB
Sequential Read (MB/s)	80	115	115	115
Sequential Write (MB/s)	27	47	44	75
4K Random Read (IOPS)	3,300	3,500	3,400	3,400
4K Random Write (IOPS)	17	33	111	231

Notes:
- Results may differ from various flash configurations or host system setting.
- Sequential read/write is based on CrystalDiskMark 5.2.1 with file size 1,000MB.
- Random read/write is measured using IOMeter with Queue Depth 32.

4.3 Environmental Specifications

Environmental specifications of the Compact Flash Card series (CFC) are shown in Table 4-3.

Table 4-3 Environmental Specifications

Item	Specifications
Operating temp.	0°C to 70°C (Standard); -40°C to 85°C (Wide)
Non-operating temp.	-40°C to 100°C
Operating vibration	7.69 GRMS, 20~2000 Hz/random (compliant with MIL-STD-810G)
Non-operating vibration	4.02 GRMS, 15 ~ 2000 Hz/random (compliant with MIL-STD-810G)
Operating shock	50G, 11ms, half-sine wave
Non-operating shock	1,500G, 0.5ms, half-sine wave

Note: This Environmental Specification table indicates the conditions for testing the device. Real world usages may affect the results.

4.4 Mean Time Between Failures (MTBF)

MTBF, an acronym for Mean Time Between Failures, is a measure of a device's reliability. Its value represents the average time between a repair and the next failure. The measure is typically in units of hours. The higher the MTBF value, the higher the reliability of the device. The predicted result of this CompactFlash Card is higher than 1,000,000 hours.

4.5 Certification and Compliance

The CompactFlash card complies with the following global standards:

- CE
- UKCA
- FCC
- Halogen-free
- RoHS Recast (2011/65/EU)

4.6 Endurance

The endurance of a storage device is predicted by TeraBytes Written based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

Table 4-4 Endurance Specifications

Capacity	TeraBytes Written
8 GB	22
16 GB	42
32 GB	87
64 GB	182

Notes:

- This estimation complies with JEDEC JESD-219, enterprise endurance workload of sequential data with payload size distribution.
- Flash vendor guaranteed MLC P/E cycle: Toshiba – 3k
- WAF/WLE may vary from capacity, flash configurations and writing behavior on each platform.
- 1 Terabyte = 1,000 GB

5. Flash Management

5.1 Error Correction Code (ECC)

The CompactFlash card is programmed with BCH Error Detection Code (EDC) and Error Correction Code (ECC) algorithms capable of correcting up to 72 random bits in 1KB bytes data.

High performance is achieved through hardware-based error detection and correction.

5.2 Flash Block Management

Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, block mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

5.3 Global Wear Leveling

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Global Wear leveling is an important mechanism that levels out the wearing of blocks so that the wearing-down of all blocks can be almost evenly distributed. This will increase the lifespan of SSDs.

5.4 Flash Translation Layer – Page Mapping

Page mapping is an advanced flash management technology whose essence lies in the ability to gather data, distribute the data into flash pages automatically, and then schedule the data to be evenly written. Page-level mapping uses one page as the unit of mapping. The most important characteristic is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different sizes of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. Thus, page mapping is adopted to increase random access speed and improve SSD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

5.5 Power Failure Management

Power Failure Management plays a crucial role when power supply becomes unstable. Power disruption may occur when users are storing data into the SSD, leading to instability in the drive. However, with Power Failure Management, a firmware protection mechanism will be activated to scan pages and blocks once power is resumed. Valid data will be transferred to new blocks for merging and the mapping table will be rebuilt. Therefore, data reliability can be reinforced, preventing damage to data stored in the NAND Flash.

5.6 S.M.A.R.T. Technology

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

Table 5-1 SMART Attribute ID List

ID (Hex)	Attribute Name
12 (0x0C)	Power Cycle Count
160 (0xA0)	Initial Bad Block Count
161 (0xA1)	Bad Block Count
162 (0xA2)	Spare Block Count
163 (0xA3)	Maximum Erase Count
165 (0xA5)	Average Erase Count

6. Software Interface

6.1 CF-ATA Command Set

Table 6-1 summarizes the CF-ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 6-1 CFC-ATA Command Set

Command Set	Command	Code	Protocol
CFA Feature Set	Request Sense	03h	Non-data
	Write Sectors Without Erase	38h	PIO data-out
	Erase Sectors	C0h	Non-data
	Write Multiple Without Erase	CDh	PIO data-out
	Translate Sector	87h	PIO data-in
	Write Multiple w/o erase	CDh	PIO
	Write sector(s) w/o erase	38h	PIO
General Feature Set	Execute Drive Diagnostic	90h	Device diagnostic
	Flush Cache	E7h	Non-data
	Identify Device	ECh	PIO data-in
	Read DMA	C8h	DMA
	Read Multiple	C4h	PIO data-in
	Read Sector(s)	20h or 21h	PIO data-in
	Read Verify Sector(s)	40h or 41h	Non-data
	Set Feature	EFh	Non-data
	Set Multiple Mode	C6h	Non-data
	Write DMA	CAh	DMA
	Write Multiple	C5h	PIO data-out
	Write Sector(s)	30h or 31h	PIO data-out
	NOP	00h	Non-data
	Read Buffer	E4h	PIO data-in
	Write Buffer	E8h	PIO data-out
	Set Feature	EFh	Non-data
Power Management Feature Set	Check Power Mode	E5h or 98h	Non-data
	Idle	E3h or 97h	Non-data
	Idle Immediate	E1h or 95h	Non-data
	Set sleep mode	E6h or 99h	Non-data
	Sleep	E6h or 99h	Non-data
	Standby	E2h or 96h	Non-data
	Standby Immediate	E0h or 94h	Non-data
Security Mode Feature Set	Security Set Password	F1h	PIO data-out
	Security Unlock	F2h	PIO data-out

Command Set	Command	Code	Protocol
	Security Erase Prepare	F3h	Non-data
	Security Erase Unit	F4h	PIO data-out
	Security Freeze Lock	F5h	Non-data
	Security Disable Password	F6h	PIO data-out
	Media Lock	DEh	Non-data
	Media Unlock	DFh	Non-data
SMART Feature Set	SMART Disable Operations	B0h	Non-data
	SMART Enable/Disable Autosave	B0h	Non-data
	SMART Enable Operations	B0h	Non-data
	SMART Return Status	B0h	Non-data
	SMART Execute Off-line Immediate	B0h	Non-data
	SMART Read Data	B0h	PIO data-in
Host Protected Area Feature Set	Data Set Management	06h	DMA
	Read Native Max Address	F8h	Non-data
	Read native max addr Ext	27h	Non-data
	Set Max Address	F9h	Non-data
Others	Format Track	50h	PIO data-out
	Initialize Drive Parameters	91h	Non-data
	Recalibrate	1Xh	Non-data
	Seek	7Xh	Non-data
	Write Verify	3Ch	PIO data-out
	Download Microcode	92h	PIO data-in
	Download Microcode DMA	93h	DMA
48-bit Address Feature Set	Read Sector Ext	24h	PIO data-in
	Read DMA Ext	25h	DMA
	Read Multiple Ext	29h	PIO data-in
	Write Sector Ext	34h	PIO data-out
	Write DMA Ext	35h	DMA
	Read Verify Sector Ext	42h	Non-data
	Write Multiple FUA Ext	CEh	PIO data-out
	Flush Cache Ext	EAh	Non-data
	Read Log Ext	2Fh	PIO
	Read Log DMA Ext	57h	DMA
	Write DMA FUA Ext	3Dh	DMA
	Write Log Ext	3Fh	PIO
	Write Log DMA Ext	57h	DMA
	Write Multiple Ext	39h	PIO
	Set max address Ext	37h	Non-data

7. Electrical Specifications

7.1 Operating Voltage

Table 7-1 lists the supply voltage for the CompactFlash card.

Table 7-1 Operating Range

Item	Range
Supply voltage at 3.3V	3.135 to 3.465 V
Supply voltage at 5V	4.75 to 5.25 V

7.2 Power Consumption

Table 7-2 and 7-3 list the power consumption for the CompactFlash card.

Table 7-2 Power Consumption @3.3V (Unit: mA)

Capacity / Mode	8 GB	16 GB	32 GB	64 GB
Active (Max.)	195	250	245	255
Standby	10	10	10	10

Table 7-3 Power Consumption @5V (Unit: mA)

Capacity / Mode	8 GB	16 GB	32 GB	64 GB
Active (Max.)	200	260	255	260
Standby	10	10	10	10

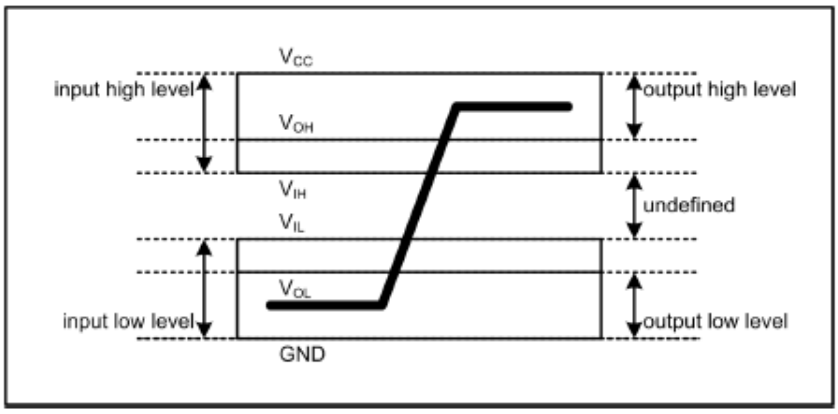
Notes:
- All values are typical and may vary depending on flash configurations or host system settings.
- Power consumption is measured using CrystalDiskMark 5.2.1.

7.3 AC/DC Characteristics

The following section provides general AC/DC characteristics of this CompactFlash card.

7.3.1 General DC Characteristics

Definitions of V_{IH}, V_{CC}, V_{OH}, V_{OL}



- **DC characteristics for host interface (Vcc = 3.3V/5V)**

Parameter	Symbol	Minimum	Maximum	Unit	Remark
Supply Voltage 5V	Vcc	4.5	5.5	V	
Supply voltage 3.3V	Vcc	2.97	3.63	V	
High Level Output Voltage	VOH	2.5		V	
Low Level Output Voltage	VOL		0.4	V	
High Level Input Voltage	VIH	2.4		V	Non-Schmitt trigger
		2.05		V	Schmitt trigger
Low Level Input Voltage	VIL		0.6	V	Non-Schmitt trigger
			1.25	V	Schmitt trigger
Pull-up Resistance	RPU	52.7	141	kOhm	
Pull-down Resistance	RPD	47.5	172	kOhm	

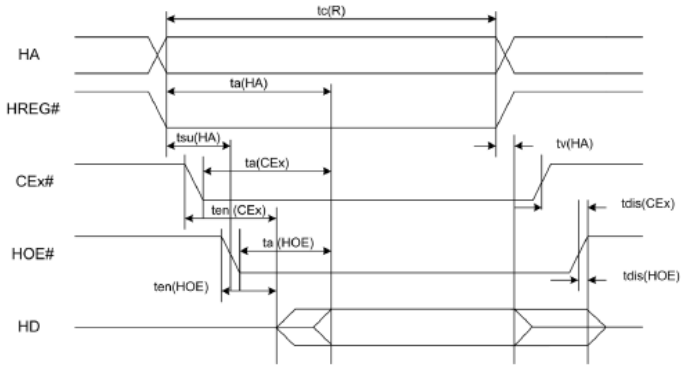
- **General DC characteristics**

Parameter	Symbol	Minimum	Maximum	Unit	Remark
Supply Voltage	Vcc	2.7	3.6	V	
High Level Output Voltage	VOH	2.4		V	
Low Level Output Voltage	VOL		0.4	V	
High Level Input Voltage	VIH	2.0		V	Non-Schmitt trigger
		1.4	2.0	V	Schmitt trigger
Low Level Input Voltage	VIL		0.8	V	Non-Schmitt trigger
			1.2	V	Schmitt trigger
Pull-up Resistance	RPU	40		kOhm	
Pull-down Resistance	RPD	40		kOhm	

7.3.2 General AC Characteristics

- **Attribute Memory Read Timing**

Item	Symbol	Min. (ns)	Max. (ns)
Read Cycle Time	tc (R)	300	
Address Access Time	ta (HA)		300
Card Enable Access Time	ta (CEx)		300
Output Enable Access Time	ta (HOE)		150
Output Disable Time from CEx#	tdis (CEx)		100
Output Disable Time from HOE#	tdis (HOE)		100
Address Setup Time	tsu (HA)	30	
Output Enable Time from CEx#	ten (CEx)	5	
Output Enable Time from HOE#	ten (HOE)	5	
Data Valid from Address Change	tv (HA)	0	

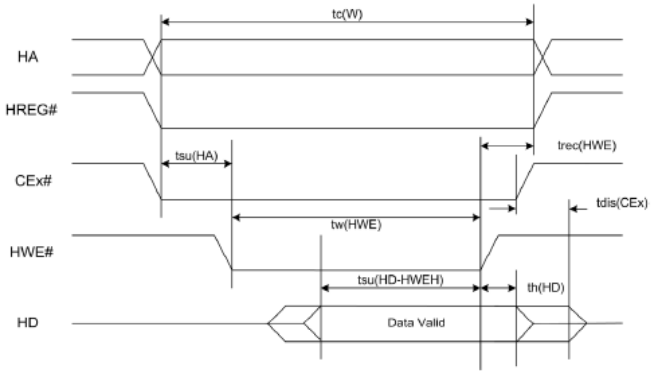


Note: all time intervals are in nanoseconds. HD refers to the data provided by the CompactFlash card to the system. The CEx# signal or both of the HOE# and the HWE# signal are de-asserted between consecutive cycle operations.

- **Attribute Memory Write Timing**

Item	Symbol	Min. (ns)	Max. (ns)
Write Cycle Time	tc (W)	250	
Write Pulse Width	tw (HWE)	150	
Address setup Time	tsu (HA)	30	
Write Recovery Time	trec (HWE)	30	
Data Setup Time for HWE#	tsu (HD-HWEH)	80	
Data Hold Time	th (HD)	30	

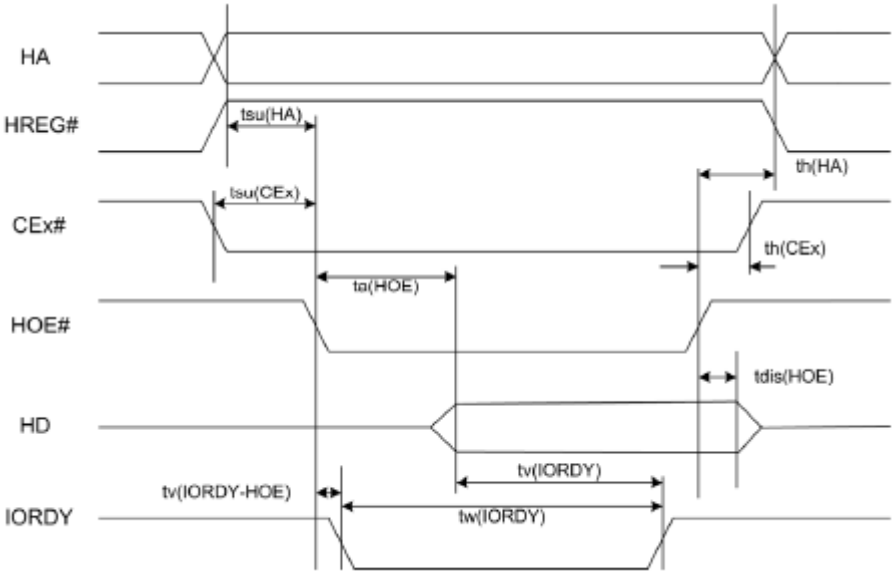
Note: all time intervals are in nanoseconds. HD refers to the data provided by the CompactFlash card to the system.



- **Common Memory Read Timing**

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
Output Enable Access Time	ta (HOE)		125		60		50		45
Output Disable Time from HOE#	tdis (HOE)		100		60		50		45
Address Setup Time	tsu (HA)	30		15		10		10	
Address Hold Time	th (HA)	20		15		15		10	
CEx# Setup before HOE#	tsu (CEx)	5		5		5		5	
CEx# Hold following HOE#	th (CEx)	20		15		15		10	
Wait Delay falling from HOE#	tv (IORDY-HOE)		35		35		35		Na
Data Setup for Wait Release	tv (IORDY)		0		0		0		Na
Wait Width Time	tw (IORDY)		350		350		350		Na

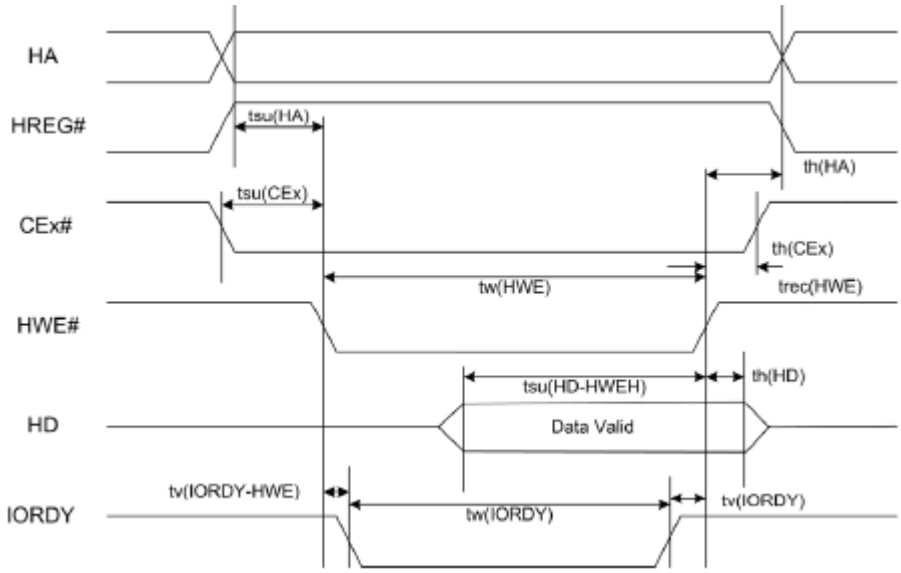
Note: IORDY is not supported in this 80 ns mode. The maximum load on IORDY is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All time intervals are in nanoseconds. HD refers to the data provided by the CompactFlash card to the system. The IORDY signal can be ignored when the HOE# cycle-to-cycle time is greater than the Wait Width Time. The Max Wait Width Time can be determined from the Card Information Structure (CIS). Although adhering to the PCM-CIA specification, the Wait Width Time is intentionally designed to be lower in this specification.



- **Common Memory Write Timing**

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
Data Setup before HWE#	tsu (HD-HWEH)	80		50		40		30	
Data Hold following HWE#	th (HD)	30		15		10		10	
HWE# Pulse Width	tw (HWE)	150		70		60		55	
Address Setup Time	tsu (HA)	30		15		10		10	
CEx# Setup before HWE#	tsu (CEx)	5		5		5		5	
Write Recovery Time	trec (HWE)	30		15		15		15	
Address Hold Time	th (HA)	20		15		15		15	
CEx# Hold following HWE#	th (CEx)	20		15		15		10	
Wait Delay falling from HWE#	tv (IIORDY-HWE)		35		35		35		Na
HWE# High from Wait Release	tv (IORDY)	0		0		0		Na	
Wait Width Time	tw (IORDY)		350		350		350		Na

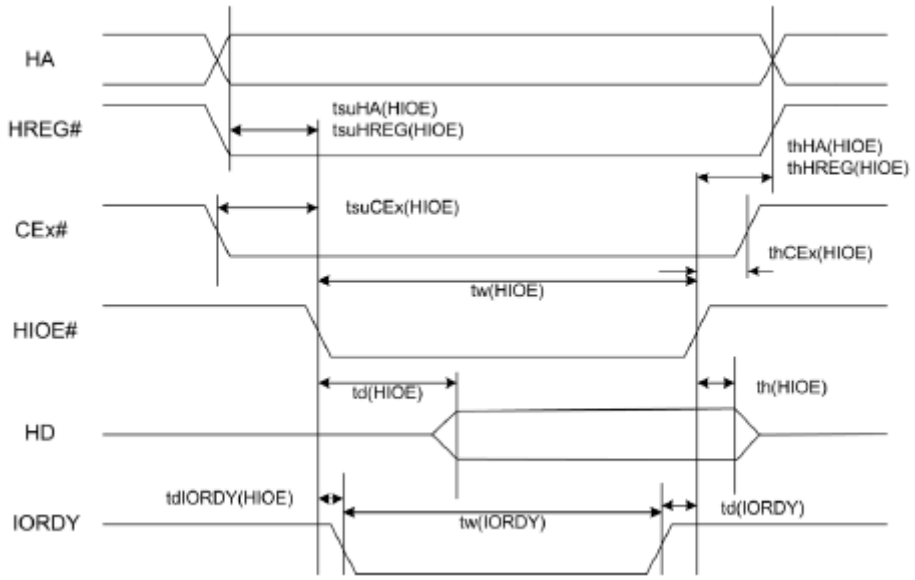
Note: IORDY is not supported in this 80 ns mode. The maximum load on IORDY is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All time intervals are in nanoseconds. HD refers to the data provided by the CompactFlash card to the system. The IORDY signal can be ignored when the HWE# cycle-to-cycle time is greater than the Wait Width Time. The Max Wait Width Time can be determined from the Card Information Structure (CIS). Although adhering to the PCM-CIA specification, the Wait Width Time is intentionally designed to be lower in this specification.



- **I/O Read Timing**

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
Data Delay after HIOE#	td (HIOE)		100		50		50		45
Data Hold following HIOE#	th (HIOE)	0		5		5		5	
HIOE# Width Time	tw (HIOE)	165		70		65		55	
Address Setup before HIOE#	tsuHA (HIOE)	70		25		25		15	
Address Hold following HIOE#	thHA (HIOE)	20		10		10		10	
CEx# Setup before HIOE#	tsuCEx (HIOE)	5		5		5		5	
CEx# Hold following HIOE#	thCEx (HIOE)	20		10		10		10	
HREG# Setup before HIOE#	tsuHREG (HIOE)	5		5		5		5	
HREG# Hold following HIOE#	thHREG (HIOE)	0		0		0		0	
Wait Delay falling from HIOE#	tdIORDY (HIOE)		35		35		35		Na
Data Delay from Wait Rising	td (IORDY)		0		0		0		na
Wait Width Time	tw (IORDY)		350		350		350		Na

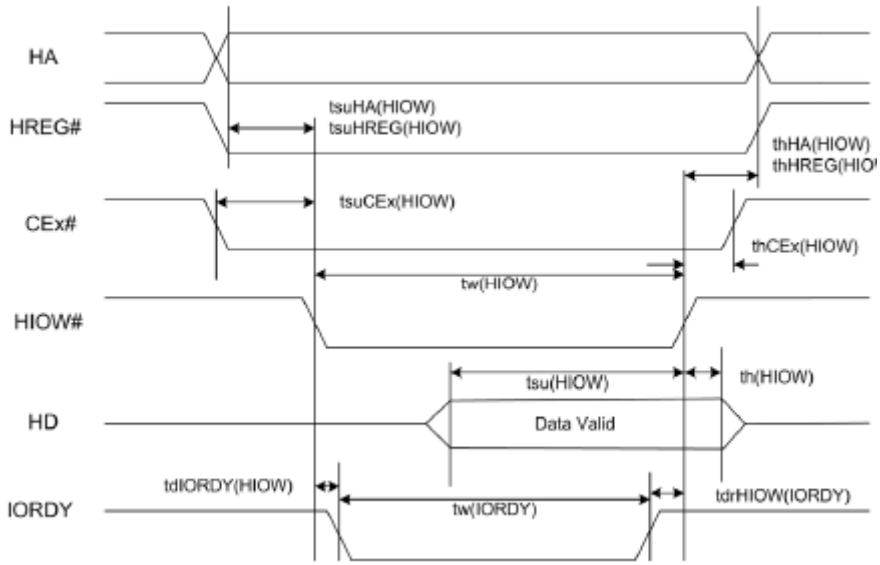
Note: IORDY is not supported in this 80 ns mode. Maximum load on IORDY is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All time intervals are in nanoseconds. Although minimum time from IORDY high to HIOE# high is 0 nsec, the minimum HIOE# width is still met. HD refers to data provided by the CompactFlash Card to the system. Although following PCMCIA specification, the Wait Width Time is intentionally lower in this specification.



- **I/O Write Timing**

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
Data Setup before HIOW#	tsu (HIOW)	60		20		20		15	
Data Hold following HIOW#	th (HIOW)	30		10		5		5	
HIOW# Width Time	tw (HIOW)	165		70		65		65	
Address Setup before HIOW#	tsuHA (HIOW)	70		25		25		15	
Address Hold following HIOW#	thHA (HIOW)	20		20		10		10	
CEx# Setup before HIOW#	tsuCEx (HIOW)	5		5		5		5	
CEx# Hold following HIOW#	thCEx (HIOW)	20		20		10		10	
HREG# Setup before HIOW#	tsuHREG (HIOW)	5		5		5		5	
HREG# Hold following HIOW#	thHREG (HIOW)	0		0		0		0	
Wait Delay falling from HIOW#	tdIORDY (HIOW)		35		35		35		na
HIOW# high from Wait High	tdHIOW (IORDY)	0		0		0		na	
Wait Width Time	tw (IORDY)		350		350		350		na

Note: IORDY is not supported in this 80 ns mode. The maximum load on IORDY is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All time intervals are in nanoseconds. Although minimum time from IORDY high to HIOW# high is 0 nsec, the minimum HIOW# width is still met. HD refers to data provided by the CompactFlash Card to the system.



- **True IDE PIO Mode Read/Write Timing**

Item	Symbol	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
Cycle Time (Min.)	t0	600	383	240	180	120	100	80
Address Valid to HIOE# / HIOW# Setup (Min.)	t1	70	50	30	30	25	15	10
HIOE# / HIOW# (Min.)	t2	165	125	100	80	70	65	55
HIOE# / HIOW# (Min.) Register (8-bit)	t2	290	290	290	80	70	65	55
HIOE# / HIOW# Recovery Time (Min.)	t2i	-	-	-	70	25	25	20
HIOW# Data Setup (Min.)	t3	60	45	30	30	20	20	15
HIOW# Data Hold (Min.)	t4	30	20	15	10	10	5	5
HIOE# Data Setup (Min.)	t5	50	35	20	20	20	15	10
HIOE# Data Hold (Min.)	t6	5	5	5	5	5	5	5
HIOE# Data Tristate (Max.)	t6Z	30	30	30	30	30	20	20
Address Valid to IOCS16# Assertion (Max.)	t7	90	50	40	n/a	n/a	n/a	n/a
Address Valid to IOCS16# released (Max.)	t8	60	45	30	n/a	n/a	n/a	n/a
HIOE# / HIOW# to Address Valid Hold	t9	20	15	10	10	10	10	10
Read Data Valid to IORDY Active (Min.), if IORDY initially low after tA	tRD	0	0	0	0	0	0	0
IORDY Setup Time	tA	35	35	35	35	35	Na	Na
IORDY Pulse Width (Max.)	tB	1250	1250	1250	1250	1250	Na	Na
IORDY Assertion to Release (Max.)	tC	5	5	5	5	5	Na	Na

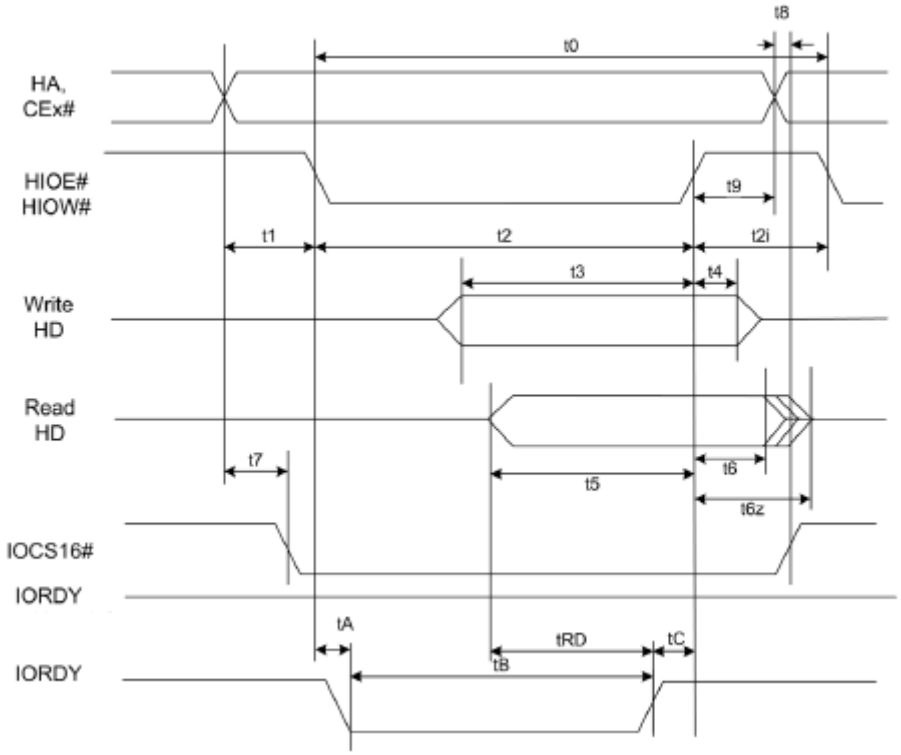
Note: All timing intervals are measured in nanoseconds. The maximum load on IOCS16# is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All time intervals are in nanoseconds. Although minimum time from IORDY high to HIOE# high is 0 nsec, the minimum HIOE# width is still met.

Where t0 denotes the minimum total cycle time; t2 represents the minimum command active time; t2i is the minimum command recovery time or command inactive time. Actual cycle time equals to the sum of actual command active time and actual command inactive time. The three timing requirements for t0, t2, and t2i are met. The minimum total cycle time requirement is greater than the sum of t2 and t2i, implying that a host implementation can extend either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device identity data. A CompactFlash card implementation supports any legal host implementation.

The delay originates from HIOW# or HIOW# activation until the state of IORDY is first sampled. If IORDY is inactive, the host waits until IORDY is active before the PIO cycle is completed. When the CompactFlash Card is not driving IORDY, which is negated at tA after HIOE# or HIOW# activation, then t5 is met and tRD is inapplicable. When the CompactFlash Card is driving IORDY, which is negated at the time tA after HIOE# or HIOW# activation, then tRD is met and t5 is inapplicable.

Both t7 and t8 apply to modes 0, 1, and 2 only. For other modes, the signal is invalid.

IORDY is not supported in this mode.



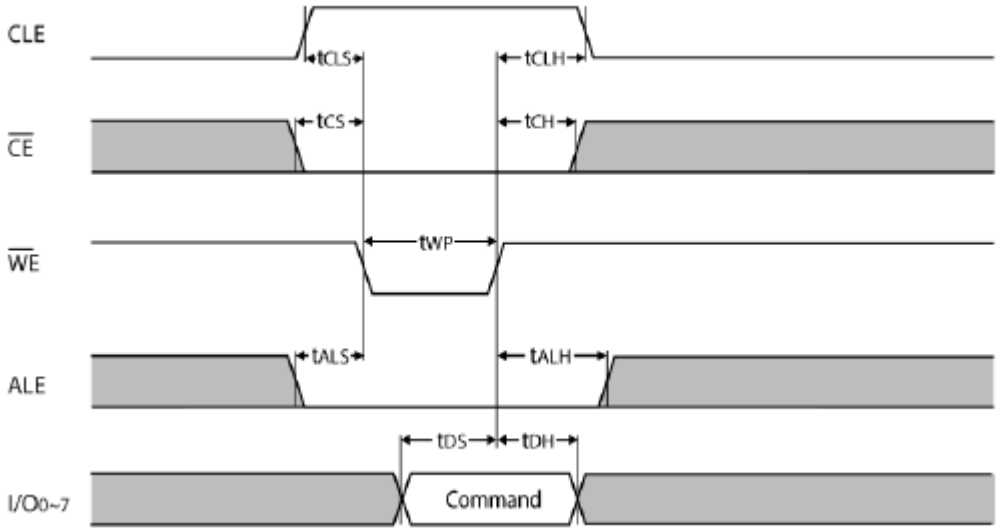
Device address comprises CE1#, CE2#, and HA[2:0]
Data comprises HD[15:0] (16-bit) or HD[7:0] (8-bit)
IOCS16# is shown for PIO modes 0, 1, and 2. For other modes, the signal is ignored.
The negation of IORDY by the device is used to lengthen the PIO cycle. Whether the cycle is to be extended is determined by the host after tA from the assertion of HIOE# or HIOW#. The assertion and negation of IORDY is described in the following cases. First, the device never negates IORDY, so no wait is generated. Secondly, device drives IORDY low before tA. Thus, wait is generated. The cycle is completed after IORDY is re-asserted. For cycles in which a wait is generated and HIOE# is asserted, the device places read data on D15-D00 for tRD before IORDY is asserted.

- **Flash Interface AC Characteristics**

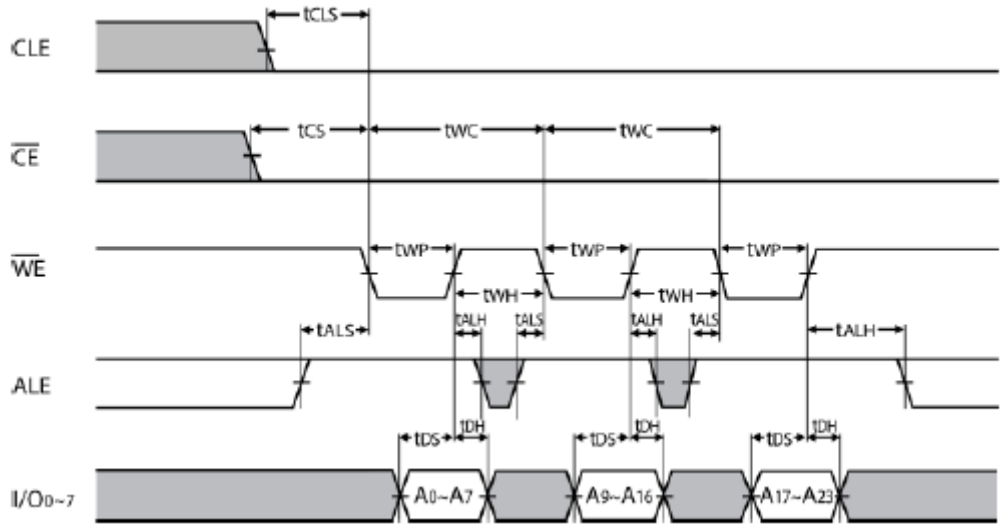
Parameter	Symbol	Timing		Unit
		Disable Flash CMD Extend	Enable Flash CMD Extend	
CLE Setup time	tCLS	2	4	tCK
CLE hold time	tCLH	1	2	tCK
ALE setup time	tALS	2	4	tCK
ALE hold time	tALH	1	2	tCK
WE pulse width	tWP	1	2	tCK
Data setup time	tDS	1	3	tCK
Data hold time	tDH	1	1	tCK
Write cycle time	tWC	2	4	tCK
WE high hold time	tWH	1	2	tCK
WE Low hold time	tWP	1	2	tCK

Parameter	Symbol	Timing	Unit
WE Pulse Width	tWP	0.5	tCK
Data setup time	tDS	0.75	tCK
Data hold time	tDH	0.25	tCK
Write cycle time	tWC	1	tCK
WE high hold time	tWH	0.5	tCK
WE pulse width	tWP	0.5	tCK
Read cycle time	tRC	1	tCK
RE Pulse Width	tRP	0.5	tCK
RE High Hold Time	tREH	0.5	tCK

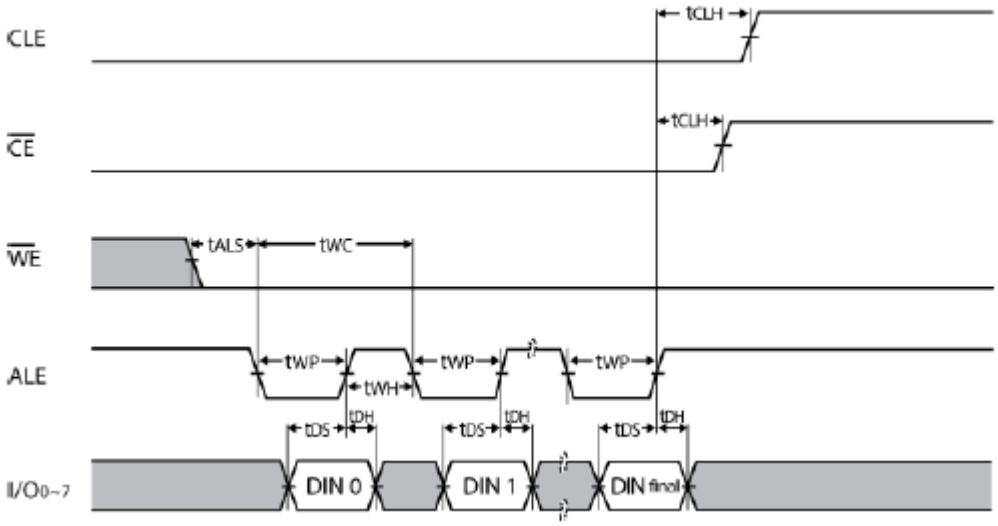
- **Command Latch Cycle**



- **Address Latch Cycle**



- **Input Data Latch Cycle**



8. Mechanical Specifications

8.1 Dimensions

8.1.1 Without Write Protect Switch

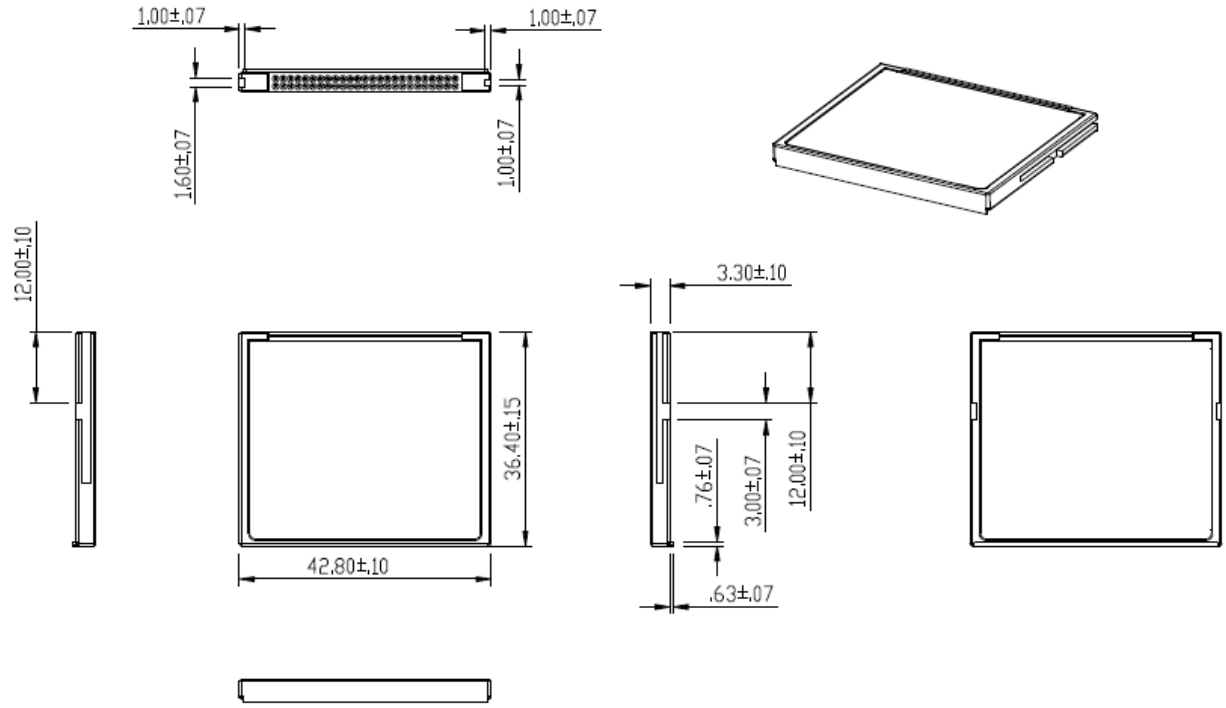


Figure 8-1 Physical Dimensions

Unit: mm

8.1.2 With Write Protect Switch

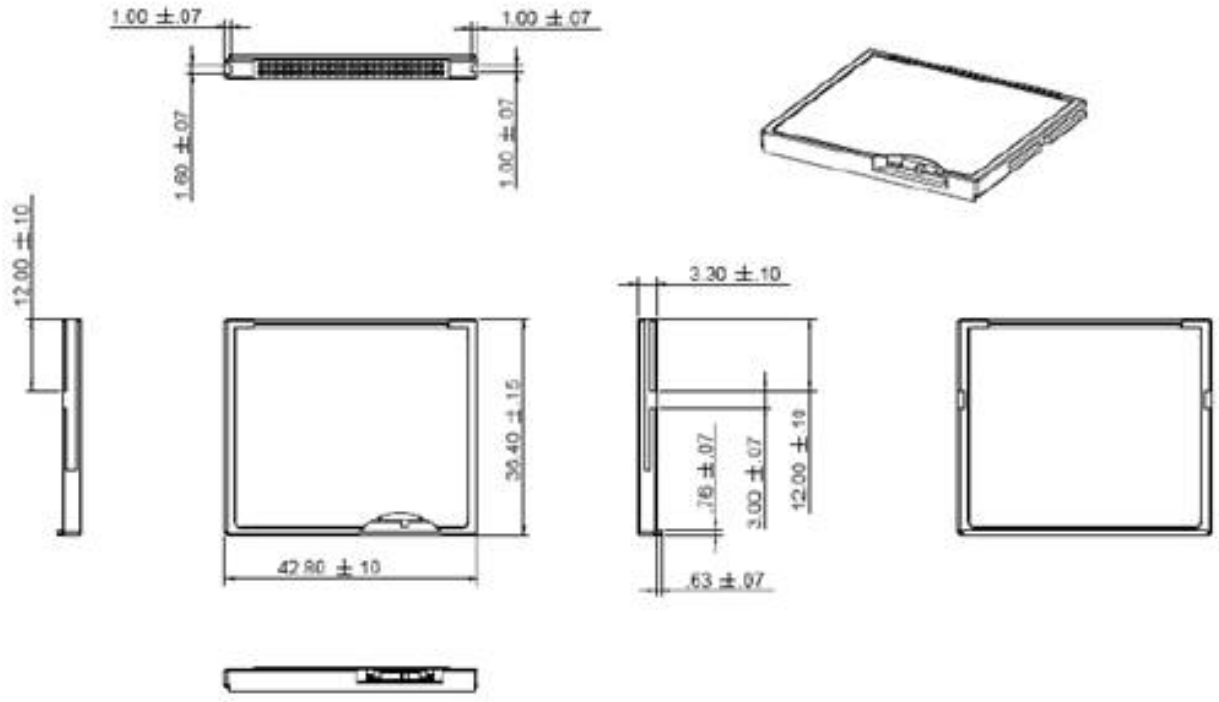


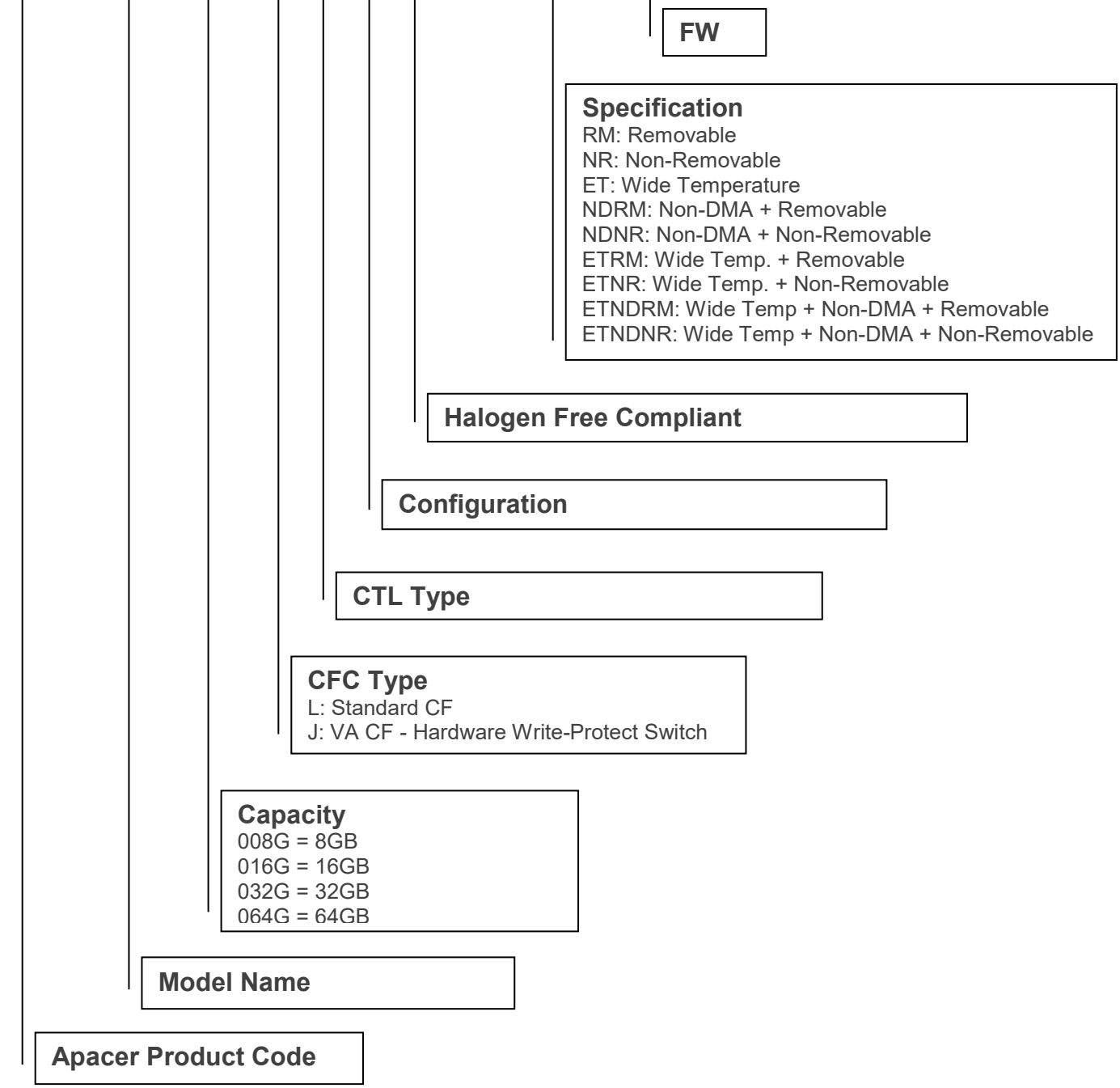
Figure 8-2 Physical Dimensions

Unit: mm

9. Product Ordering Information

9.1 Product Code Designations

AP – CF xxxG X B N S – XXXXXX G



9.2 Valid Combinations

The following tables list the available models of the CompactFlash Card series which are in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

A. Standard CF - Standard Temperature

9.2.1 Non-Removable

Capacity	Part Number
8GB	AP-CF008GLBNS-NRG
16GB	AP-CF016GLBNS-NRG
32GB	AP-CF032GLBNS-NRG
64GB	AP-CF064GLBNS-NRG

9.2.2 Removable

Capacity	Part Number
8GB	AP-CF008GLBNS-RMG
16GB	AP-CF016GLBNS-RMG
32GB	AP-CF032GLBNS-RMG
64GB	AP-CF064GLBNS-RMG

9.2.3 Non-DMA + Non-Removable

Capacity	Part Number
8GB	AP-CF008GLBNS-NDNRG
16GB	AP-CF016GLBNS-NDNRG
32GB	AP-CF032GLBNS-NDNRG
64GB	AP-CF064GLBNS-NDNRG

9.2.4 Non-DMA + Removable

Capacity	Part Number
8GB	AP-CF008GLBNS-NDRMG
16GB	AP-CF016GLBNS-NDRMG
32GB	AP-CF032GLBNS-NDRMG
64GB	AP-CF064GLBNS-NDRMG

B. Standard CF – Wide Temperature

9.2.5 Non-Removable

Capacity	Part Number
8GB	AP-CF008GLBNS-ETNRG
16GB	AP-CF016GLBNS-ETNRG
32GB	AP-CF032GLBNS-ETNRG
64GB	AP-CF064GLBNS-ETNRG

9.2.6 Removable

Capacity	Part Number
8GB	AP-CF008GLBNS-ETRMG
16GB	AP-CF016GLBNS-ETRMG
32GB	AP-CF032GLBNS-ETRMG
64GB	AP-CF064GLBNS-ETRMG

9.2.7 Non-DMA + Non-Removable

Capacity	Part Number
8GB	AP-CF008GLBNS-ETNDNRG
16GB	AP-CF016GLBNS-ETNDNRG
32GB	AP-CF032GLBNS-ETNDNRG
64GB	AP-CF064GLBNS-ETNDNRG

9.2.8 Non-DMA + Removable

Capacity	Part Number
8GB	AP-CF008GLBNS-ETNDRMG
16GB	AP-CF016GLBNS-ETNDRMG
32GB	AP-CF032GLBNS-ETNDRMG
64GB	AP-CF0642GLBNS-ETNDRMG

C. VA CF – Standard Temperature

9.2.9 Non-Removable

Capacity	Part Number
8GB	AP-CF008GJBNS-NRG
16GB	AP-CF016GJBNS-NRG
32GB	AP-CF032GJBNS-NRG
64GB	AP-CF064GJBNS-NRG

9.2.10 Removable

Capacity	Part Number
8GB	AP-CF008GJBNS-RMG
16GB	AP-CF016GJBNS-RMG
32GB	AP-CF032GJBNS-RMG
64GB	AP-CF064GJBNS-RMG

9.2.11 Non-DMA + Non-Removable

Capacity	Part Number
8GB	AP-CF008GJBNS-NDNRG
16GB	AP-CF016GJBNS-NDNRG
32GB	AP-CF032GJBNS-NDNRG
64GB	AP-CF064GJBNS-NDNRG

9.2.12 Non-DMA + Removable

Capacity	Part Number
8GB	AP-CF008GJBNS-NDRMG
16GB	AP-CF016GJBNS-NDRMG
32GB	AP-CF032GJBNS-NDRMG
64GB	AP-CF064GJBNS-NDRMG

D. VA CF – Wide Temperature

9.2.13 Non-Removable

Capacity	Part Number
8GB	AP-CF008GJBNS-ETNRG
16GB	AP-CF016GJBNS-ETNRG
32GB	AP-CF032GJBNS-ETNRG
64GB	AP-CF064GJBNS-ETNRG

9.2.14 Removable

Capacity	Part Number
8GB	AP-CF008GJBNS-ETRMG
16GB	AP-CF016GJBNS-ETRMG
32GB	AP-CF032GJBNS-ETRMG
64GB	AP-CF064GJBNS-ETRMG

9.2.15 Non-DMA + Non-Removable

Capacity	Part Number
8GB	AP-CF008GJBNS-ETNDNRG
16GB	AP-CF016GJBNS-ETNDNRG
32GB	AP-CF032GJBNS-ETNDNRG
64GB	AP-CF064GJBNS-ETNDNRG

9.2.16 Non-DMA + Removable

Capacity	Part Number
8GB	AP-CF008GJBNS-ETNDRMG
16GB	AP-CF016GJBNS-ETNDRMG
32GB	AP-CF032GJBNS-ETNDRMG
64GB	AP-CF064GJBNS-ETNDRMG

Revision History

Revision	Description	Date
1.0	Official release	5/4/2017
1.1	- Added MTBF on Features page - Changed the description of $1.99x10^6$ hours to 1,000,000 hours at 4.4 Mean Time Between Failures (MTBF)	7/21/2017
1.2	- Added product photos to cover page - Added Power Failure Management to Flash Management on Features page - Added 1.1.5 Power Failure Management	9/22/2017
1.3	- Changed "Features" to "Specifications Overview" - Updated 4.3 Environmental Specifications	5/24/2018
1.4	- Updated wear-leveling algorithms at Flash Management on Specifications Overview page to Global Wear Leveling - Updated 1.1.2 Wear-Leveling Algorithms to Global Wear Leveling	9/3/2018
1.5	- Renamed extended temperature to wide temperature - Added SMART attribute ID list table to 1.1.3 S.M.A.R.T. Technology - Renamed Power Failure Management to DataDefender at Flash Management on Specifications Overview page and 1.1.5 section and updated the technology description	2/20/2019
1.6	- Added Endurance to Specifications Overview page - Added 4.6 Endurance	2/26/2019
1.7	Removed DataDefender support and replaced it with Power Failure Management at Flash Management on Specifications Overview page and 1.1.5 section	7/16/2019
1.8	- Modified non-operating vibration specification at Table 4-3 by changing sine to random - Added UKCA to and removed EMC from 4.5 Certification and Compliance	1/6/2023

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