Apacer

Halogen-Free & RoHS Recast Compliant

CompactFlash Series 6

Industrial CompactFlash Card Product Specifications

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Version 1.6

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Specifications Overview:

- **CompactFlash Association Specification Revision 6.0 Standard Interface**
  - ATA command set compatible
  - ATA transfer mode supports:
    - PIO Mode 6
    - Multiword DMA Mode 4
    - Ultra DMA Mode 7
    - PCMCIA UDMA Mode 7
- **Capacity**
  - 8, 16, 32, 64, 128 GB
- **Performance***
  - Sequential read: Up to 106 MB/sec
  - Sequential write: Up to 65 MB/sec
- **Power Management**
- **Flash Management**
  - Built-in hardware ECC
  - Global Wear Leveling
  - S.M.A.R.T.
  - Flash Block Management
  - Power Failure Management
- **NAND Flash Type:** MLC
- **Power Smart Design**
  - Built-in 1.2V Power-On-Reset
  - Built-in 2.7V Voltage detector for power fail protection
- **Temperature Range**
  - Operating:
    - Standard: 0°C to 70°C
    - Wide: -40°C to 85°C
  - Storage: -40°C to 100°C
- **Supply Voltage**
  - 3.3 V
  - 5.0 V
- **Power Consumption***

  Operating voltage: 3.3V
  - Active mode: 260
  - Standby mode: 15

  Operating voltage: 5V
  - Active mode: 270
  - Standby mode: 15
- **Connector Type**
  - 50 pins female
- **Physical Dimensions**
  - 36.4mm x 42.8mm x 3.3mm
- **Halogen Free**
- **RoHS Recast Compliant**
  - Complies with 2011/65/EU

*Varies from capacities. The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings.

Table of Contents

1. General Descriptions

Apacer's value-added Industrial CompactFlash Card offers high performance, high reliability and power-efficient storage. Regarding standard compliance, this CompactFlash Card complies with CompactFlash specification revision 6.0, supporting transfer modes up to Programmed Input Output (PIO) Mode 6, Multi-word Direct Memory Access (DMA) Mode 4, Ultra DMA Mode 7, and PCMCIA Ultra DMA Mode 7.

For power efficiency, this industrial CompactFlash card supports some power smart design mechanisms such as Power-On-Reset, voltage regulator for output voltage adjustments and power failure protection, as well as the automatic sleep and wake-up feature.

Apacer's value-added CFC provides complete PCMCIA – ATA functionality and compatibility. Apacer 's CompactFlash technology is designed for applications in Point of Sale (POS) terminals, telecom, IP-STB, medical instruments, surveillance systems, industrial PCs and handheld applications such as the new generation of Digital Single Lens Reflex (DSLR) cameras.

1.1 Performance-Optimized Controller

The CompactFlash Card Controller translates standard CF signals into flash media data and control signals.

1.1.1 Power Management

The controller unit of this ComactFlash is built with power management design that optimizes power utilization and voltage flow. It enhances the power efficiency of CompactFlash Card Controller by employing advanced circuit regulator technology.

1.1.2 RAM

The controller is implemented with RAM as a data process to optimize data transfer between the host and the flash media.

1.1.3 Error Correction Code (ECC)

The CompactFlash card is programmed with BCH Error Detection Code (EDC) and Error Correction Code (ECC) algorithms capable of correcting up to 72 random bits in 1KB bytes data.

High performance is achieved through hardware-based error detection and correction.

1.2 Intelligent Endurance Design

1.2.1 Global Wear Leveling

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Global wear leveling is an important mechanism that levels out the wearing of all blocks so that the wearing-down of all blocks can be almost evenly distributed. This will increase the lifespan of SSDs.

1.2.2 S.M.A.R.T.

S.M.A.R.T. is an acronym for Self-Monitoring, Analysis and Reporting Technology, an open standard allowing disk drives to automatically monitor their own health and report potential problems. It protects the user from unscheduled downtime by monitoring and storing critical drive performance and calibration parameters. Ideally, this should allow taking proactive actions to prevent impending drive failure. Apacer SMART feature adopts the standard SMART command B0h to read data from the drive. When the Apacer SMART Utility running on the host, it analyzes and reports the disk status to the host before the device is in critical condition.

1.2.3 Flash Block Management

Contemporary process technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a highly minimal number of initial bad block during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. On the other hand, bad blocks may develop during program/erase cycles. When host performs program/erase command on a block, bad block may appear in Status Register. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, block mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

1.2.4 Power Failure Management

Power Failure Management plays a crucial role when power supply becomes unstable. Power disruption may occur when users are storing data into the SSD, leading to instability in the drive. However, with Power Failure Management, a firmware protection mechanism will be activated to scan pages and blocks once power is resumed. Valid data will be transferred to new blocks for merging and the mapping table will be rebuilt. Therefore, data reliability can be reinforced, preventing damage to data stored in the NAND Flash.

2. Functional Block

The CompactFlash Card (CFC) includes a controller and flash media, as well as the CompactFlash standard interface. Figure 2-1 shows the functional block diagram.

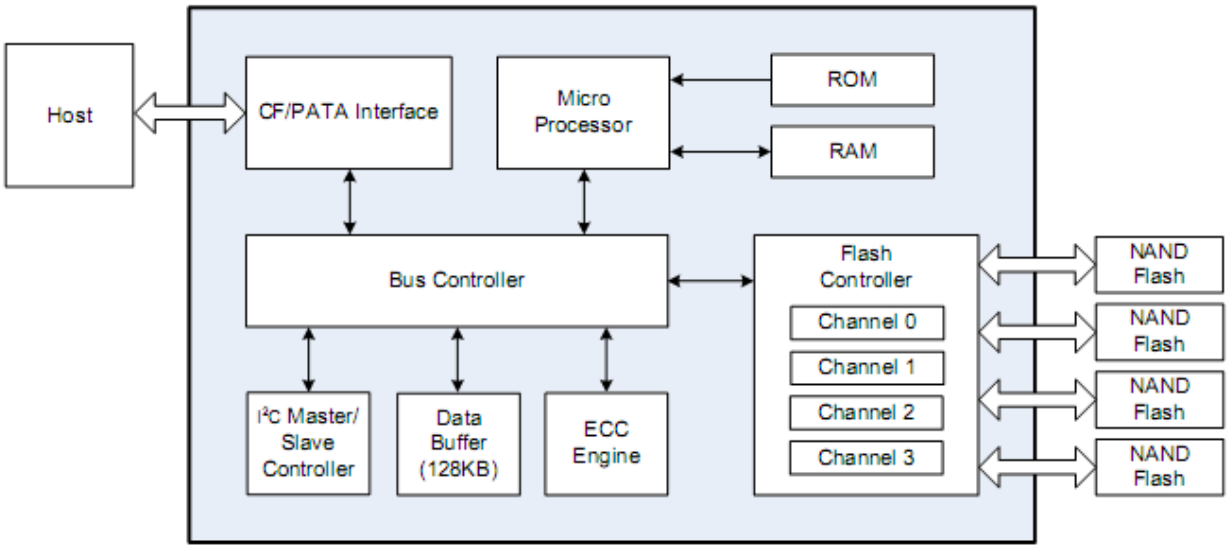


Figure 2-1 Functional Block Diagram

3. Pin Assignments

Table 3-1 lists the pin assignments with respective signal names for the 50-pin configuration. A "#" suffix indicates the active low signal. The pin type can be input, output or input/output.

Table 3-1 Pin Assignments

Pin No.	Memory card mode		I/O card mode		True IDE mode	
	Signal name	Pin I/O type	Signal name	Pin I/O type	Signal name	Pin I/O type
1	GND	-	GND	-	GND	-
2	D3	I/O	D3	I/O	D3	I/O
3	D4	I/O	D4	I/O	D4	I/O
4	D5	I/O	D5	I/O	D5	I/O
5	D6	I/O	D6	I/O	D6	I/O
6	D7	I/O	D7	I/O	D7	I/O
7	#CE1	I	#CE1	I	#CS0	I
8	A10	I	A10	I	A10[1]	I
9	#OE	I	#OE	I	#ATA SEL	I
10	A9	I	A9	I	A9[1]	I
11	A8	I	A8	I	A8[1]	I
12	A7	I	A7	I	A7[1]	I
13	VCC	-	VCC	-	VCC	-
14	A6	I	A6	I	A6[1]	I
15	A5	I	A5	I	A5[1]	I
16	A4	I	A4	I	A4[1]	I
17	A3	I	A3	I	A3[1]	I
18	A2	I	A2	I	A2	I
19	A1	I	A1	I	A1	I
20	A0	I	A0	I	A0	I
21	D0	I/O	D0	I/O	D0	I/O
22	D1	I/O	D1	I/O	D1	I/O
23	D2	I/O	D2	I/O	D2	I/O
24	WP	O	#IOIS16	O	#IOCS16	O
25	#CD2	O	#CD2	O	#CD2	O
26	#CD1	O	#CD1	O	#CD1	O
27	D11	I/O	D11	I/O	D11	I/O
28	D12	I/O	D12	I/O	D12	I/O
29	D13	I/O	D13	I/O	D13	I/O
30	D14	I/O	D14	I/O	D14	I/O
31	D15	I/O	D15	I/O	D15	I/O
32	#CE2	I	#CE2	I	#CS1	I
33	#VS1	O	#VS1	O	#VS1	O
34	#IORD	I	#IORD	I	#IORD	I
35	#IOWR	I	#IOWR	I	#IOWR	I
36	#WE	I	#WE	I	#WE	I
37	RDY/-BSY	O	#IREQ	O	INTRQ	O
38	VCC	-	VCC	-	VCC	-
39	#CSEL	I	#CSEL	I	#CSEL	I
40	#VS2	O	#VS2	O	#VS2	O
41	RESET	I	RESET	I	#RESET	I
42	#WAIT	O	#WAIT	O	IORDY	O
43	#INPACK	O	#INPACK	O	DMARQ[2]	O
44	#REG	I	#REG	I	DMACK[2]	I
45	BVD2	O	#SPKR	O	#DASP	I/O
46	BVD1	O	#STSCHG	O	#PDIAG	I/O

Pin No.	Memory card mode		I/O card mode		True IDE mode	
	Signal name	Pin I/O type	Signal name	Pin I/O type	Signal name	Pin I/O type
47	D8	I/O	D8	I/O	D8	I/O
48	D9	I/O	D9	I/O	D9	I/O
49	D10	I/O	D10	I/O	D10	I/O
50	GND	-	GND	-	GND	-

1. The signal should be grounded by the host.
2. Connection required when UDMA is in use.

4. Product Specifications

4.1 Capacity

Capacity specification of the Compact Flash Card series (CFC) is available as shown in Table 4-1. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

Table 4-1 Capacity Specifications

Capacity	Total bytes[1]	Cylinders	Heads	Sectors	Max LBA
8 GB	8,195,604,480	15,880	16	63	16,007,040
16 GB	16,391,340,032	16,383	16	63	32,014,336
32 GB	32,019,316,736	16,383	16	63	62,537,728
64 GB	64,030,244,864	16,383	16	63	125,059,072
128 GB	128,043,712,512	16,383	16	63	250,085,376

*Display of total bytes varies from file systems, which means not all of the bytes can be used for storage.
**Notes: 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.
LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

4.2 Performance

Performances of the CF cards are listed in Table 4-2.

Table 4-2 Performance Specifications

Capacity / Performance	8 GB	16 GB	32 GB	64 GB	128 GB
Sequential Read* (MB/s)	50	90	110	95	105
Sequential Write* (MB/s)	23	42	42	60	65

Note:
Results may differ from various flash configurations or host system setting.
*Sequential performance is based on CrystalDiskMark 5.2.1 with file size 1,000MB.

4.3 Environmental Specifications

Environmental specifications of the Compact Flash Card series (CFC) are shown in Table 4-3.

Table 4-3 Environmental Specifications

Environment		Specifications
Temperature	Operating	0°C to 70°C (Standard); -40°C to 85°C (Wide)
	Storage	-40°C to 100°C
Vibration (Non-Operation)		Sine wave : 10~2000Hz, 15G (X, Y, Z axes)
Shock (Non-Operation)		Half sine wave 1,500G (X, Y, Z ; All 6 axes)

4.4 Certification and Compliance

The CompactFlash card complies with the following global standards:

- CE
- FCC
- Halogen-free
- EMC
- RoHS Recast (2011/65/EU)

5. Software Interface

5.1 CF-ATA Command Set

Table 5-1 summarizes the CF-ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 5-1 CFC-ATA Command Set

Command Set	Command	Code	Protocol
CFA Feature Set	Request Sense	03h	Non-data
	Write Sectors Without Erase	38h	PIO data-out
	Erase Sectors	C0h	Non-data
	Write Multiple Without Erase	CDh	PIO data-out
	Translate Sector	87h	PIO data-in
	Set Features Enable/Disable 8-bit Transfer	Efh	Non-data
General Feature Set	Execute Drive Diagnostic	90h	Device diagnostic
	Flush Cache	E7h	Non-data
	Identify Device	Ech	PIO data-in
	Read DMA	C8h	DMA
	Read Multiple	C4h	PIO data-in
	Read Sector(s)	20h or 21h	PIO data-in
	Read Verify Sector(s)	40h or 41h	Non-data
	Set Feature	Efh	Non-data
	Set Multiple Mode	C6h	Non-data
	Write DMA	Cah	DMA
	Write Multiple	C5h	PIO data-out
	Write Sector(s)	30h or 31h	PIO data-out
	NOP	00h	Non-data
	Read Buffer	E4h	PIO data-in
	Write Buffer	E8h	PIO data-out
	Set Feature	Efh	Non-data
Power Management Feature Set	Check Power Mode	E5h or 98h	Non-data
	Idle	E3h or 97h	Non-data
	Idle Immediate	E1h or 95h	Non-data
	Sleep	E6h or 99h	Non-data
	Standby	E2h or 96h	Non-data
	Standby Immediate	E0h or 94h	Non-data

Command Set	Command	Code	Protocol
Security Mode Feature Set	Security Set Password	F1h	PIO data-out
	Security Unlock	F2h	PIO data-out
	Security Erase Prepare	F3h	Non-data
	Security Erase Unit	F4h	PIO data-out
	Security Freeze Lock	F5h	Non-data
	Security Disable Password	F6h	PIO data-out
SMART Feature Set	SMART Disable Operations	B0h	Non-data
	SMART Enable/Disable Autosave	B0h	Non-data
	SMART Enable Operations	B0h	Non-data
	SMART Return Status	B0h	Non-data
	SMART Execute Off-line Immediate	B0h	Non-data
	SMART Read Data	B0h	PIO data-in
Host Protected Area Feature Set	Read Native Max Address	F8h	Non-data
	Set Max Address	F9h	Non-data
	Set Max Set Password	F9h	PIO data-out
	Set Max Lock	F9h	Non-data
	Set Max Freeze Lock	F9h	Non-data
	Set Max Unlock	F9h	PIO data-out
Others	Format Track	50h	PIO data-out
	Initialize Drive Parameters	91h	Non-data
	Recalibrate	1Xh	Non-data
	Seek	7Xh	Non-data
	Wear Level	F5h	Non-data
	Write Verify	3Ch	PIO data-out
48-bit Address Feature Set	Read Sector Ext	24h	PIO data-in
	Read DMA Ext	25h	DMA
	Read Multiple Ext	29h	PIO data-in
	Write Sector Ext	34h	PIO data-out
	Write DMA Ext	35h	DMA
	Read Verify Sector Ext	42h	Non-data
	Write Multiple FUA Ext	Ceh	PIO data-out
	Flush Cache Ext	Eah	Non-data

6. Electrical Specifications

6.1 Operating Voltage

Table 6-1 lists the supply voltage for CompactFlash card.

Table 6-1 Operating Range

Item	Range
Supply Voltage	3.3V ± 5% (3.135-3.465V)
	5V ± 5% (4.75-5.25V)

6.2 Power Consumption

Table 6-2 and 6-3 list the power consumption for CompactFlash card.

Table 6-2 Power Consumption@3.3.V

Capacity / Mode	8 GB	16 GB	32 GB	64 GB	128 GB
Active (mA)	155	225	255	245	260
Standby (mA)	10	10	10	10	15

Table 6-3 Power Consumption@5.V

Capacity / Mode	8 GB	16 GB	32 GB	64 GB	128 GB
Active (mA)	160	240	265	255	260
Standby (mA)	10	10	10	10	15

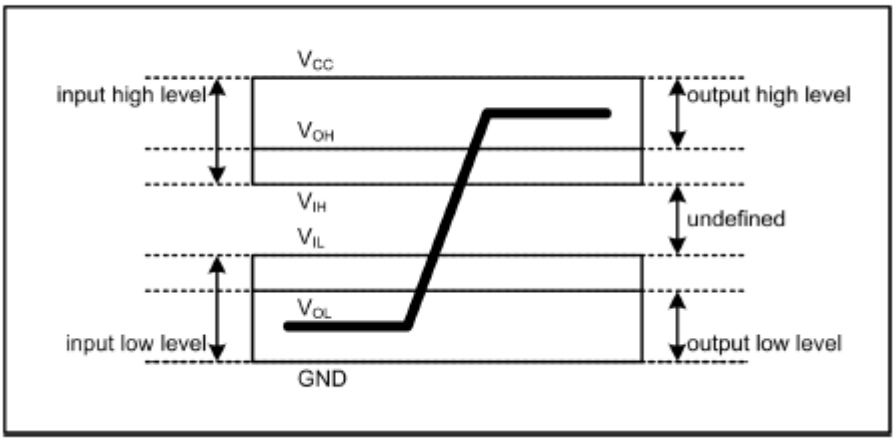
Note:
*All values are typical and may vary depending on flash configurations or host system settings.
**Active power is an average power measurement performed using CrystalDiskMark with 128KB sequential read/write transfers.

6.3 AC/DC Characteristics

The following section provides general AC/DC characteristics of this CompactFlash card.

6.3.1 General DC Characteristics

Definitions of V_{IH}, V_{CC}, V_{OH}, V_{OL}



- **DC characteristics for host interface (Vcc = 3.3V/5V)**

Parameter	Symbol	Minimum	Maximum	Unit	Remark
Supply Voltage 5V	Vcc	4.5	5.5	V	
Supply voltage 3.3V	Vcc	2.97	3.63	V	
High Level Output Voltage	VOH	2.5		V	
Low Level Output Voltage	VOL		0.4	V	
High Level Input Voltage	VIH	2.4		V	Non-Schmitt trigger
		2.05		V	Schmitt trigger
Low Level Input Voltage	VIL		0.6	V	Non-Schmitt trigger
			1.25	V	Schmitt trigger
Pull-up Resistance	RPU	52.7	141	kOhm	
Pull-down Resistance	RPD	47.5	172	kOhm	

- **General DC characteristics**

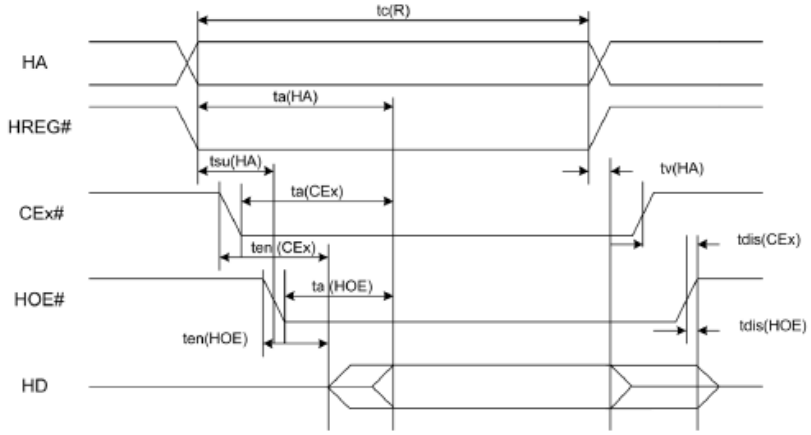
Parameter	Symbol	Minimum	Maximum	Unit	Remark
Supply Voltage	Vcc	2.7	3.6	V	
High Level Output Voltage	VOH	2.4		V	
Low Level Output Voltage	VOL		0.4	V	
High Level Input Voltage	VIH	2.0		V	Non-Schmitt trigger
		1.4	2.0	V	Schmitt trigger
Low Level Input Voltage	VIL		0.8	V	Non-Schmitt trigger
			1.2	V	Schmitt trigger
Pull-up Resistance	RPU	40		kOhm	
Pull-down Resistance	RPD	40		kOhm	

6.3.2 General AC Characteristics

- **Attribute Memory Read Timing**

Item	Symbol	Min. (ns)	Max. (ns)
Read Cycle Time	tc (R)	300	
Address Access Time	ta (HA)		300
Card Enable Access Time	ta (CEx)		300
Output Enable Access Time	ta (HOE)		150
Output Disable Time from CEx#	tdis (CEx)		100
Output Disable Time from HOE#	tdis (HOE)		100
Address Setup Time	tsu (HA)	30	
Output Enable Time from CEx#	ten (CEx)	5	
Output Enable Time from HOE#	ten (HOE)	5	
Data Valid from Address Change	tv (HA)	0	

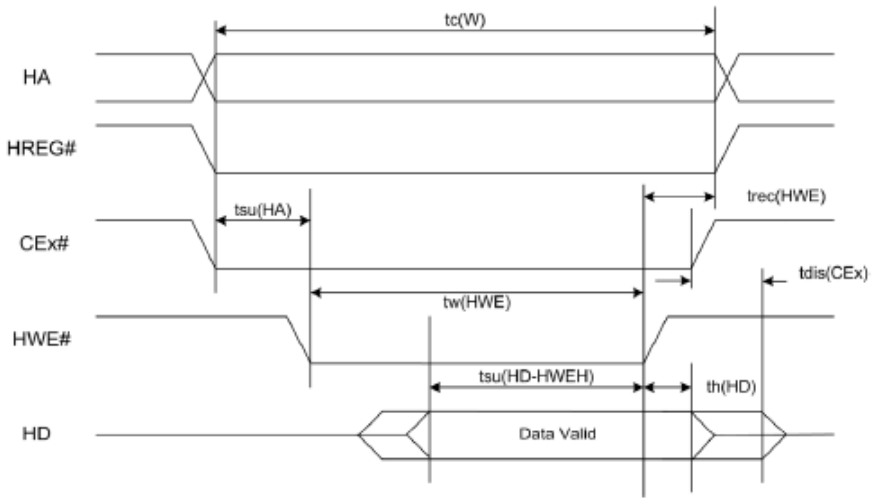
Notes: all time intervals are in nanoseconds. HD refers to the data provided by the CompactFlash card to the system. The CEx# signal or both of the HOE# and the HWE# signal are de-asserted between consecutive cycle operations.



- **Attribute Memory Write Timing**

Item	Symbol	Min. (ns)	Max. (ns)
Write Cycle Time	tc (W)	250	
Write Pulse Width	tw (HWE)	150	
Address setup Time	tsu (HA)	30	
Write Recovery Time	trec (HWE)	30	
Data Setup Time for HWE#	tsu (HD-HWEH)	80	
Data Hold Time	th (HD)	30	

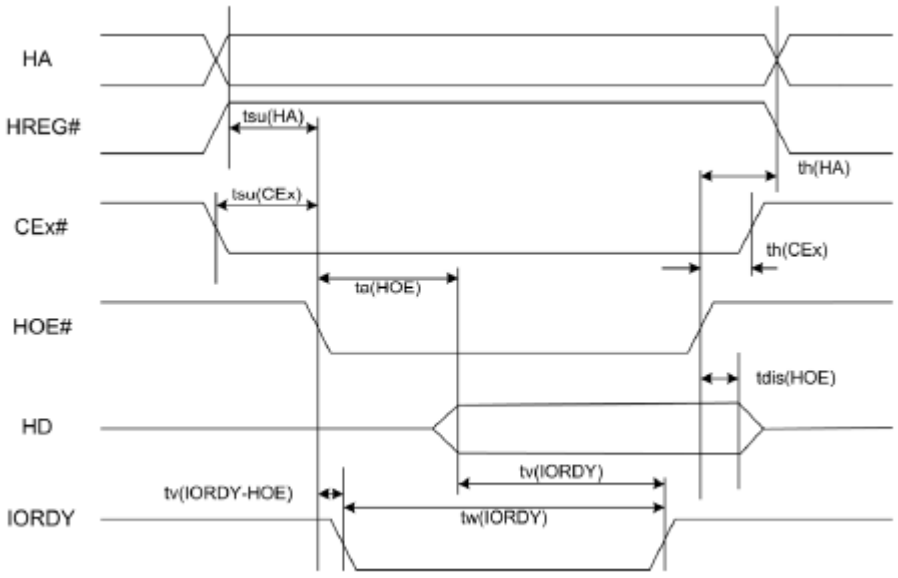
Notes: all time intervals are in nanoseconds. HD refers to the data provided by the CompactFlash card to the system.



- **Common Memory Read Timing**

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
Output Enable Access Time	ta (HOE)		125		60		50		45
Output Disable Time from HOE#	tdis (HOE)		100		60		50		45
Address Setup Time	tsu (HA)	30		15		10		10	
Address Hold Time	th (HA)	20		15		15		10	
CEx# Setup before HOE#	tsu (CEx)	5		5		5		5	
CEx# Hold following HOE#	th (CEx)	20		15		15		10	
Wait Delay falling from HOE#	tv (IORDY-HOE)		35		35		35		Na
Data Setup for Wait Release	tv (IORDY)		0		0		0		Na
Wait Width Time	tw (IORDY)		350		350		350		Na

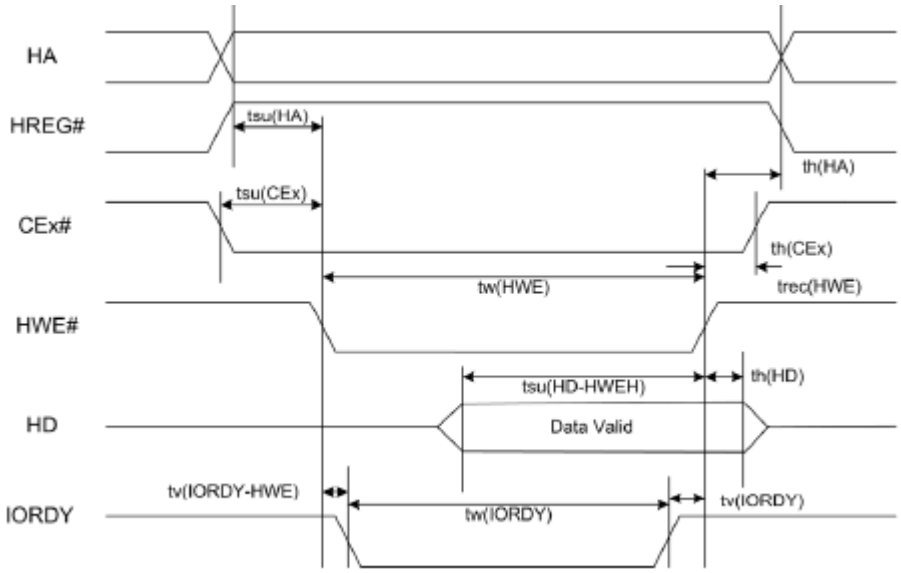
Note: IORDY is not supported in this 80 ns mode. The maximum load on IORDY is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All time intervals are in nanoseconds. HD refers to the data provided by the CompactFlash card to the system. The IORDY signal can be ignored when the HOE# cycle-to-cycle time is greater than the Wait Width Time. The Max Wait Width Time can be determined from the Card Information Structure (CIS). Although adhering to the PCM-CIA specification, the Wait Width Time is intentionally designed to be lower in this specification.



- **Common Memory Write Timing**

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
Data Setup before HWE#	tsu (HD-HWEH)	80		50		40		30	
Data Hold following HWE#	th (HD)	30		15		10		10	
HWE# Pulse Width	tw (HWE)	150		70		60		55	
Address Setup Time	tsu (HA)	30		15		10		10	
CEx# Setup before HWE#	tsu (CEx)	5		5		5		5	
Write Recovery Time	trec (HWE)	30		15		15		15	
Address Hold Time	th (HA)	20		15		15		15	
CEx# Hold following HWE#	th (CEx)	20		15		15		10	
Wait Delay falling from HWE#	tv (IIORDY-HWE)		35		35		35		Na
HWE# High from Wait Release	tv (IORDY)	0		0		0		Na	
Wait Width Time	tw (IORDY)		350		350		350		Na

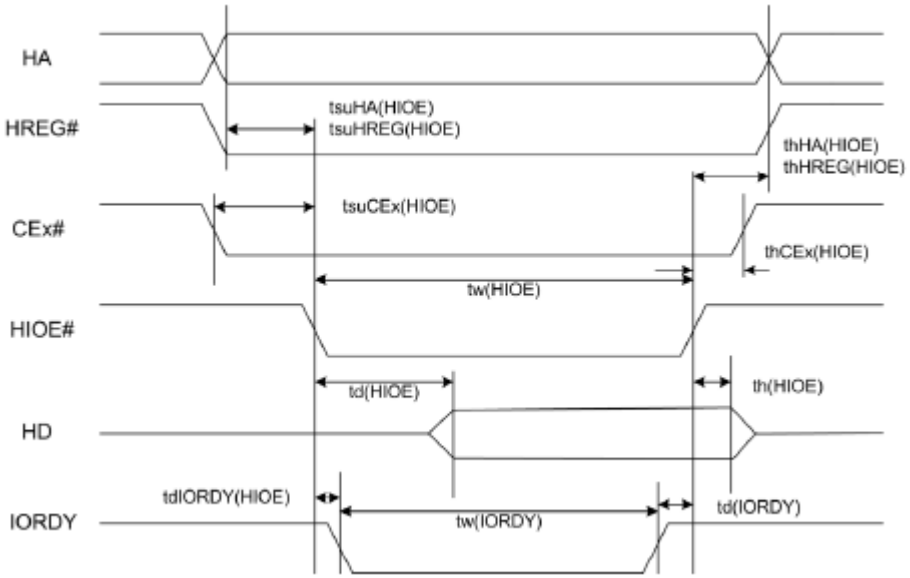
Note: IORDY is not supported in this 80 ns mode. The maximum load on IORDY is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All time intervals are in nanoseconds. HD refers to the data provided by the CompactFlash card to the system. The IORDY signal can be ignored when the HWE# cycle-to-cycle time is greater than the Wait Width Time. The Max Wait Width Time can be determined from the Card Information Structure (CIS). Although adhering to the PCM-CIA specification, the Wait Width Time is intentionally designed to be lower in this specification.



- **I/O Read Timing**

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
Data Delay after HIOE#	td (HIOE)		100		50		50		45
Data Hold following HIOE#	th (HIOE)	0		5		5		5	
HIOE# Width Time	tw (HIOE)	165		70		65		55	
Address Setup before HIOE#	tsuHA (HIOE)	70		25		25		15	
Address Hold following HIOE#	thHA (HIOE)	20		10		10		10	
CEx# Setup before HIOE#	tsuCEx (HIOE)	5		5		5		5	
CEx# Hold following HIOE#	thCEx (HIOE)	20		10		10		10	
HREG# Setup before HIOE#	tsuHREG (HIOE)	5		5		5		5	
HREG# Hold following HIOE#	thHREG (HIOE)	0		0		0		0	
Wait Delay falling from HIOE#	tdIORDY (HIOE)		35		35		35		Na
Data Delay from Wait Rising	td (IORDY)		0		0		0		na
Wait Width Time	tw (IORDY)		350		350		350		Na

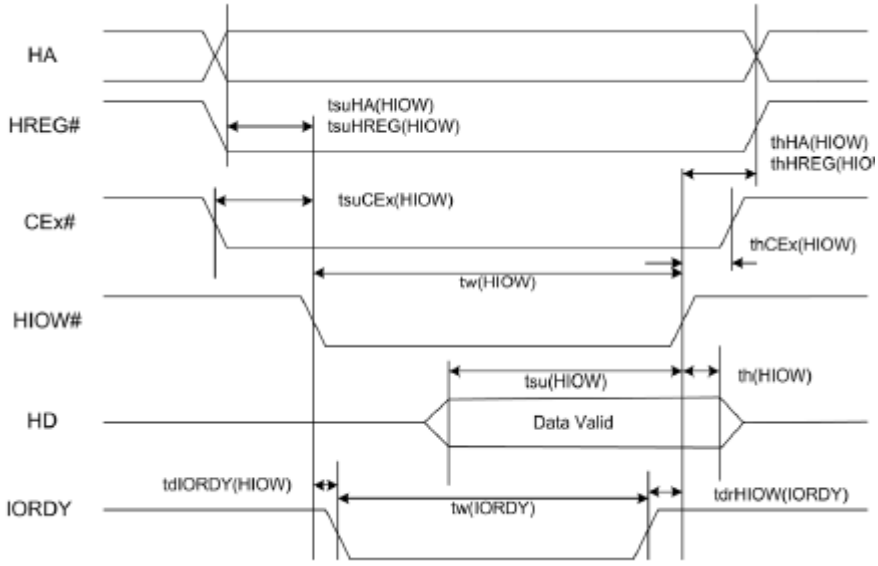
Note: IORDY is not supported in this 80 ns mode. Maximum load on IORDY is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All time intervals are in nanoseconds. Although minimum time from IORDY high to HIOE# high is 0 nsec, the minimum HIOE# width is still met. HD refers to data provided by the CompactFlash Card to the system. Although following PCMCIA specification, the Wait Width Time is intentionally lower in this specification.



- **I/O Write Timing**

Cycle Time Mode		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
Data Setup before HIOW#	tsu (HIOW)	60		20		20		15	
Data Hold following HIOW#	th (HIOW)	30		10		5		5	
HIOW# Width Time	tw (HIOW)	165		70		65		65	
Address Setup before HIOW#	tsuHA (HIOW)	70		25		25		15	
Address Hold following HIOW#	thHA (HIOW)	20		20		10		10	
CEx# Setup before HIOW#	tsuCEx (HIOW)	5		5		5		5	
CEx# Hold following HIOW#	thCEx (HIOW)	20		20		10		10	
HREG# Setup before HIOW#	tsuHREG (HIOW)	5		5		5		5	
HREG# Hold following HIOW#	thHREG (HIOW)	0		0		0		0	
Wait Delay falling from HIOW#	tdIORDY (HIOW)		35		35		35		na
HIOW# high from Wait High	tdHIOW (IORDY)	0		0		0		na	
Wait Width Time	tw (IORDY)		350		350		350		na

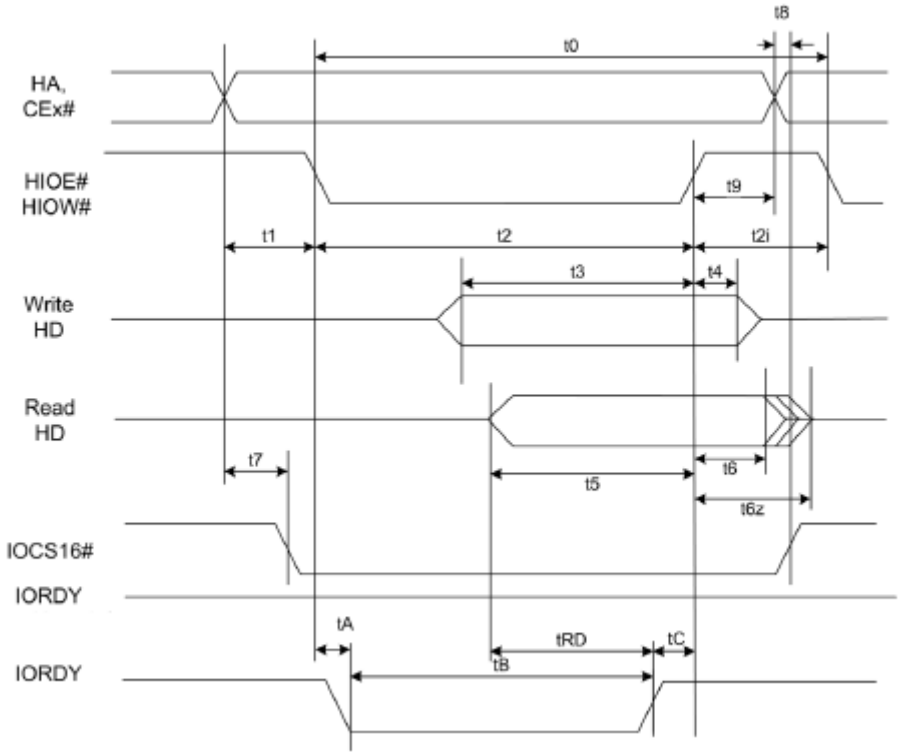
Note: IORDY is not supported in this 80 ns mode. The maximum load on IORDY is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All time intervals are in nanoseconds. Although minimum time from IORDY high to HIOW# high is 0 nsec, the minimum HIOW# width is still met. HD refers to data provided by the CompactFlash Card to the system.



- **True IDE PIO Mode Read/Write Timing**

Item	Symbol	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
Cycle Time (Min.)	t0	600	383	240	180	120	100	80
Address Valid to HIOE# / HIOW# Setup (Min.)	t1	70	50	30	30	25	15	10
HIOE# / HIOW# (Min.)	t2	165	125	100	80	70	65	55
HIOE# / HIOW# (Min.) Register (8-bit)	t2	290	290	290	80	70	65	55
HIOE# / HIOW# Recovery Time (Min.)	t2i	-	-	-	70	25	25	20
HIOW# Data Setup (Min.)	t3	60	45	30	30	20	20	15
HIOW# Data Hold (Min.)	t4	30	20	15	10	10	5	5
HIOE# Data Setup (Min.)	t5	50	35	20	20	20	15	10
HIOE# Data Hold (Min.)	t6	5	5	5	5	5	5	5
HIOE# Data Tristate (Max.)	t6Z	30	30	30	30	30	20	20
Address Valid to IOCS16# Assertion (Max.)	t7	90	50	40	n/a	n/a	n/a	n/a
Address Valid to IOCS16# released (Max.)	t8	60	45	30	n/a	n/a	n/a	n/a
HIOE# / HIOW# to Address Valid Hold	t9	20	15	10	10	10	10	10
Read Data Valid to IORDY Active (Min.), if IORDY initially low after tA	tRD	0	0	0	0	0	0	0
IORDY Setup Time	tA	35	35	35	35	35	Na	Na
IORDY Pulse Width (Max.)	tB	1250	1250	1250	1250	1250	Na	Na
IORDY Assertion to Release (Max.)	tC	5	5	5	5	5	Na	Na

*All timing intervals are measured in nanoseconds. The maximum load on IOCS16# is 1 LSTTL with a 50 pF (40 pF below 120 nsec cycle time) total load. All time intervals are in nanoseconds. Although minimum time from IORDY high to HIOE# high is 0 nsec, the minimum HIOE# width is still met.
Where t0 denotes the minimum total cycle time; t2 represents the minimum command active time; t2i is the minimum command recovery time or command inactive time. Actual cycle time equals to the sum of actual command active time and actual command inactive time. The three timing requirements for t0, t2, and t2i are met. The minimum total cycle time requirement is greater than the sum of t2 and t2i, implying that a host implementation can extend either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device identity data. A CompactFlash card implementation supports any legal host implementation.
The delay originates from HIOW# or HIOW# activation until the state of IORDY is first sampled. If IORDY is inactive, the host waits until IORDY is active before the PIO cycle is completed. When the CompactFlash Card is not driving IORDY, which is negated at tA after HIOE# or HIOW# activation, then t5 is met and tRD is inapplicable. When the CompactFlash Card is driving IORDY, which is negated at the time tA after HIOE# or HIOW# activation, then tRD is met and t5 is inapplicable.
Both t7 and t8 apply to modes 0, 1, and 2 only. For other modes, the signal is invalid.
IORDY is not supported in this mode.

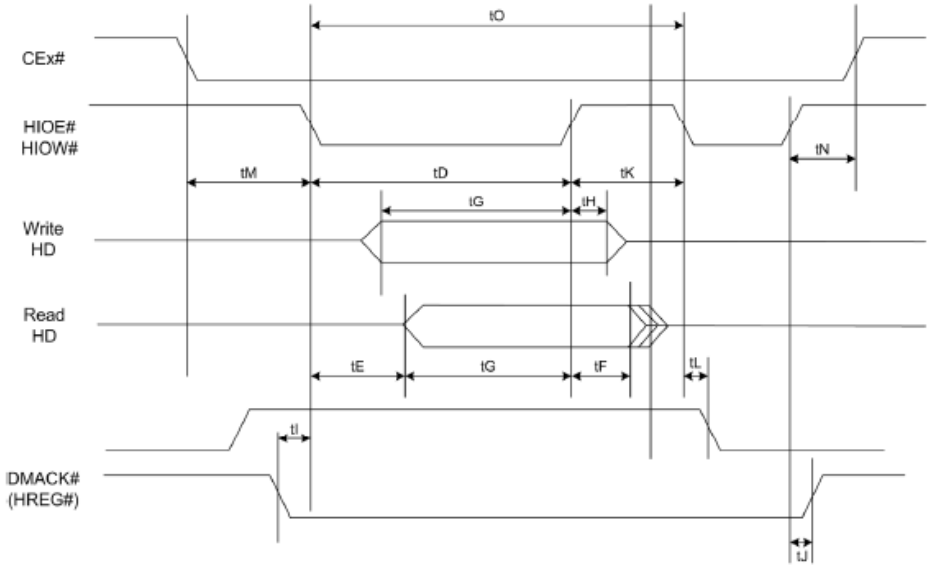


Device address comprises CE1#, CE2#, and HA[2:0]
Data comprises HD[15:0] (16-bit) or HD[7:0] (8-bit)
IOCS16# is shown for PIO modes 0, 1, and 2. For other modes, the signal is ignored.
The negation of IORDY by the device is used to lengthen the PIO cycle. Whether the cycle is to be extended is determined by the host after tA from the assertion of HIOE# or HIOW#. The assertion and negation of IORDY is described in the following cases. First, the device never negates IORDY, so no wait is generated. Secondly, device drives IORDY low before tA. Thus, wait is generated. The cycle is completed after IORDY is re-asserted. For cycles in which a wait is generated and HIOE# is asserted, the device places read data on D15-D00 for tRD before IORDY is asserted.

- **True IDE Multiword DMA Mode Read/Write Timing**

Item	Symbol	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
Cycle Time (Min.)	tO	480	150	120	100	80
HIOE#/HIOW# asserted width (Min.)	tD	215	80	70	65	65
HIOE# data access (Max.)	tE	150	60	50	50	45
HIOE# data hold (Min.)	tF	5	5	5	5	5
HIOE# / HIOW# data setup (Min.)	tG	100	30	20	15	10
HIOW# data hold (Min.)	tH	20	15	10	5	5
HREG# to HIOE#/HIOW# setup (Min.)	tI	0	0	0	0	0
HIOE#/HIOW# to HREG# hold (Min.)	tJ	20	5	5	5	5
HIOE# negated width (Min.)	tKR	50	50	25	25	20
HIOW# negated width (Min.)	tKW	215	50	25	25	20
HIOE# to DMARQ delay (Max.)	tLR	120	40	35	35	35
HIOW# to DMARQ delay (Max.)	tLW	40	40	35	35	35
CEx# valid to HIOE#/HIOW#	tM	50	30	25	10	5
CEx# hold	tN	15	10	10	10	10

Note: Where t0 is the minimum total cycle time and tD is minimum command active time, whereas tKR and tKW are minimum command recovery time or command inactive time for input and output cycles, respectively. Actual cycle time equals to the sum of actual command active time and actual command inactive time. The three timing requirements of t0, for instance, tD, tKR, and tKW, must be met. The minimum total cycle time requirement exceeds the sum of tD and tKR or tKW for input and output cycles respectively, implying that a host implementation can extend either or both tD and tKR or tKW as deemed necessary to ensure that t0 equals or exceeds the value reported in the device identify data. A CompactFlash card implementation supports any legal host, appropriate host implementation.



If a card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ during the time from the start of a DMA transfer cycle (to suspend DMA transfers in progress) and re-assertion of the signal at a relatively later time to continue DMA transfer operations. The host may negate this signal to suspend the DMA transfer in progress.

- **Ultra DMA Signal Usage in Each Interface Mode**

Signal	Type	Non-UDMA Memory Mode	PC Card Memory Mode UDMA	PC Card IO Mode UDMA	True IDE Mode UDMA
DMARQ	Output	(INPACK#)	DMARQ#	DMARQ#	DMARQ
HREG#	Input	(REG#)	DMACK#	DMACK	DMACK#
HIOW#	Input	(IOWR#)	STOP[1]	STOP[1]	STOP[1]
HIOE#	Input	(IORD#)	HDMARDY#(R)[1,2] HSTROBE(W)[1,3,4]	HDMARDY#(R)[1,2] HSTROBE(W)[1,3,4]	HDMARDY#(R)[1,2] HSTROBE(W)[1,3,4]
IORDY	Output	(WAIT#)	DDMARDY#(W)[1,3] DSTROBE(R)[1,2,4]	DDMARDY#(W)[1,3] DSTROBE(R)[1,2,4]	DDMARDY#(W)[1,3] DSTROBE(R)[1,2,4]
HD[15:0]	Bidir	(D[15:00])	D[15:00]	D[15:00]	D[15:00]
HA[10:0]	Input	(A[10:00])	A[10:00]	A[10:00]	A[02:00][5]
CSEL#	Input	(CESL#)	CSEL#	CSEL#	CSEL#
HIRQ	Output	(READY)	READY	INTRQ#	INTRQ
CE1# CE2#	Input	(CE1#) (CE2#)	CE1# CE2#	CE1# CE2#	CS0# CS1#

1. UDMA interpretation of this signal is valid only during an Ultra DMA data burst.
2. UDMA interpretation of this signal is valid only during an Ultra DMA data burst during a DMA Read command.
3. UDMA interpretation of this signal is valid only during an Ultra DMA data burst during a DMA Write command.
4. HSTROBE and DSTROBE signals are active on both rising and falling edges.
5. Address lines 03-10 are not used in the True IDE mode.

- **Ultra DMA Data Burst Timing Requirements**

Parameter	UDMA Mode 0	UDMA Mode 1	UDMA Mode 2	UDMA Mode 3	UDMA Mode 4	UDMA Mode 5	Measure Location
$t_{2CYCTYP}$	240	160	120	90	60	40	Sender
t_{CYC}	112	73	54	39	25	16.8	See note
t_{2CYC}	230	153	115	86	57	38	Sender
t_{DS}	15.0	10.0	7.0	7.0	5.0	4.0	Recipient
t_{DH}	5.0	5.0	5.0	5.0	5.0	4.6	Recipient
t_{DVS}	70.0	48.0	31.0	20.0	6.7	4.8	Sender
t_{DVH}	6.2	6.2	6.2	6.2	6.2	4.8	Sender
t_{CS}	15.0	10.0	7.0	7.0	5.0	5.0	Device
t_{CH}	5.0	5.0	5.0	5.0	5.0	5.0	Device
t_{CVS}	70.0	48.0	31.0	20.0	6.7	10.0	Host
t_{CVH}	6.2	6.2	6.2	6.2	6.2	10.0	Host
t_{ZFS}	0	0	0	0	0	35	Device
t_{DZFS}	70.0	48.0	31.0	20.0	6.7	25	Sender
t_{FS}	230	200	170	130	120	90	Device
t_{LI}	0 - 150	0 - 150	0 - 150	0 - 100	0 - 100	0 - 75	See note
t_{MLI}	20	20	20	20	20	20	Host
t_{UI}	0	0	0	0	0	0	Host
t_{AZ}	10	10	10	10	10	10	See note
t_{ZAH}	20	20	20	20	20	20	Host
t_{ZAD}	0	0	0	0	0	0	Device
t_{ENV}	20 - 70	20 - 70	20 – 70	20 - 55	20 - 55	20 - 50	Host
t_{RFS}	75	70	60	60	60	50	Sender
t_{RP}	160	125	100	100	100	85	Recipient
t_{IORDYZ}	20	20	20	20	20	20	Device
t_{ZIORDY}	0	0	0	0	0	0	Device
t_{ACK}	20	20	20	20	20	20	Host
t_{SS}	50	50	50	50	50	50	Sender

Notes:
All timing are in nanoseconds and all timing measurement switching points (low to high and high to low) are taken at 1.5V. All signal transitions for a timing parameter are determined at the connector specified in the measurement location column. Parameter t_{CYC} is determined at the connector of the recipient farthest from the sender, while parameter t_{LI} is determined at the connector of a sender or recipient responding to an incoming transition from the recipient or sender, respectively. Both incoming signal and outgoing response are determined at the same connector. Parameter t_{AZ} is determined at the connector of a sender or recipient driving the bus, and must release the bus to allow for a bus turnaround.

- **Ultra DMA Data Burst Timing Descriptions**

Parameter	Description & Comment	Note
$t_{2CYCTYP}$	Typical sustained average two cycle time	
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	
t_{DS}	Data setup time at recipient (from data valid until STROBE edge)	2, 5
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid)	2,5
t_{DVS}	Data valid setup at sender (from data valid until STROBE edge)	3
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	3
t_{CS}	CRC word setup time at device	2
t_{CH}	CRC word hold time at device	2
t_{CVS}	CRC word valid setup time at host (from CRC valid until DMACK(#) negation)	3
t_{CVH}	CRC word valid hold time at sender (from DMACK(#) negation until CRC may become invalid)	3
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing	
t_{DZFS}	Time from data output released-to-driving until the first transition of critical timing)	
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	
t_{LI}	Limited interlock time	1
t_{MLI}	Interlock time with minimum	1
t_{UI}	Unlimited interlock time	1
t_{AZ}	Maximum time allowed for output drives to release (from asserted or negated)	
t_{ZAH}	Minimum delay time required for output	
t_{ZAD}	Drivers to assert or negate (from released)	
t_{ENV}	Envelope time (from DMACK(#)) to STOP and HDMARDY# during data in burst initiation and from DMACK(#) to STOP during data out burst initiation	
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY#)	
t_{RP}	Ready-to-pause time (that recipient shall wait to pause after negating DMARDY#)	
t_{IORDYZ}	Maximum time before releasing IORDY	6
t_{ZIORDY}	Minimum time before driving IORDY	4, 6
t_{ACK}	Setup and hold times for DMACK(#) (before assertion or negation	
t_{SS}	Time from STROBE edge to negation of DMARQ(#) or assertion of STOP (when sender terminates a burst)	

Notes:
1. Parameters tUI, tMLI and tLI represent sender-to-recipient or recipient-to-sender interlocks, for instance, one agent (sender or recipient) is waiting for the other agent to respond with a signal before proceeding. Parameter tUI denotes an unlimited interlock that has no maximum time value; tMLI represents a limited time-out that has defined minimum; tLI is a limited time-out that has a defined maximum.

2. The 80-conductor cabling is required to meet setup (tDS, tCS) and hold (tDH, tCH) times in modes exceeding 2.
3. Timing for tDVS, tDVH, tCVS, and tCVH must be met for lumped capacitive loads of 15 and 40 pF at the connector where the data and STROBE signals have the same capacitive load value.
4. Fall all timing modes, parameter tZIORDY may be greater than tENV since the host has a pull up on IORDY giving it a known state when released.
5. Parameters tDS and tDH for mode 5 are defined for a recipient at the end of a cable only in a configuration that has a single device located at the cable end. This configuration can result in tDS, and tDH for mode 5 at the middle connector having minimum values of 3.0 and 3.9 nanoseconds respectively.
6. The parameters are only applied to True IDE mode operation.

● Ultra DMA Sender & Recipient IC Timing Requirements

Item	UDMA Mode 0 (ns)		UDMA Mode 1 (ns)		UDMA Mode 2 (ns)		UDMA Mode 3 (ns)		UDMA Mode 4 (ns)		UDMA Mode 5 (ns)	
	Min.	Max.	Min.	Max.	Min.	Min.	Max.	Max.	Min.	Max.	Min.	Max.
t_{DSIC}	14.7		9.7		6.8		6.8		4.8		2.3	
t_{DHIC}	4.8		4.8		4.8		4.8		4.8		2.8	
t_{DVSIC}	72.9		50.9		33.9		22.6		9.5		6.0	
t_{DVHIC}	9.0		9.0		9.0		9.0		9.0		6.0	
t_{DSIC}	Recipient IC data setup time (from data valid until STROBE edge)											
t_{DHIC}	Recipient IC data hold time (from STROBE edge until data may become invalid)											
t_{DVSIC}	Sender IC data valid setup time (from data valid until STROBE edge)											
t_{DVHIC}	Sender IC data valid hold time (from STROBE edge until data may become invalid)											

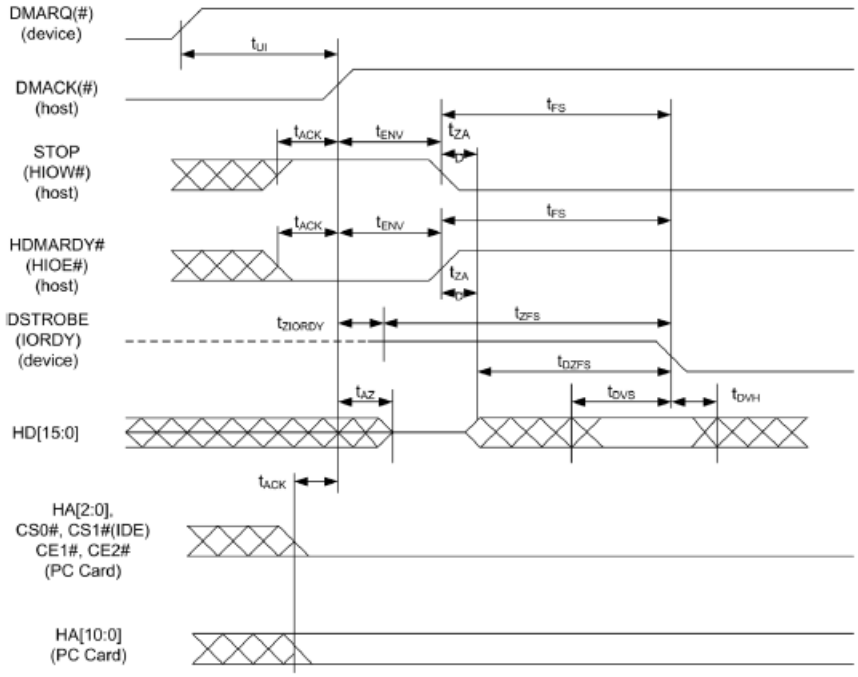
Note: all timing switching point measurements are taken at 1.5V. The correct data value is captured by the recipient given input data with a slew rate of 0.4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at tDSIC and tDHIC timing (measured at 1.5V). Parameters tDVSIC and tDVHIC must be met for lumped capacitive loads of 15 and 40 pF at the IC where all signals have the same capacitive load value. Noise that can couple onto the output signals from external sources is not included in these values.

● Ultra DMA AC Signal Requirements

Item	Symbol	Min. (V/ns)	Max. (V/ns)
Rising Edge Slew Rate for any signal	S_{RISE}		1.25
Falling Edge Slew Rate for any signal	S_{FALL}		1.25

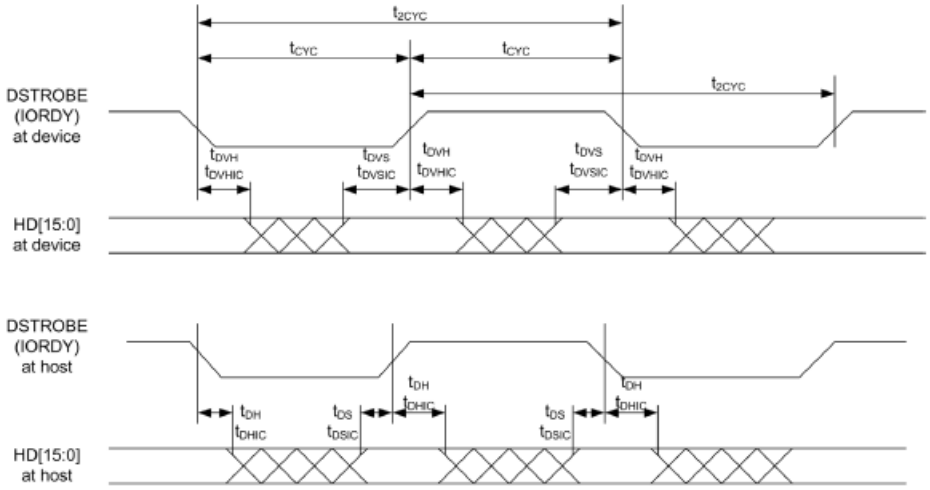
Notes:
1. The sender is tested while driving an 18-inch, 80-conductor cable with PVC insulation. The signal being tested must be cut at a test point such that it has no trace, cable, or recipient loading after the test point. All other signals must remain connected through to the recipient. The test point should be located between a sender's series termination resistor and within 0.5 inch or less from where the conductor exits the connector. If the test point is on a cable conductor rather than on the PCB, an adjacent ground conductor must also be cut within 0.5 inch or the connector.
2. The test load and test points should be soldered directly to the exposed source side connectors. The test loads consist of a 15 pF or a 40 pF, 5%, 0.08 inch by 0.05 inch surface mount or relatively smaller capacitor connected between the test point and ground. Slew rates are met for both capacitor values.
3. Measurements must be taken at the test point using a <1 pF, >100 Kohm, 1GHz probe and a 500 MHz oscilloscope. The average rate is measured from 20% ~ 80% of the settled VOH level with data transitions at least 120 nanoseconds apart. The settled VOH level must be measured as the average high output level under the defined test conditions from 100 nanoseconds after 80% of a rising edge until 20% of the subsequent falling edge.

- **Ultra DMA Data-in Burst Initiation Timing**



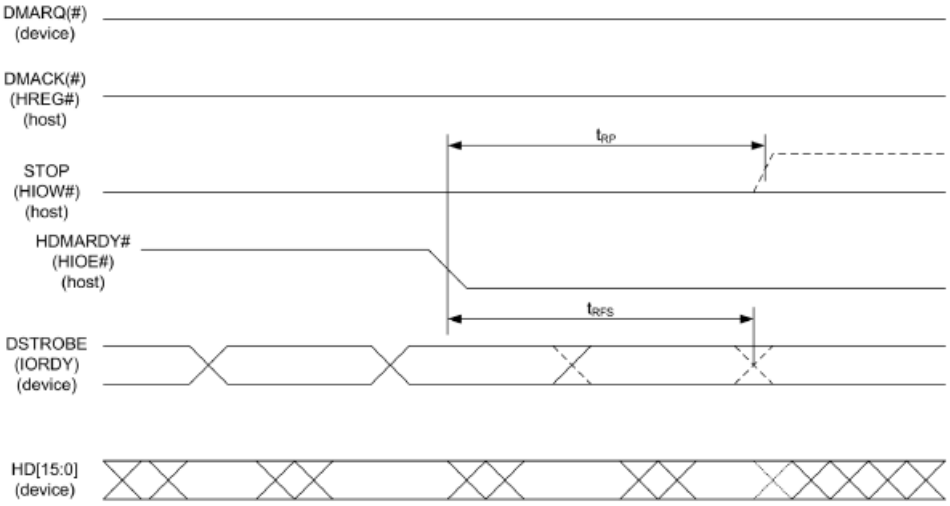
1. All waveforms in this diagram are shown with the asserted state high. Negative true signals are inverted on the bus relative to the diagram.
2. The definitions for the IORDY:DDMARDY#:DSTROBE, HIOE#: HDMARDY#: HSTROBE and HIOW#: STOP signal lines are not in effect until DMARQ(#) and DMACK(#) are asserted. Notably, HA[2:0], CS0# and CS1# are True IDE mode signal definitions, and HA[10:0], CE1# and CE2# are PC Card mode signals. The Bus polarity of DMACK(#) and DMARQ(#) is based on the active interface mode.

- **Sustained Ultra DMA Data-in Burst Timing**



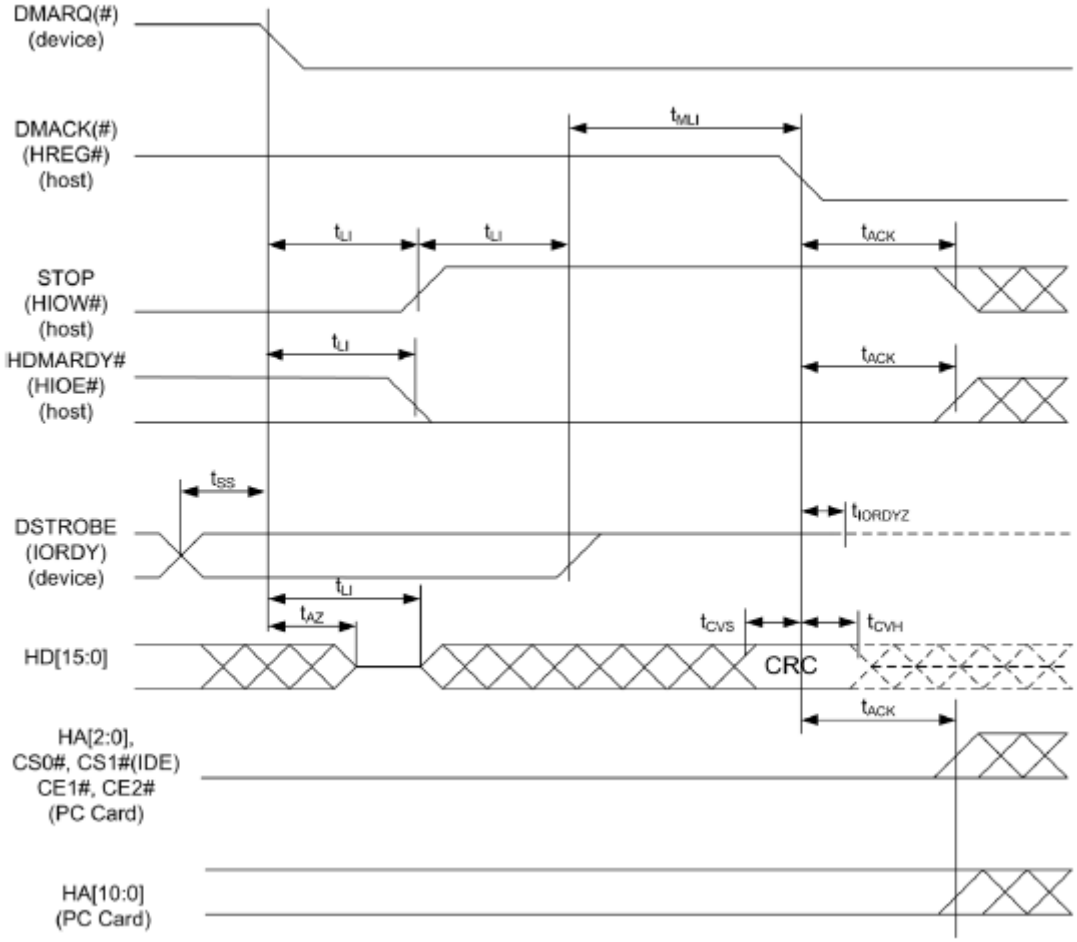
HD[15:0] and IORDY signals are shown at both the host and device to emphasize that neither cable settling time nor cable propagation delay allow data signals to be considered stable at the host until after they are driven by the device.

- **Ultra DMA Data-in Burst Host Pause Timing**



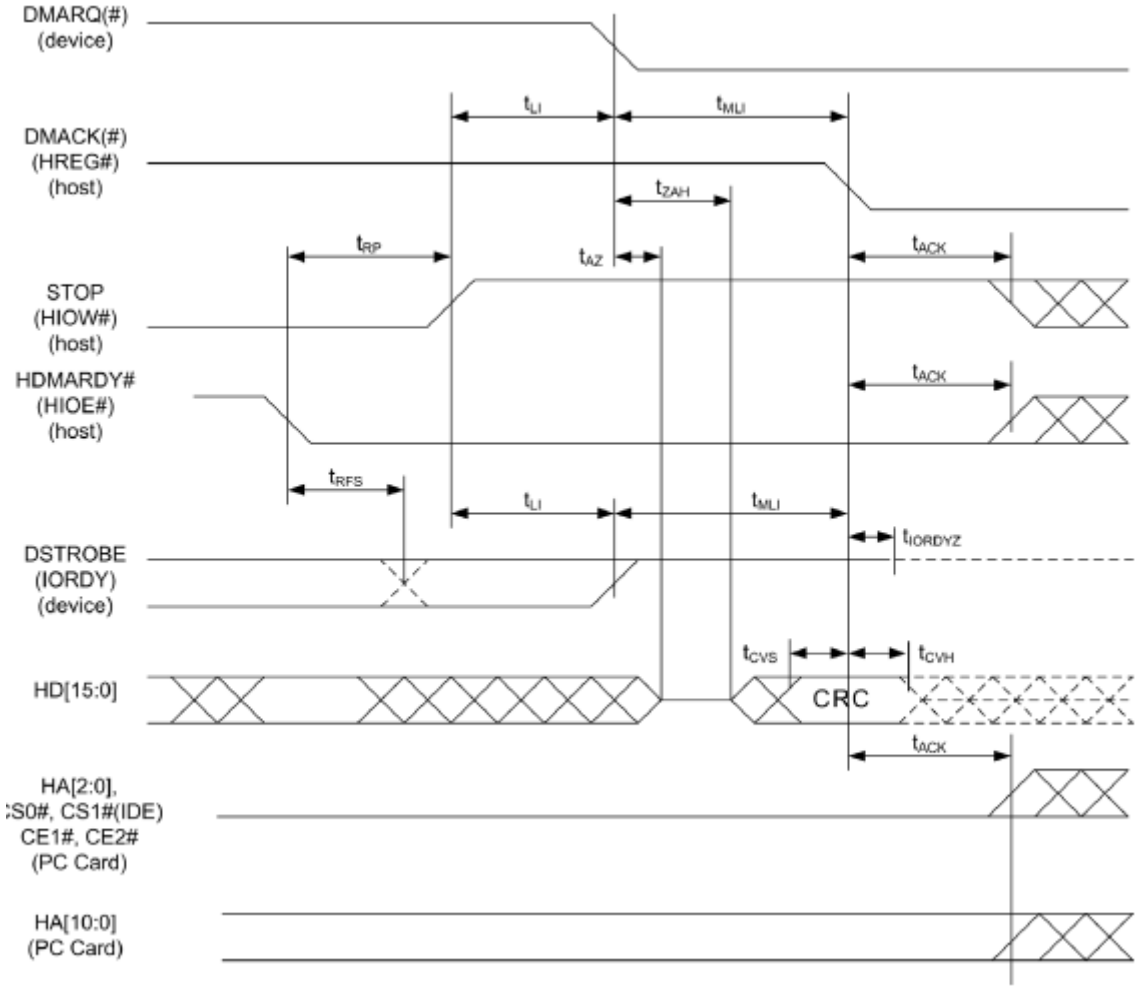
1. All waveforms in this diagram are shown with the asserted state high. Negative true signals are inverted on the bus relative to the diagram.
2. The host can implement STOP to request termination of the Ultra DMA data burst at a time no sooner than when tRP after HDMARDY# is negated.
3. After negating HDMARDY#, the host may receive zero, 1, 2, or 3 additional data words from the device.
4. Bus polarities of the DMARQ(#) and DMACK(#) signals are dependent on the active interface mode.

- **Ultra DMA Data-in Burst Device Termination Timing**



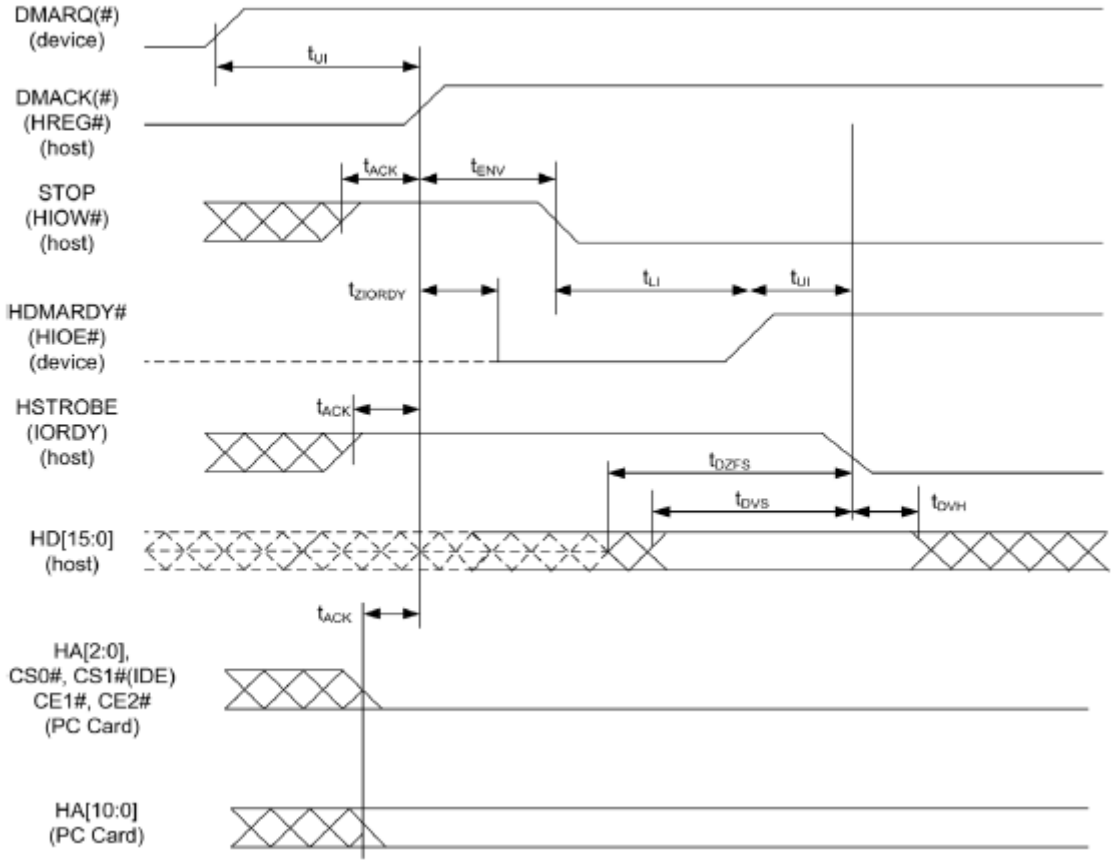
1. All waveforms in this diagram are shown with the asserted state high. Negative true signals are inverted on the bus relative to the diagram.
2. Definitions for STOP, HDMARDY#, and DSTROBE signal lines are no longer in effect once DMARQ(#) and DMACK(#) are negated. The HA[2:0], CS0# and CS1# are True IDE mode signal definitions. HA[10:0], CE1# and CE2# are PC Card mode signals. Bus polarities of DMARQ(#) and DMACK(#) are dependent on the active interface mode.

- **Ultra DMA Data-in Burst Host Termination Timing**



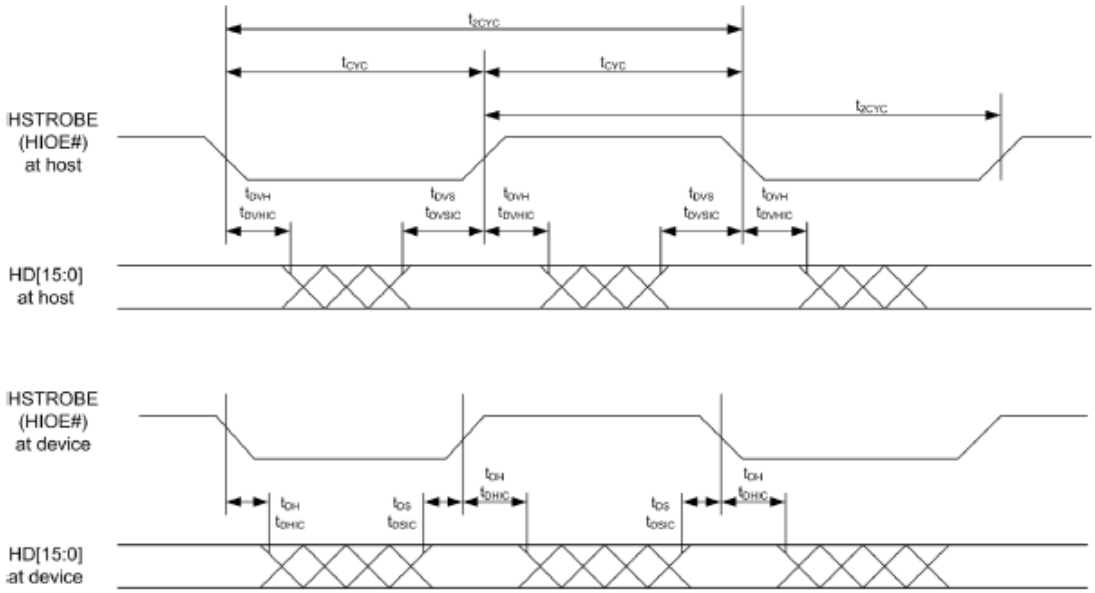
1. All waveforms in this diagram are shown with the asserted state high. Negative true signals are inverted on the bus relative to the diagram.
2. Definitions for STOP, HDMARDY#, and DSTROBE signal lines are no longer in effect once DMARQ(#) and DMACK(#) are negated. The HA[2:0], CS0# and CS1# are True IDE mode signal definitions. The HA[10:0], CE1# and CE2# are PC Card mode signal definitions. Bus polarities of DMARQ(#) and DMACK(#) are dependent on the active interface mode.

- **Ultra DMA Data-out Burst Initiation Timing**



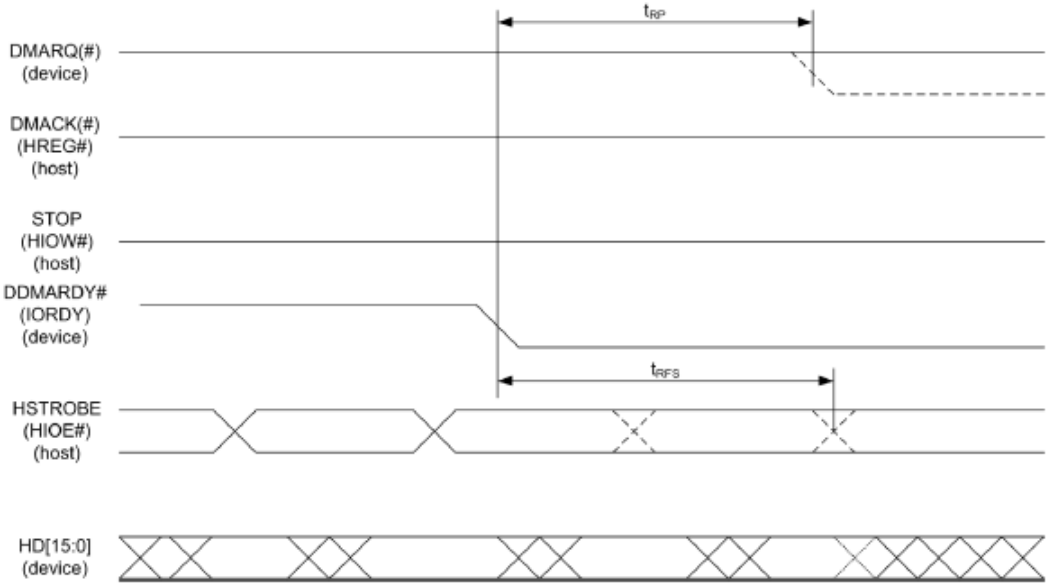
1. All waveforms in this diagram are shown with the asserted state high. Negative true signals are inverted on the bus relative to the diagram.
2. Definitions for STOP, DDMARDY#, and HSTROBE signal lines are not in effect until DMARQ(#) and DMACK(#) are asserted. The HA[2:0], CS0# and CS1# are True IDE mode signal definitions. The HA[10:0], CE1# and CE2# are PC Card mode signal definitions. Bus polarities of DMARQ(#) and DMACK(#) are dependent on the active interface mode.

- **Sustained Ultra DMA Data-out Burst Timing**



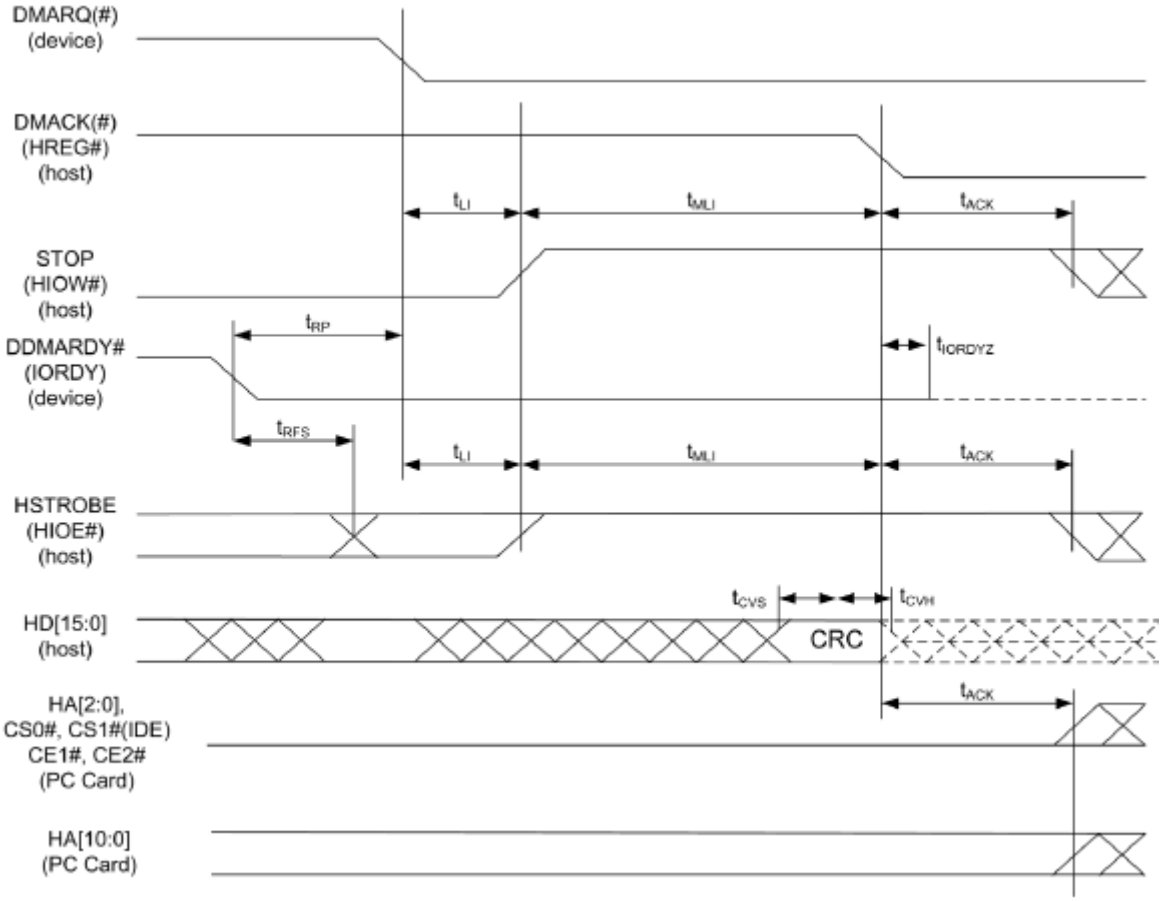
Data (HD[15:0]) and HSTROBE signals are shown at both the device and host to emphasize that neither cable settling time nor cable propagation delay allow for data signals to be considered stable at the device until after they are driven by a host.

- **Ultra DMA Data-out Burst Device Pause Timing**



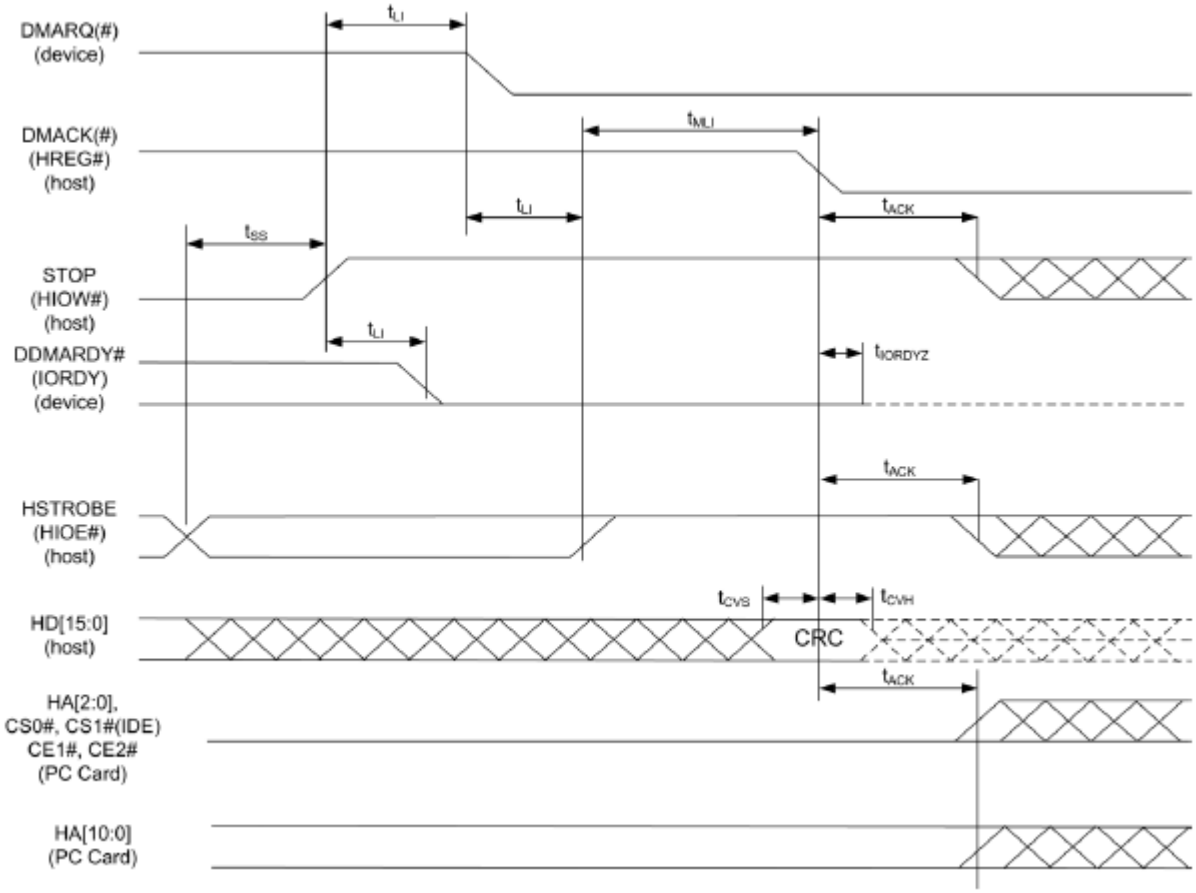
1. All waveforms in this diagram are shown with the asserted state high. Negative true signals are inverted on the bus relative to the diagram.
2. The device can negate DMARQ(#) when requesting termination of the Ultra DMA data burst no sooner than tRP after DDMARDY# is negated.
3. After negating DDMARDY#, the device may receive zero, 1, 2, or 3 additional data words from the host.
4. The bus polarities of DMARQ(#) and DMACK(#) are dependent on the active interface mode.

- **Ultra DMA Data-out Burst Device Termination Timing**



1. All waveforms in this diagram are shown with the asserted state high. Negative true signals are inverted on the bus relative to the diagram.
2. Definitions for the STOP, DDMARDY#, and HSTROBE signal lines are no longer in effect [after OR once] DMARQ(#) and DMACK(#) are negated. The HA[2:0], CS0# and CS1# are True IDE mode signal definitions. The HA[10:0], CE1# and CE2# are PC Card mode signals. Bus polarities of DMARQ(#) and DMACK(#) are dependent on the active interface mode.

- **Ultra DMA Data-out Burst Host Termination Timing**



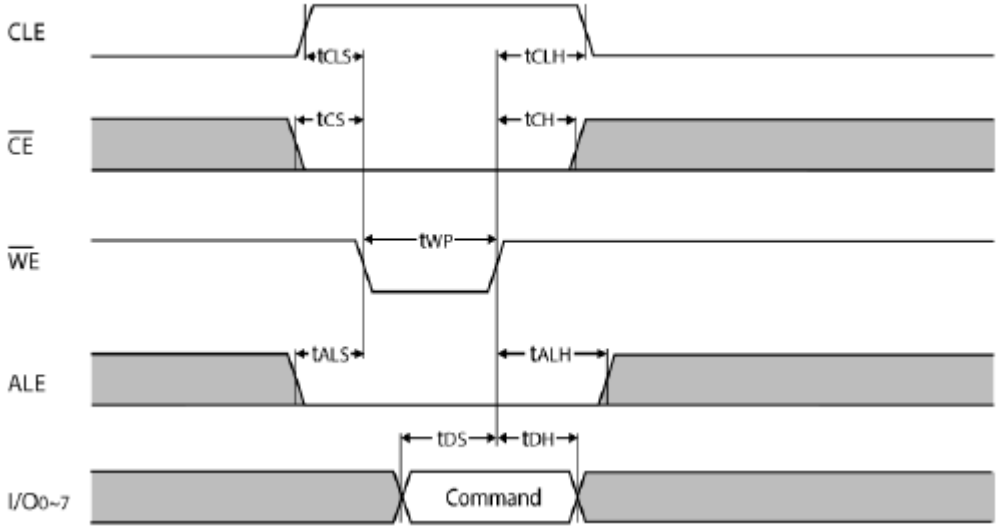
1. All waveforms in this diagram are shown with the asserted state high. Negative true signals are inverted on the bus relative to the diagram.
2. Definitions for the STOP, DDMARDY#, and HSTROBE signal lines are no longer in effect once DMARQ(#) and DMACK(#) are negated. The HA[2:0], CS0# and CS1# are True IDE mode signal definitions. The HA[10:0], CE1# and CE2# are PC Card mode signal definitions. Bus polarities of DMARQ(#) and DMACK(#) are dependent on the active interface mode.

- **Flash Interface AC Characteristics**

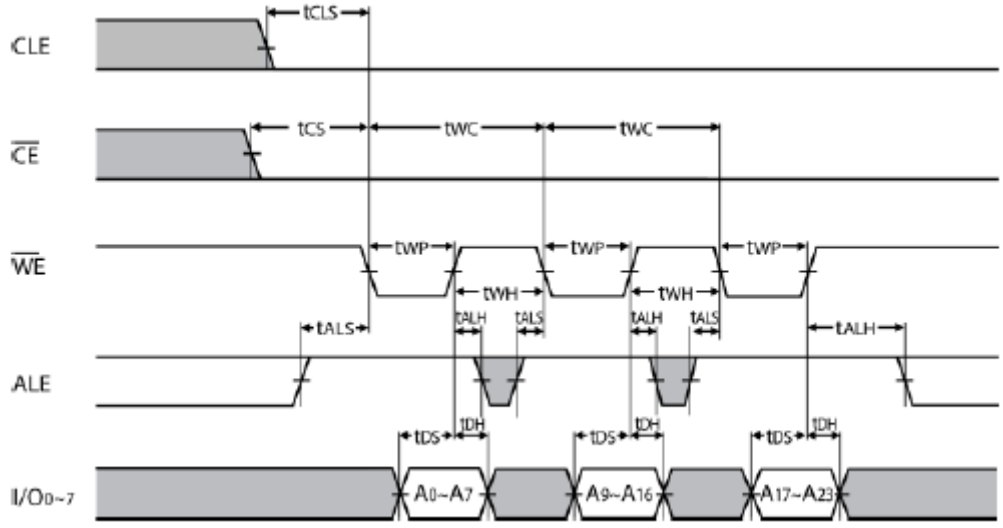
Parameter	Symbol	Timing		Unit
		Disable Flash CMD Extend	Enable Flash CMD Extend	
CLE Setup time	tCLS	2	4	tCK
CLE hold time	tCLH	1	2	tCK
ALE setup time	tALS	2	4	tCK
ALE hold time	tALH	1	2	tCK
WE pulse width	tWP	1	2	tCK
Data setup time	tDS	1	3	tCK
Data hold time	tDH	1	1	tCK
Write cycle time	tWC	2	4	tCK
WE high hold time	tWH	1	2	tCK
WE Low hold time	tWP	1	2	tCK

Parameter	Symbol	Timing	Unit
WE Pulse Width	tWP	0.5	tCK
Data setup time	tDS	0.75	tCK
Data hold time	tDH	0.25	tCK
Write cycle time	tWC	1	tCK
WE high hold time	tWH	0.5	tCK
WE pulse width	tWP	0.5	tCK
Read cycle time	tRC	1	tCK
RE Pulse Width	tRP	0.5	tCK
RE High Hold Time	tREH	0.5	tCK

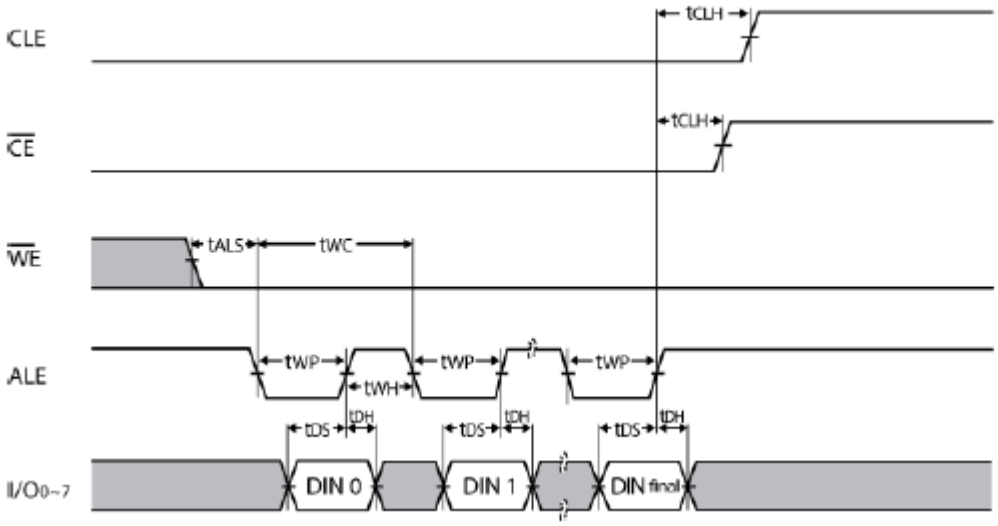
- **Command Latch Cycle**



- **Address Latch Cycle**



- **Input Data Latch Cycle**



7. Physical Characteristics

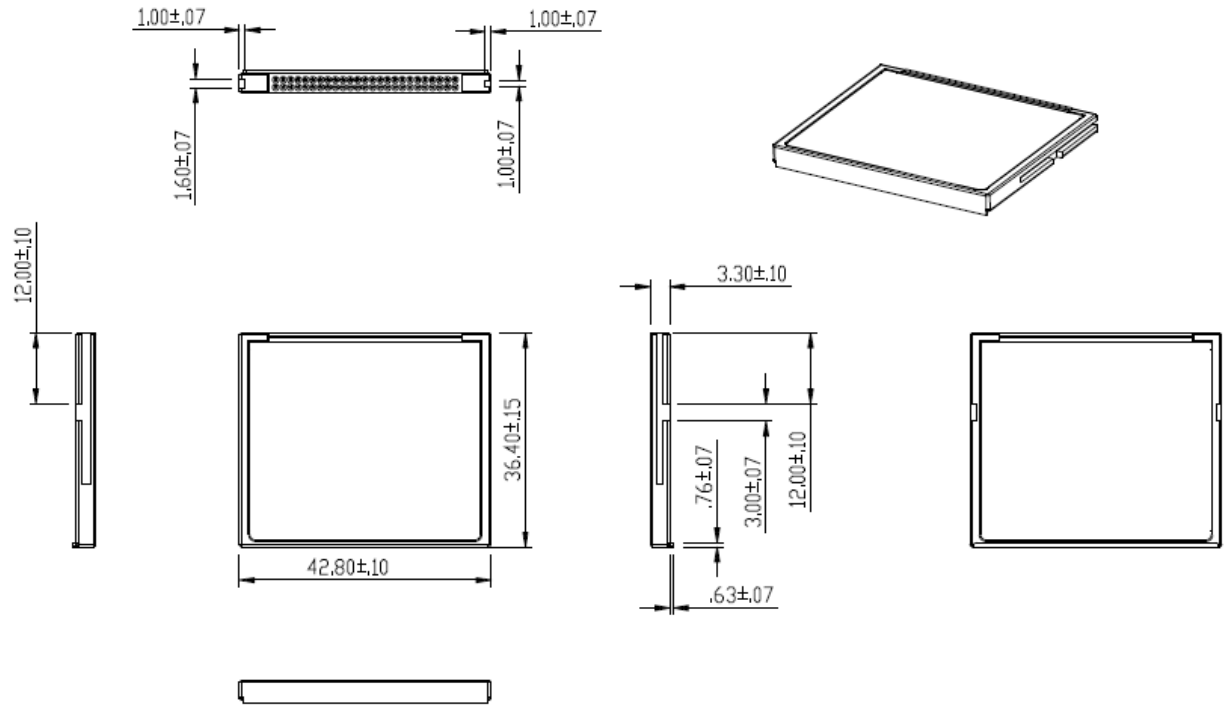


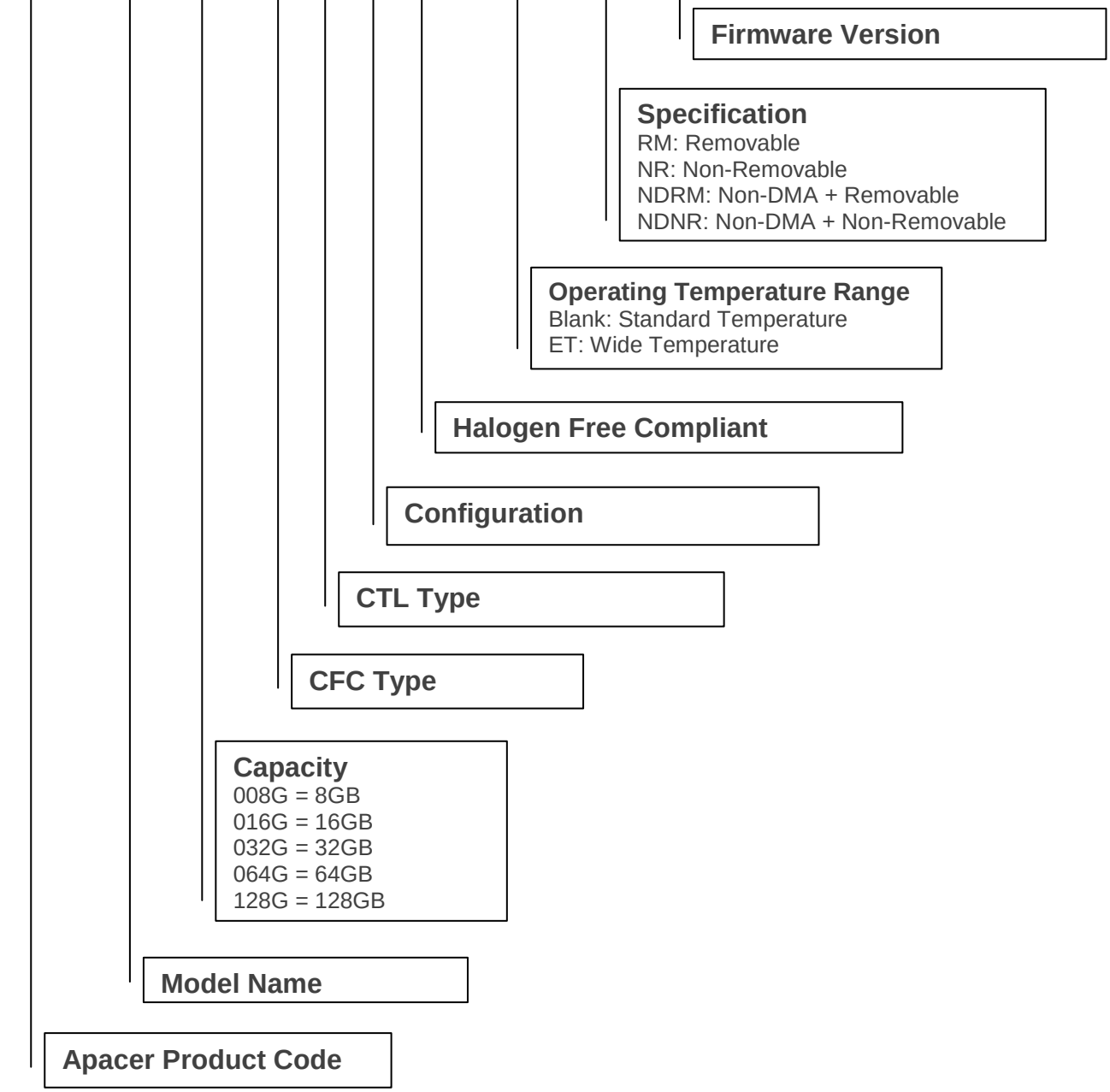
Figure 7-1 Physical Dimensions

Unit: mm

8. Product Ordering Information

8.1 Product Code Designations

A P – CF xxxG L A N S – XX XXXX C



8.2 Valid Combinations

A. Standard Temperature

8.2.1 Non-Removable

Capacity	Part Number
8GB	AP-CF008GLANS-NRG
16GB	AP-CF016GLANS-NRG
32GB	AP-CF032GLANS-NRG
64GB	AP-CF064GLANS-NRG
128GB	AP-CF128GLANS-NRG

8.2.2 Removable

Capacity	Part Number
8GB	AP-CF008GLANS-RMG
16GB	AP-CF016GLANS-RMG
32GB	AP-CF032GLANS-RMG
64GB	AP-CF064GLANS-RMG
128GB	AP-CF128GLANS-RMG

8.2.3 Non-DMA + Removable

Capacity	Part Number
8GB	AP-CF008GLANS-NDRMG
16GB	AP-CF016GLANS-NDRMG
32GB	AP-CF032GLANS-NDRMG
64GB	AP-CF064GLANS-NDRMG
128GB	AP-CF128GLANS-NDRMG

8.2.4 Non-DMA + Non-Removable

Capacity	Part Number
8GB	AP-CF008GLANS-NDNRG
16GB	AP-CF016GLANS-NDNRG
32GB	AP-CF032GLANS-NDNRG
64GB	AP-CF064GLANS-NDNRG
128GB	AP-CF128GLANS-NDNRG

B. Wide Temperature

8.2.5 Non-Removable

Capacity	Part Number
8GB	AP-CF008GLANS-ETNRG
16GB	AP-CF016GLANS-ETNRG
32GB	AP-CF032GLANS-ETNRG
64GB	AP-CF064GLANS-ETNRG
128GB	AP-CF128GLANS-ETNRG

8.2.6 Removable

Capacity	Part Number
8GB	AP-CF008GLANS-ETRMG
16GB	AP-CF016GLANS-ETRMG
32GB	AP-CF032GLANS-ETRMG
64GB	AP-CF064GLANS-ETRMG
128GB	AP-CF128GLANS-ETRMG

8.2.7 Non-DMA + Removable

Capacity	Part Number
8GB	AP-CF008GLANS-ETNDRMG
16GB	AP-CF016GLANS-ETNDRMG
32GB	AP-CF032GLANS-ETNDRMG
64GB	AP-CF064GLANS-ETNDRMG
128GB	AP-CF128GLANS-ETNDRMG

8.2.8 Non-DMA + Non-Removable

Capacity	Part Number
8GB	AP-CF008GLANS-ETNDNRG
16GB	AP-CF016GLANS-ETNDNRG
32GB	AP-CF032GLANS-ETNDNRG
64GB	AP-CF064GLANS-ETNDNRG
128GB	AP-CF128GLANS-ETNDNRG

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Revision History

Revision	Description	Date
0.1	Preliminary release	10/6/2015
0.2	Revised product ordering information due to FW change	11/5/2015
1.0	- Modified performance and power consumption values - Added extended temperature - Revised product ordering information	12/11/2015
1.1	- Revised product ordering information	1/13/2016
1.2	- Modified performance and power consumption values for 8-64GB - Revised product ordering information due to FW change	4/12/2016
1.3	Revised sectors value for 8GB	6/29/2016
1.4	Changed Wear-Leveling Algorithms to Global Wear Leveling at Flash Management on Specifications Overview page and 1.2 Intelligent Endurance Design	6/4/2018
1.5	- Renamed extended temperature to wide temperature - Updated supported versions of Ultra DMA Mode and PCMCIA UDMA Mode to 7 at CompactFlash Association Specification Revision 6.0 Standard Interface on Specifications Overview page and 1. General Descriptions	5/8/2019
1.6	- Updated technology description for 1.2.4 Power Failure Management - Updated 7. Physical Characteristics	8/2/2019

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