

RoHS Compliant

CFast 2.0

SM230-CFast 2.0 Product Specifications



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Version 1.1



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Specifications Overview:

- **Standard Serial ATA Interface**
 - SATA Revision 3.1 compliance
 - SATA 6.0 Gbps interface speed
 - Backward compatible with SATA 1.5 and 3.0 Gbps interfaces
 - ATA-compatible command set
- **Capacity**
 - 8, 16, 32, 64, 128, 256 GB
- **Performance***
 - Burst read/write: 600 MB/sec

Standard:

 - Sequential read: Up to 560 MB/sec
 - Sequential write: Up to 465 MB/sec
 - Random read (4K): Up to 38,000 IOPS
 - Random write (4K): Up to 41,000 IOPS

AES & Opal Implemented:

 - Sequential read: Up to 560 MB/sec
 - Sequential write: Up to 450 MB/sec
 - Random read (4K): Up to 37,000 IOPS
 - Random write (4K): Up to 41,000 IOPS
- **Flash Management**
 - Built-in hardware ECC
 - Global Wear Leveling
 - Flash bad-block management
 - Flash Translation Layer: Page Mapping
 - S.M.A.R.T.
 - Power Failure Management
 - Device Sleep (optional)
 - ATA Secure Erase
 - TRIM
- **NAND Flash Type:** MLC
- **MTBF:** >1,000,000 hours
- **Temperature Range**
 - Operating:
 - Standard: 0°C to 70°C
 - Extended: -40°C to 85°C
 - Storage: -40°C to 100°C
- **Power Consumption***
 - Supply voltage: 3.3V
 - Active mode: 645 mA
 - Idle mode: 135 mA
- **Connector Type**
 - 7 + 17 pin female connector
- **Hardware Write-Protection Switch Support (optional)**
- **Security (optional)**
 - Trusted Computing Group (TCG) Opal 2.0
 - AES 256-bit hardware encryption
- **RoHS Compliant**

*Varies from capacities. The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings.

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1. General Descriptions

Apacer SM230-CFast 2.0 is the latest enhancement of conventional CFast form factor that delivers various technological advantages. This new flash memory card comes with SATA 6.0 Gbps interface for higher performance and consists of SATA-based 7-pin signal segment and 17-pin for power and control purposes. Designed without DRAM on the internal controlling unit, SM230-CFast ensures data integrity by preventing data loss during a sudden power outage.

For data efficiency, SM230-CFast 2.0 delivers data transfer rates up to 560 MB/s in sequential access and 38,000 IOPS in 4KB random access. In addition, Apacer CFast cards come with S.M.A.R.T. for lifetime monitoring and customization support if write protection is required. Apacer SM230-CFast 2.0 guarantees reliability of applications in harsh environments by implementing intelligent Flash Management algorithms and Error Correction.

2. Functional Block

Apacer SM230-CFast 2.0 includes a single-chip SATA 6.0 Gbps and the flash media. The controller integrates the flash management unit to support multi-channel, multi-bank flash arrays. Figure 2-1 shows the functional block diagram.

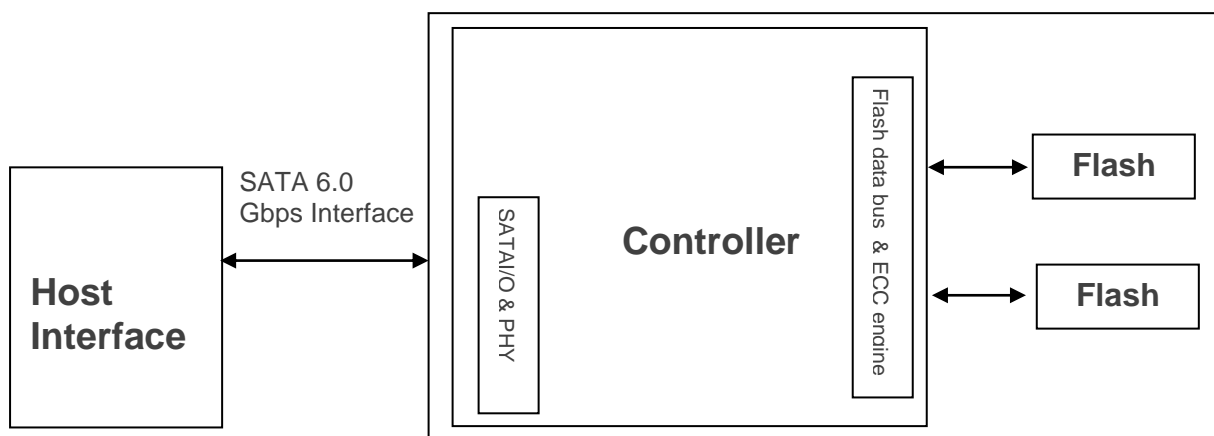


Figure 2-1 Functional Block Diagram

3. Pin Assignments

Table 3-1 describes SM230-CFast 2.0 signal segment, and Table 3-2, its power segment.



Figure 3-1 Pin Assignment

Table 3-1 Signal Segment

Pin	Definition	Description
S1	GND	Ground
S2	A+	SATA Differential Signal Pair A
S3	A-	
S4	GND	Ground
S5	B-	SATA Differential Signal Pair B
S6	B+	
S7	GND	Ground

Table 3-2 Power Segment

Pin	Definition	Type	Description
PC1	CDI	Input	Card Detect In
PC2	PGND	Device GND	Device GND
PC3	DEVSLP*	DEVSLP card input	DEVSLP enable
PC4			Reserved
PC5			Reserved
PC6			Reserved
PC7	PGND	Device GND	Device GND
PC8	LED1	LED Output	Power indicator
PC9	LED2	LED Output	Access indicator
PC10			Reserved
PC11			Write Protect**
PC12	IFDet	GND	Card output, connect to PGND on card
PC13	PWR	3.3V	Device power (3.3V)
PC14	PWR	3.3V	Device power (3.3V)
PC15	PGND	Device GND	Device GND
PC16	PGND	Device GND	Device GND
PC17	CDO	Output	Card Detect Out

*Optional

**Enabled by adjusting the pin "PC11" from high to low active (from 1Mohm to 100Kohm)

Notes about Write Protect:

Apacer implements the Virtual Write scheme that allows write commands to go through the flash controller and data is temporarily stored, but no data has been actually written into the flash. Once the host resets or restarts the system, all the temporarily stored data will disappear and nowhere to be found in the drive. Since the Virtual Write scheme runs at device level, it requires no software or driver installation and is independent from the host OS.

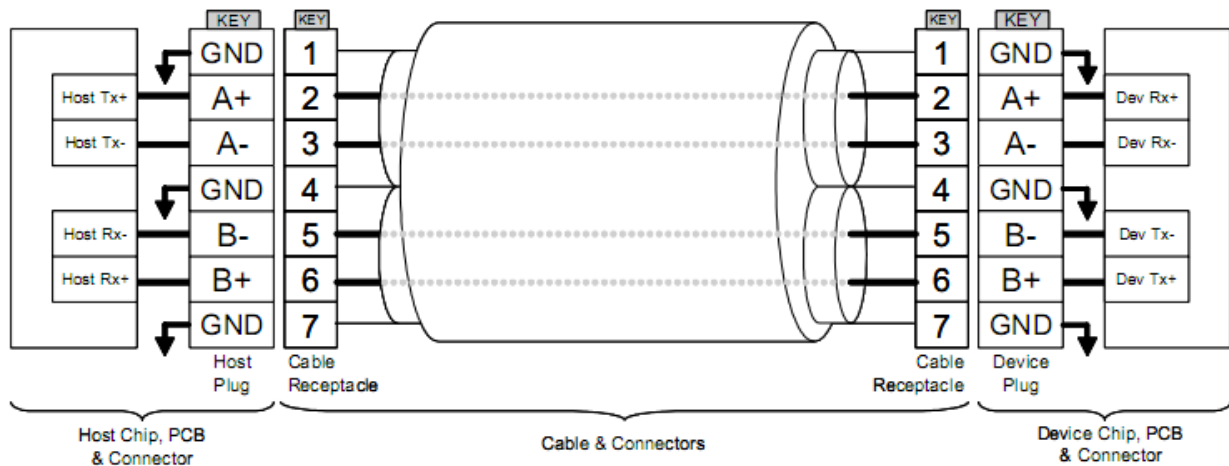


Figure 3-2 SATA Cable / Connector Connection Diagram

The connector on the left represents the Host with TX/RX differential pairs connected to a cable while the connector on the right shows the Device with TX/RX differential pairs also connected to the cable. Notice also the ground path connecting the shielding of the cable to the Cable Receptacle.

4. Product Specifications

4.1 Capacity

Capacity specifications of the SM230-CFast 2.0 are available as shown in Table 4-1. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

Table 4-1 Capacity Specifications

Capacity	Total bytes*	Cylinders	Heads	Sectors	Max LBA
8 GB	8,012,390,400	15,525	16	63	15,649,200
16 GB	16,013,942,784	16,383	16	63	31,277,232
32 GB	32,017,047,552	16,383	16	63	62,533,296
64 GB	64,023,257,088	16,383	16	63	125,045,424
128 GB	128,035,676,160	16,383	16	63	250,069,680
256 GB	256,060,514,304	16,383	16	63	500,118,192

*Display of total bytes varies from file systems, which means not all of the bytes can be used for storage.

**Notes: 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.

LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

4.2 Performance

Performance of SM230-CFast 2.0 product family is available as shown in Table 4-2 and 4-3.

Table 4-2 Performance Specifications (Standard)

Capacity	8 GB	16 GB	32 GB	64 GB	128 GB	256 GB
Performance						
Sequential Read* (MB/s)	135	280	560	560	560	555
Sequential Write* (MB/s)	60	125	270	235	450	465
Random Read IOPS** (4K)	8,000	14,000	24,000	23,000	38,000	38,000
Random Write IOPS** (4K)	3,000	7,000	16,000	18,000	38,000	41,000

Table 4-3 Performance Specifications (AES & Opal Implemented)

Capacity	8 GB	16 GB	32 GB	64 GB	128 GB	256 GB
Performance						
Sequential Read* (MB/s)	135	280	560	560	560	560
Sequential Write* (MB/s)	65	130	265	450	230	430
Random Read IOPS** (4K)	7,000	13,000	23,000	37,000	23,000	37,000
Random Write IOPS** (4K)	3,000	7,000	16,000	38,000	18,000	41,000

Note:

Results may differ from various flash configurations or host system setting.

*Sequential performance is based on CrystalDiskMark 5.2.1 with file size 1,000MB.

**Random performance measured using IOMeter with Queue Depth 32.

4.3 Environmental Specifications

Environmental specifications of SM230-CFast 2.0 are shown in Table 4-4.

Table 4-4 Environmental Specifications

Environment	Specifications
Temperature	0°C to 70°C (Standard); -40°C to 85°C (Extended)
	-40°C to 100°C (Non-operating)
Vibration	Non-operating: Sine wave, 15(G), 10~2000(Hz), Operating: Random, 7.69(GRMS), 20~2000(Hz)
Shock	Non-operating: Acceleration, 1,500 G, 0.5 ms Operating: Peak acceleration, 50 G, 11 ms

Note: This Environmental Specification table indicates the conditions for testing the device. Real world usages may affect the results.

4.4 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in SM230-CFast 2.0. Serving as statistical reference, the prediction result for SM230-CFast is more than 1,000,000 hours.

Note: The MTBF is predicated and calculated based on “Telcordia Technologies Special Report, SR-332, Issue 2” method.

4.5 Certification and Compliance

SM230-CFast 2.0 complies with the following standards:

- CE
- FCC
- RoHS
- MIL-STD-810G

5. Flash Management

5.1 Error Correction/Detection

SM230-CFast 2.0 implements a hardware ECC scheme, based on the BCH algorithm. It can detect and correct up to 76 bits error in 1K bytes.

5.2 Bad Block Management

Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. When host performs program/erase command on a block, bad block may appear in Status Register. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, page mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

5.3 Global Wear Leveling

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Global wear leveling is an important mechanism that levels out the wearing of all blocks so that the wearing-down of all blocks can be almost evenly distributed. This will increase the lifespan of SSDs.

5.4 Flash Translation Layer – Page Mapping

Page mapping is an advanced flash management technology whose essence lies in the ability to gather data, distribute the data into flash pages automatically, and then schedule the data to be evenly written. Page-level mapping uses one page as the unit of mapping. The most important characteristic is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different sizes of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. Thus, page mapping is adopted to increase random access speed and improve SSD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

5.5 ATA Secure Erase

ATA Secure Erase is an ATA disk purging command currently embedded in most of the storage drives. Defined in ATA specifications, (ATA) Secure Erase is part of Security Feature Set that allows storage drives to erase all user data areas. The erase process usually runs on the firmware level as most of the ATA-based storage media currently in the market are built-in with this command. ATA Secure Erase can securely wipe out the user data in the drive and protects it from malicious attack.

5.6 Power Failure Management

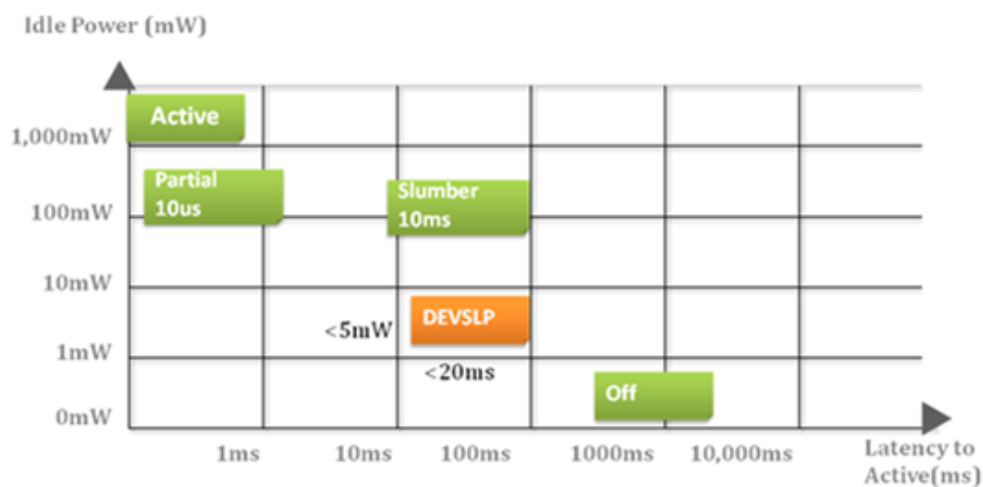
Power Failure Management plays a crucial role when experiencing unstable power supply. Power disruption may occur when users are storing data into the SSD. In this urgent situation, the controller would run multiple write-to-flash cycles to store the metadata for later block rebuilding. This urgent operation requires about several milliseconds to get it done. At the next power up, the firmware will perform a status tracking to retrieve the mapping table and resume previously programmed NAND blocks to check if there is any incompleteness of transmission.

5.7 TRIM

TRIM is a SATA command that helps improve the read/write performance and efficiency of solid-state drives (SSD). The command enables the host operating system to inform SSD controller which blocks contain invalid data, mostly because of the erase commands from host. The invalid will be discarded permanently and the SSD will retain more space for itself.

5.8 DEVSLP (DevSleep or DEVSLP) Mode (optional)

Device Sleep is a feature that allows SATA devices to enter a low power mode by designating pin 38 as DEVSLP signal with an aim to reducing power consumption.



Parameter	Description & Conditions	Min	Max
V_{DIn}	Tolerated input voltage.	-0.5 V	3.6 V
$V_{HAssert}$	Voltage presented to host if signal not driven low. Value specified for all allowable $I_{HAssert}$.	-	2.4 V
$I_{HNegate}$	Device current delivered to host if host driving signal low. Value specified at $V_{HNegate}$ voltage of 0 V.	-	100 μ A

5.9 SATA Power Management

By complying with SATA 6.0 Gb/s specifications, the SSD supports the following SATA power saving modes:

- ACTIVE: PHY ready, full power, Tx & Rx operational
- PARTIAL: Reduces power, resumes in under 10 μ s (microseconds)
- SLUMBER: Reduces power, resumes in under 10 ms (milliseconds)
- HIPM: Host-Initiated Power Management
- DIPM: Device-Initiated Power Management
- AUTO-SLUMBER: Automatic transition from partial to slumber.

Note: The behaviors of power management features would depend on host/device settings.

6. Security Features

6.1 TCG Opal (optional)

Developed by the Trusted Computing Group (TCG), an organization whose members work together to formulate industry standards, Opal is a set of security specifications used for applying hardware-based encryption to storage devices.

Hardware encryption has many advantages. First of all, it transfers the computational load of the encryption process to dedicated processors, reducing the stress on the host system's CPU. In addition, storage devices complying with Opal specifications are self-encryption devices. Opal specifications also feature boot authentication. When the drive is being accessed, the shadow MBR will request the drive password at boot. The drive will only unlock and decrypt if the correct password is supplied. The other feature is LBA-specific permissions. Users are assigned different permissions for LBA ranges created by the device administrator. Each LBA range is password-protected and can only be accessed by users with the correct key to perform permitted actions (read/write/erase).

6.2 Advanced Encryption Standard (optional)

Advanced Encryption Standard (AES) is a specification for the encryption of electronic data. AES has been adopted by the U.S. government since 2001 to protect classified information and is now widely implemented in embedded computing applications. The AES algorithm used in software and hardware is symmetric so that encrypting/decrypting requires the same encryption key. Without the key, the encrypted data is inaccessible to ensure information security.

Notably in flash memory applications, AES 256-bit hardware encryption is the mainstream to protect sensitive or confidential data. The hardware encryption provides better performance, reliability, and security than software encryption. It uses a dedicated processor, which is built inside the controller, to process the encryption and decryption. This enormously shortens the processing time and makes it efficient.

7. Software Interface

7.1 Command Set

Table 7-1 Command Set

Code	Command	Code	Command
E5h	Check Power Mode	F6h	Security Disable Password
90h	Execute Diagnostics	F3h	Security Erase Prepare
E7h	Flush Cache	F4h	Security Erase Unit
ECh	Identify Device	F5h	Security Freeze Lock
E3h	Idle	F1h	Security Set Password
E1h	Idle Immediate	F2h	Security Unlock
91h	Initialize Device Parameters	7Xh	Seek
C8h	Read DMA	EFh	Set Features
25h	Read DMA EXT	C6h	Set Multiple Mode
60h	Read FPDMA Queued	E6h	Sleep
47h	Read Log DMA EXT	B0h	S.M.A.R.T.
2Fh	Read Log EXT	E2h	Standby
C4h	Read Multiple	E0h	Standby Immediate
20 or 21h	Read Sector(s)	CAh	Write DMA
40 or 41h	Read Verify Sector(s)	35h	Write DMA EXT
10h	Recalibrate	61h	Write FPDMA Queued
57h	Write Log DMA EXT	3Fh	Write Log EXT
C5h	Write Multiple	30h or 31h	Write Sector(s)

7.2 S.M.A.R.T.

S.M.A.R.T. is an abbreviation for Self-Monitoring, Analysis and Reporting Technology, a self-monitoring system that provides indicators of drive health as well as potential disk problems. It serves as a warning for users from unscheduled downtime by monitoring and displaying critical drive information. Ideally, this should allow taking proactive actions to prevent drive failure and make use of S.M.A.R.T. information for future product development reference.

Apacer devices use the standard SMART command B0h to read data out from the drive to activate our S.M.A.R.T. feature that complies with the ATA/ATAPI specifications. S.M.A.R.T. Attribute IDs shall include initial bad block count, total later bad block count, maximum erase count, average erase count, power on hours and power cycle. When the S.M.A.R.T. Utility running on the host, it analyzes and reports the disk status to the host before the device reaches in critical condition.

Note: Attribute IDs may vary from product models due to various solution design and supporting capabilities.

Apacer memory products come with S.M.A.R.T. commands and subcommands for users to obtain information of drive status and to predict potential drive failures. Users can take advantage of the following commands/subcommands to monitor the health of the drive.

Code	SMART Subcommand
D0h	READ DATA
D1h	READ ATTRIBUTE THRESHOLDS
D2h	Enable/Disable Attribute Autosave
D4h	Execute Off-line Immediate
D5h	Read Log (optional)
D6h	Write Log (optional)
D8h	Enable Operations
D9h	Disable operations
DAh	Return Status

General SMART attribute structure

Byte	Description
0	ID (Hex)
1 – 2	Status flag
3	Value
4	Worst
5*-11	Raw Data

*Byte 5: LSB

SMART attribute ID list

ID (Hex)	Attribute Name
9 (0x09)	Power-on hours
12 (0x0C)	Power cycle count
163 (0xA3)	Max. erase count
164 (0xA4)	Avg. erase count
166 (0xA6)	Total later bad block count
167 (0xA7)	SSD Protect Mode (vendor specific)
168 (0xA8)	SATA PHY Error Count
175 (0xAF)	Bad Cluster Table Count
192 (0xC0)	Unexpected Power Loss Count
194 (0xC2)	Temperature
241 (0xF1)	Total sectors of write

8. Electrical Specifications

8.1 Operating Voltage

Table 8-1 lists the supply voltage for SM230-CFast 2.0.

Table 8-1 Operating Range

Parameter	Symbol	Min	Type	Max	Units
Power Supply	Vcc	3.135	3.3	3.465	V

8.2 Power Consumption

Table 8-2 lists the power consumption for SM230-CFast 2.0.

Table 8-2 Power Consumption

Mode \ Capacity	8 GB	16 GB	32 GB	64 GB	128 GB	256 GB
	Active (mA)	645	645	645	645	645
Idle (mA)	120	115	110	110	105	135

Note:

*All values are typical and may vary depending on flash configurations or host system settings.

**Active power is an average power measurement performed using CrystalDiskMark with 128KB sequential read/write transfers.

9. Physical Characteristics

9.1 Dimensions

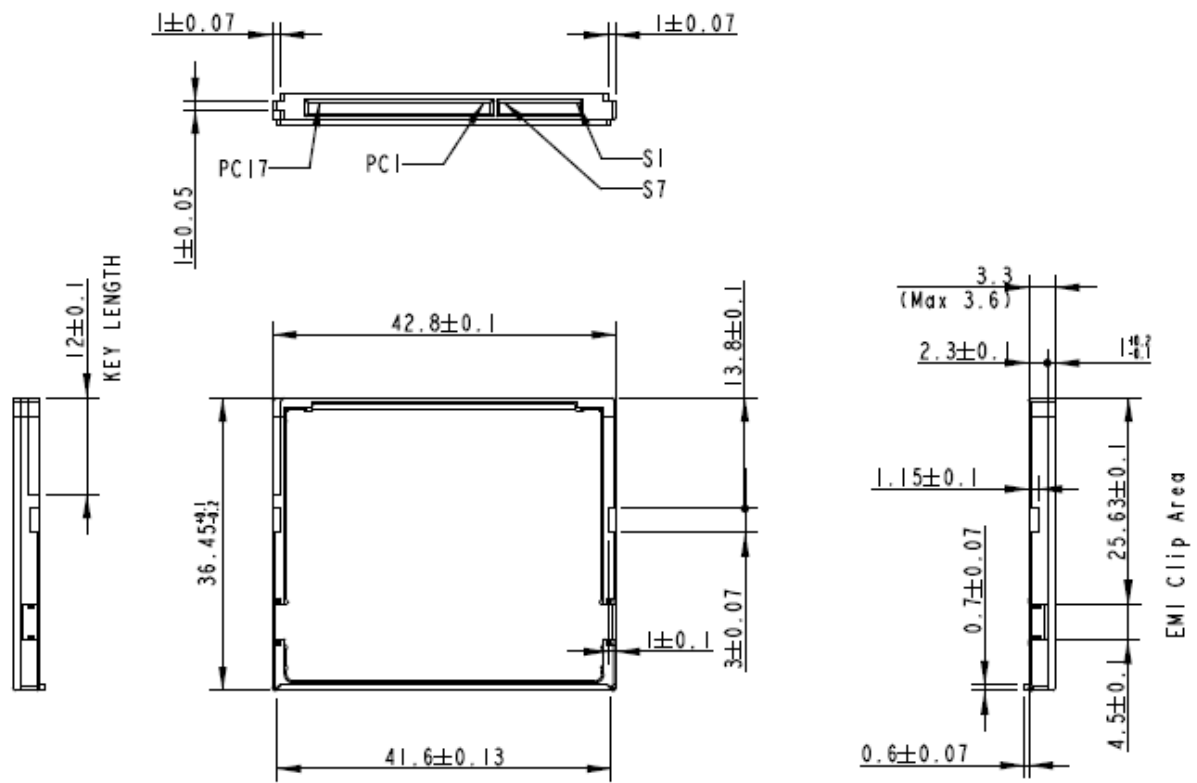
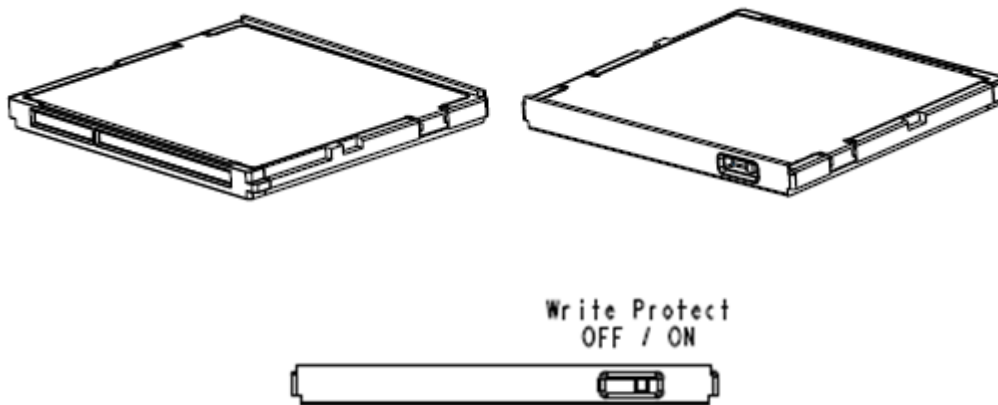


Figure 8-1 Physical Dimensions

Unit: mm

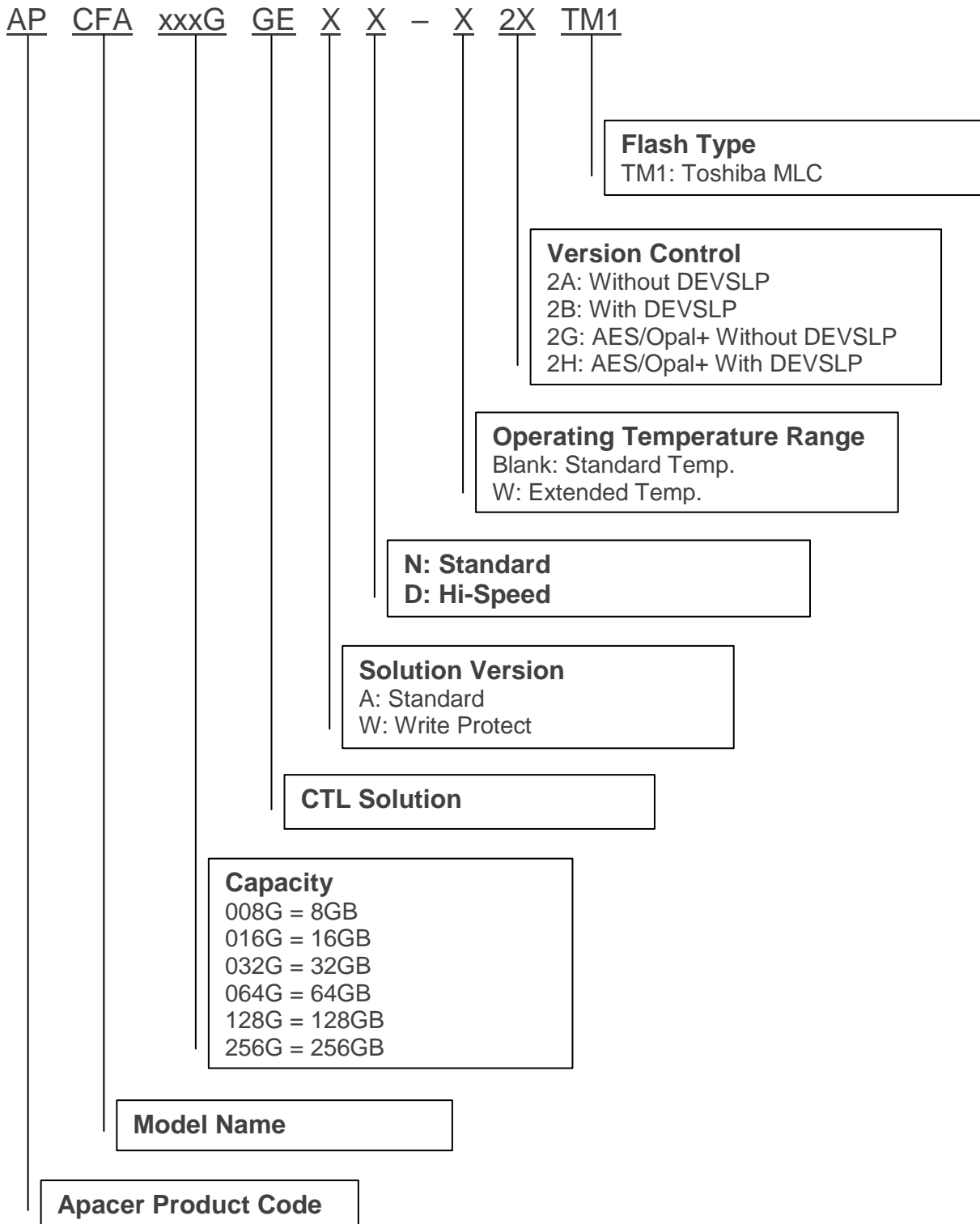
9.2 Write Protect Switch (optional)

Apacer implements the Virtual Write scheme that allows write commands to go through the flash controller and data temporarily stored, but no data has been actually written into the flash. Once the system is reset and rebooted, the temporarily stored data will be lost and nowhere to be found in the system. Since the Virtual Write scheme runs at device level, it requires no software or driver installation and is independent from the host OS.



10. Product Ordering Information

10.1 Product Code Designations



10.2 Valid Combinations

A. Standard

10.2.1 Without DEVSLP

Capacity	Standard Temperature	Extended Temperature
8GB	APCFA008GGEAN-2ATM1	APCFA008GGEAN-W2ATM1
16GB	APCFA016GGEAN-2ATM1	APCFA016GGEAN-W2ATM1
32GB	APCFA032GGEAD-2ATM1	APCFA032GGEAD-W2ATM1
64GB	APCFA064GGEAD-2ATM1	APCFA064GGEAD-W2ATM1
128GB	APCFA128GGEAD-2ATM1	APCFA128GGEAD-W2ATM1
256GB	APCFA256GGEAD-2ATM1	APCFA256GGEAD-W2ATM1

10.2.2 With DEVSLP

Capacity	Standard Temperature	Extended Temperature
8GB	APCFA008GGEAN-2BTM1	APCFA008GGEAN-W2BTM1
16GB	APCFA016GGEAN-2BTM1	APCFA016GGEAN-W2BTM1
32GB	APCFA032GGEAD-2BTM1	APCFA032GGEAD-W2BTM1
64GB	APCFA064GGEAD-2BTM1	APCFA064GGEAD-W2BTM1
128GB	APCFA128GGEAD-2BTM1	APCFA128GGEAD-W2BTM1
256GB	APCFA256GGEAD-2BTM1	APCFA256GGEAD-W2BTM1

10.2.3 Without DEVSLP + Write Protect

Capacity	Standard Temperature	Extended Temperature
8GB	APCFA008GGEWN-2ATM1	APCFA008GGEWN-W2ATM1
16GB	APCFA016GGEWN-2ATM1	APCFA016GGEWN-W2ATM1
32GB	APCFA032GGEWD-2ATM1	APCFA032GGEWD-W2ATM1
64GB	APCFA064GGEWD-2ATM1	APCFA064GGEWD-W2ATM1
128GB	APCFA128GGEWD-2ATM1	APCFA128GGEWD-W2ATM1
256GB	APCFA256GGEWD-2ATM1	APCFA256GGEWD-W2ATM1

10.2.4 With DEVSLP + Write Protect

Capacity	Standard Temperature	Extended Temperature
8GB	APCFA008GGEWN-2BTM1	APCFA008GGEWN-W2BTM1
16GB	APCFA016GGEWN-2BTM1	APCFA016GGEWN-W2BTM1
32GB	APCFA032GGEWD-2BTM1	APCFA032GGEWD-W2BTM1
64GB	APCFA064GGEWD-2BTM1	APCFA064GGEWD-W2BTM1
128GB	APCFA128GGEWD-2BTM1	APCFA128GGEWD-W2BTM1
256GB	APCFA256GGEWD-2BTM1	APCFA256GGEWD-W2BTM1

B. AES/Opal Function (optional)

10.2.5 Without DEVSLP

Capacity	Standard Temperature	Extended Temperature
8GB	APCFA008GGEAN- 2GTM1	APCFA008GGEAN-W2GTM1
16GB	APCFA016GGEAN- 2GTM1	APCFA016GGEAN-W2GTM1
32GB	APCFA032GGEAD- 2GTM1	APCFA032GGEAD-W2GTM1
64GB	APCFA064GGEAD- 2GTM1	APCFA064GGEAD-W2GTM1
128GB	APCFA128GGEAD- 2GTM1	APCFA128GGEAD-W2GTM1
256GB	APCFA256GGEAD- 2GTM1	APCFA256GGEAD-W2GTM1

10.2.6 With DEVSLP

Capacity	Standard Temperature	Extended Temperature
8GB	APCFA008GGEAN-2HTM1	APCFA008GGEAN-W2HTM1
16GB	APCFA016GGEAN-2HTM1	APCFA016GGEAN-W2HTM1
32GB	APCFA032GGEAD-2HTM1	APCFA032GGEAD-W2HTM1
64GB	APCFA064GGEAD-2HTM1	APCFA064GGEAD-W2HTM1
128GB	APCFA128GGEAD-2HTM1	APCFA128GGEAD-W2HTM1
256GB	APCFA256GGEAD-2HTM1	APCFA256GGEAD-W2HTM1

10.2.7 Without DEVSLP + Write Protect

Capacity	Standard Temperature	Extended Temperature
8GB	APCFA008GGEWN-2GTM1	APCFA008GGEWN-W2GTM1
16GB	APCFA016GGEWN-2GTM1	APCFA016GGEWN-W2GTM1
32GB	APCFA032GGEWD-2GTM1	APCFA032GGEWD-W2GTM1
64GB	APCFA064GGEWD-2GTM1	APCFA064GGEWD-W2GTM1
128GB	APCFA128GGEWD-2GTM1	APCFA128GGEWD-W2GTM1
256GB	APCFA256GGEWD-2GTM1	APCFA256GGEWD-W2GTM1

10.2.8 With DEVSLP + Write Protect

Capacity	Standard Temperature	Extended Temperature
8GB	APCFA008GGEWN-2HTM1	APCFA008GGEWN-W2HTM1
16GB	APCFA016GGEWN-2HTM1	APCFA016GGEWN-W2HTM1
32GB	APCFA032GGEWD-2HTM1	APCFA032GGEWD-W2HTM1
64GB	APCFA064GGEWD-2HTM1	APCFA064GGEWD-W2HTM1
128GB	APCFA128GGEWD-2HTM1	APCFA128GGEWD-W2HTM1
256GB	APCFA256GGEWD-2HTM1	APCFA256GGEWD-W2HTM1

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Revision History

Revision	Description	Date
1.0	Official release	7/17/2018
1.1	<ul style="list-style-type: none">- Removed Reliability section from Specifications Overview- Added "optional" to Device Sleep on Specifications Overview page and to 5.8 DEVSLP (DevSleep or DEVSLP) Mode- Removed 6.3 Thermal Sensor and 6.4 Thermal Management Technique	7/31/2018

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